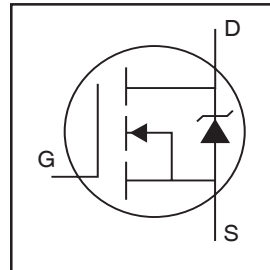


# IRFB4215PbF

HEXFET® Power MOSFET

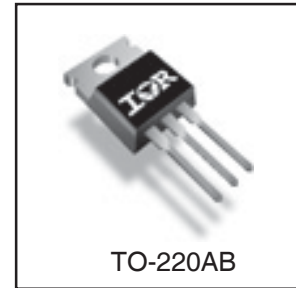
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Optimized for SMPS Applications
- Lead-Free



$V_{DSS} = 60V$
$R_{DS(on)} = 9.0m\Omega$
$I_D = 115A^{\textcircled{3}}$

## Description

Advanced HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.



## Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	115 <sup>③</sup>	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	81	
$I_{DM}$	Pulsed Drain Current ① ⑦	360	
$P_D @ T_C = 25^\circ C$	Power Dissipation	270	W
	Linear Derating Factor	1.8	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$I_{AR}$	Avalanche Current ①	85	A
$E_{AR}$	Repetitive Avalanche Energy ①	18	mJ
dv/dt	Peak Diode Recovery dv/dt ③ ⑦	4.7	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

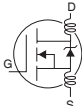
## Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.56	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

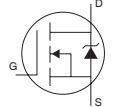
# IRFB4215PbF

International  
**IR** Rectifier

## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

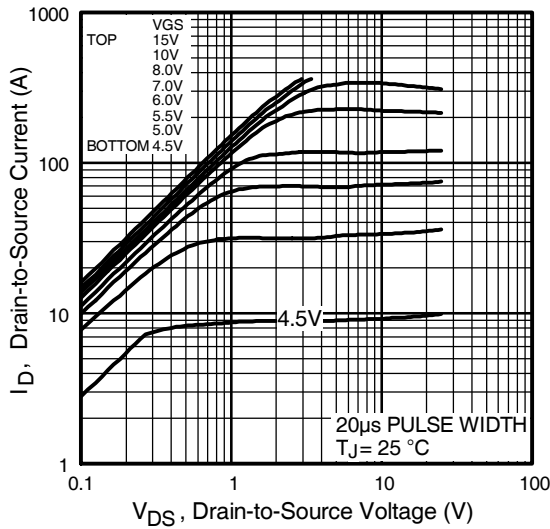
	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	60	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS/ΔT<sub>J</sub></sub>	Breakdown Voltage Temp. Coefficient	—	0.066	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	9.0	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 54A ④⑦
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
g <sub>fs</sub>	Forward Transconductance	61	—	—	S	V <sub>DS</sub> = 25V, I <sub>D</sub> = 54A④⑦
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> = 60V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 48V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V
Q <sub>g</sub>	Total Gate Charge	—	—	170	nC	I <sub>D</sub> = 64A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	39		V <sub>DS</sub> = 48V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	59		V <sub>GS</sub> = 10V, See Fig. 6 and 13⑦
t <sub>d(on)</sub>	Turn-On Delay Time	—	22	—	ns	V <sub>DD</sub> = 30V
t <sub>r</sub>	Rise Time	—	160	—		I <sub>D</sub> = 64A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	77	—		R <sub>G</sub> = 6.2Ω
t <sub>f</sub>	Fall Time	—	110	—		V <sub>GS</sub> = 10V, See Fig. 10 ④⑦
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		
C <sub>iss</sub>	Input Capacitance	—	4080	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	840	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	180	—		f = 1.0MHz, See Fig. 5⑦
E <sub>AS</sub>	Single Pulse Avalanche Energy②	—	1080③	220⑥		mJ

## Source-Drain Ratings and Characteristics

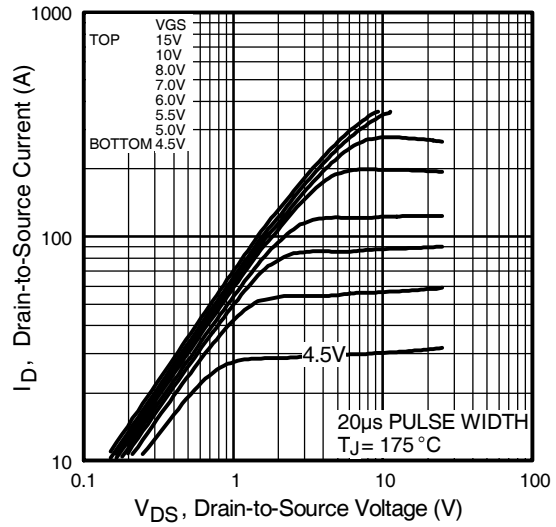
	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	115⑧	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode)①	—	—	360		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.2	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 90A, V <sub>GS</sub> = 0V ④⑦
t <sub>rr</sub>	Reverse Recovery Time	—	78	120	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 64A
Q <sub>rr</sub>	Reverse Recovery Charge	—	250	380	nC	di/dt = 100A/μs ④⑦
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

### Notes:

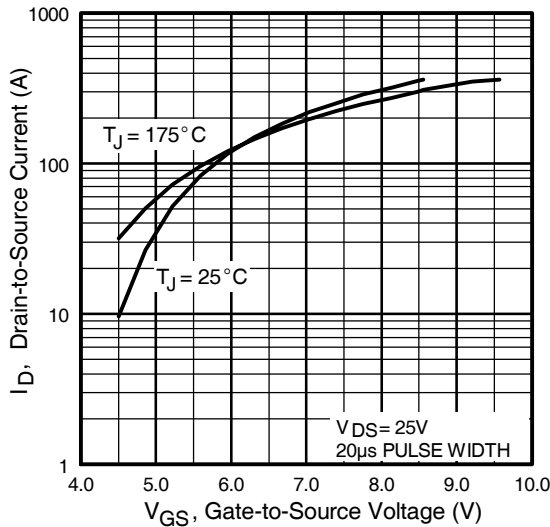
- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting T<sub>J</sub> = 25°C, L = 60μH  
R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 85A, V<sub>GS</sub> = 10V (See Figure 12)
- ③ I<sub>SD</sub> ≤ 90A, di/dt ≤ 250A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>,  
T<sub>J</sub> ≤ 175°C
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑤ This is a typical value at device destruction and represents operation outside rated limits.
- ⑥ This is a calculated value limited to T<sub>J</sub> = 175°C.
- ⑦ This is tested with same test conditions as the existing data sheet
- ⑧ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.



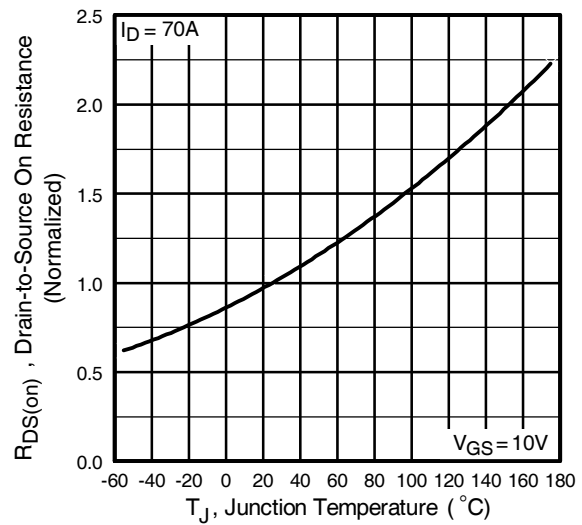
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics



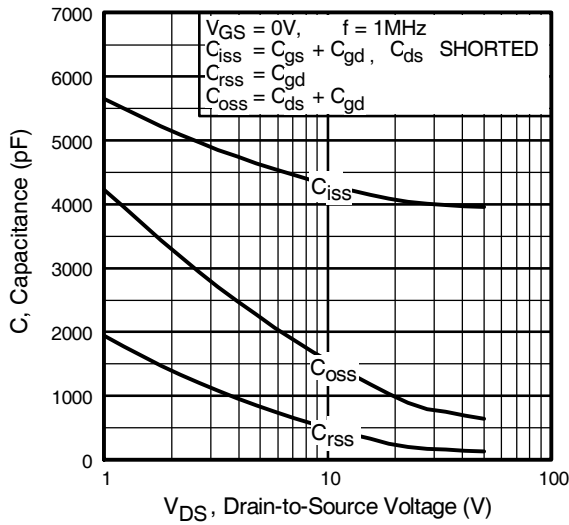
**Fig 3.** Typical Transfer Characteristics



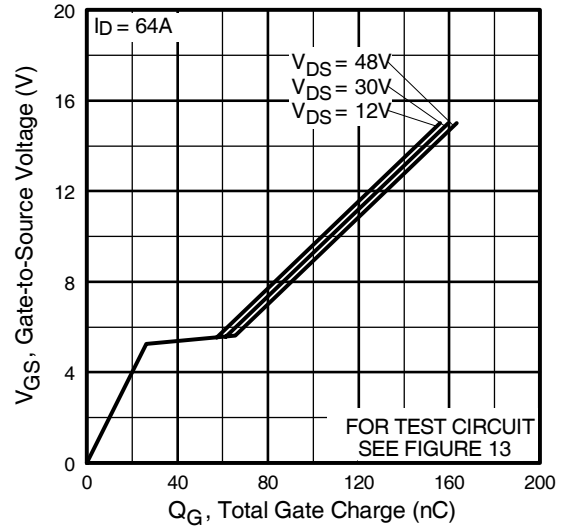
**Fig 4.** Normalized On-Resistance Vs. Temperature

# IRFB4215PbF

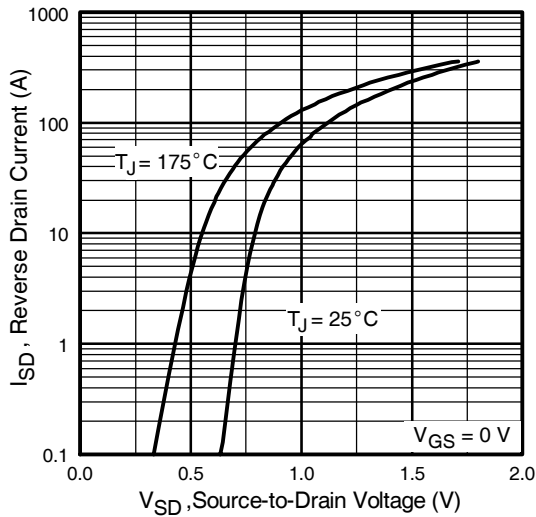
International  
**IR** Rectifier



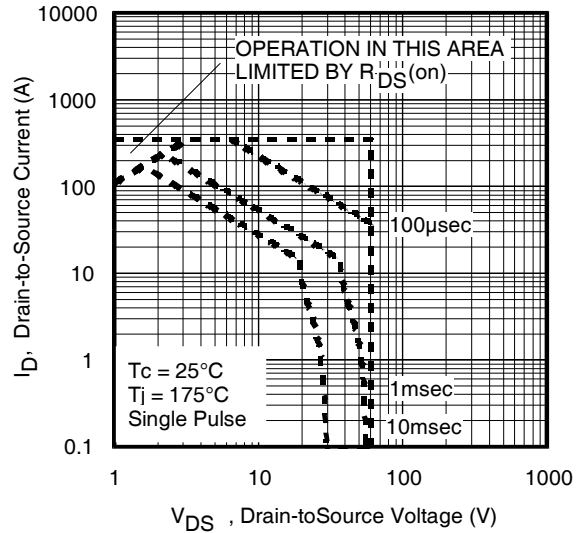
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



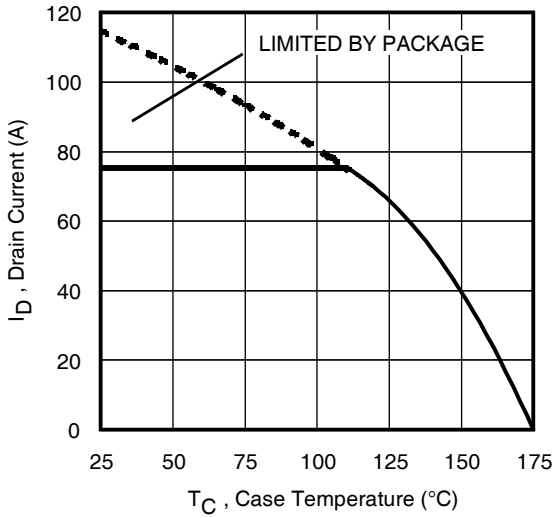
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area



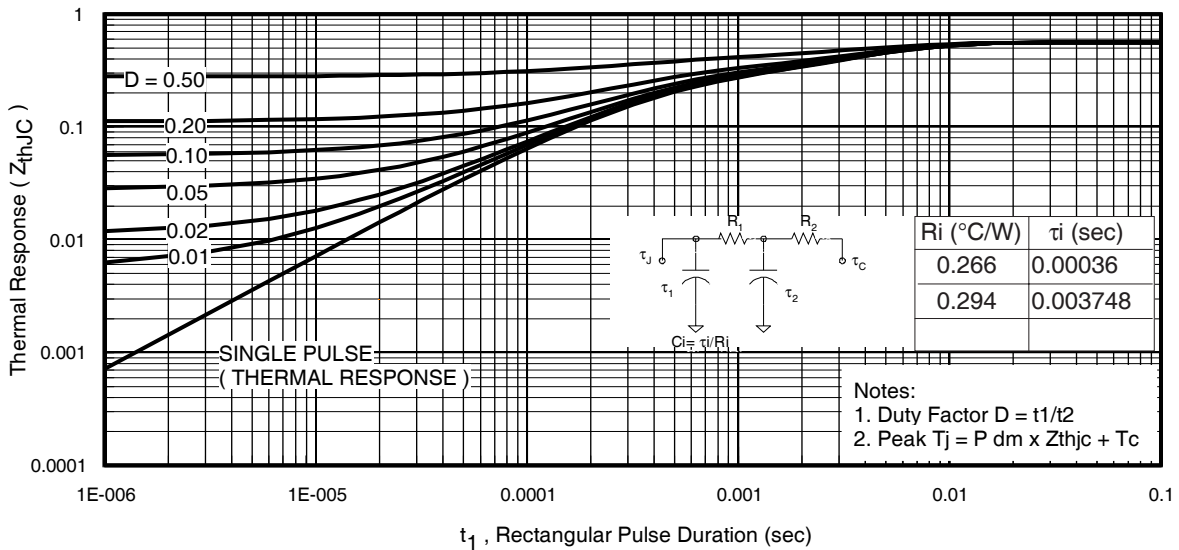
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit

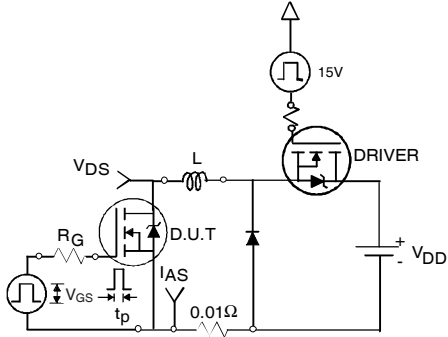


**Fig 10b.** Switching Time Waveforms



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

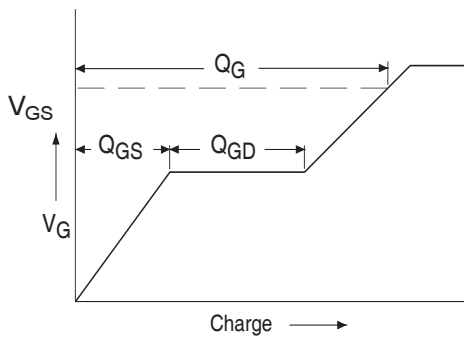
# IRFB4215PbF



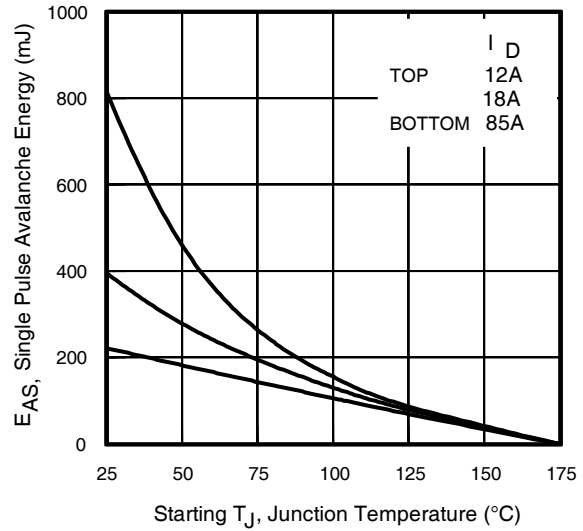
**Fig 12a.** Unclamped Inductive Test Circuit



**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform

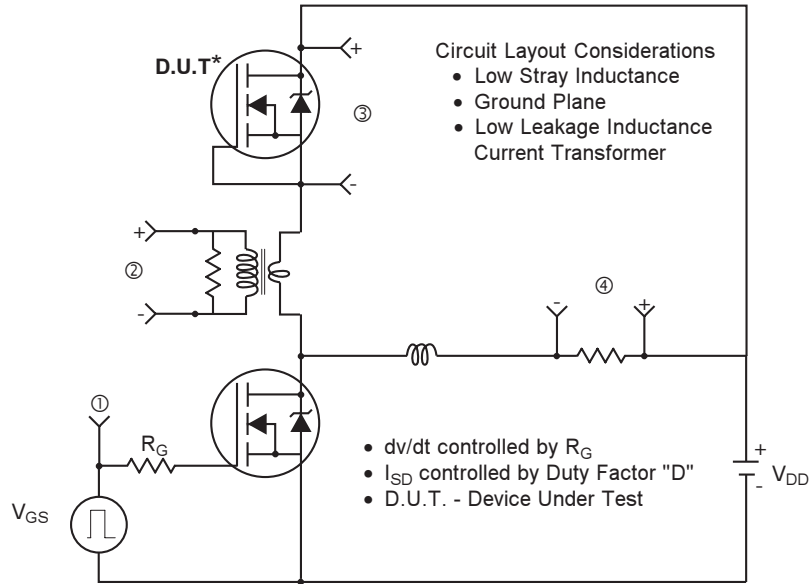


**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13b.** Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



\* Reverse Polarity of D.U.T for P-Channel



\*\*\*  $V_{GS} = 5.0V$  for Logic Level and 3V Drive Devices

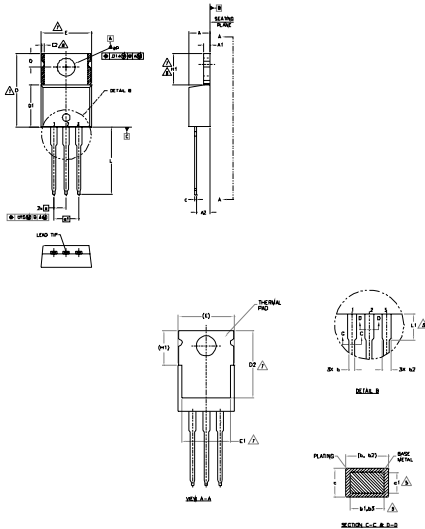
Fig 14. For N-channel HEXFET® power MOSFETs

# IRFB4215PbF

## TO-220AB Package Outline

Dimensions are shown in millimeters (inches)

International  
**IR** Rectifier



- NOTES:
- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
  - 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
  - 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
  - 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
  - 5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
  - 6.- CONTROLLING DIMENSION - INCHES.
  - 7.- THERMAL PAD CONTOUR OPTIONAL. WITHIN DIMENSIONS E1, D2 & E1.
  - 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
  - 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	5
b1	0.38	0.97	.015	.038	
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	-	0.76	-	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.96	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

**LEAD ASSIGNMENTS**

- HEXITE**
- 1- GATE
  - 2- DRAIN
  - 3- SOURCE

**IRFBL GATE**

- 1- GATE
- 2- COLLECTOR
- 3- EMITTER

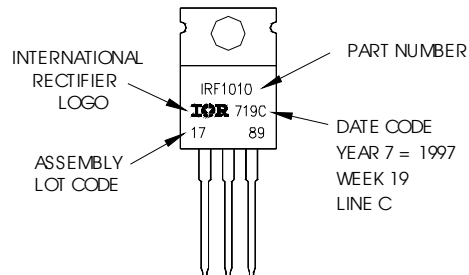
**DOCKS**

- 1- ANODE
- 2- CATHODE
- 3- ANODE

## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
LOT CODE 1789  
ASSEMBLED ON WW 19, 1997  
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position  
indicates "Lead-Free"



TO-220AB packages are not recommended for Surface Mount Application.

**Notes:**

1. For an Automotive Qualified version of this part please see <http://www.irf.com/product-info/auto/>
2. For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Data and specifications subject to change without notice.  
This product has been designed and qualified for the Industrial market.  
Qualification Standards can be found on IR's Web site.

International  
**IR** Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
TAC Fax: (310) 252-7903

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