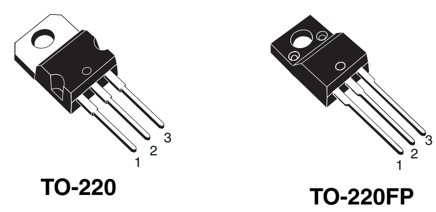
STP9NK65Z
STP9NK65ZFP

N-channel 650 V - 1 Ω - 6.4 A TO-220 / TO-220FP Zener-protected SuperMESH™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$	I_D	Pw
STP9NK65ZFP	650 V	< 1.2 Ω	6.4 A	125 W
STP9NK65Z	650 V	< 1.2 Ω	6.4 A	30 W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability



Application

- Switching applications

Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

Figure 1. Internal schematic diagram

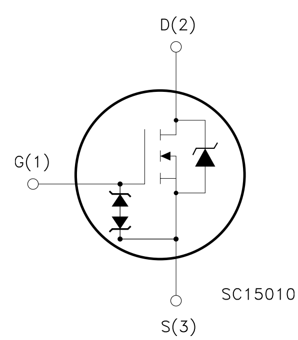


Table 1. Device summary

Order codes	Marking	Package	Packaging
STP9NK65ZFP	P9NK65ZFP	TO-220FP	Tube
STP9NK65Z	P9NK65Z	TO-220	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
V_{DS}	Drain-source voltage (V_{GS} = 0)	650		V
V_{GS}	Gate- source voltage	± 30		V
I_D	Drain current (continuous) at T_C = 25 °C	6.4	6.4 (1)	A
I_D	Drain current (continuous) at T_C = 100 °C	4	4(1)	A
I_{DM} (2)	Drain current (pulsed)	25.6	25.6 (1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	125	30	W
	Derating factor	1	0.24	W/°C
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100 pF, R=1.5 kΩ)	4000		V
dv/dt (3)	Peak diode recovery voltage slope	4.5		V/ns
V_{ISO}	Insulation withstand voltage (DC)	-	2500	V
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150 -55 to 150		°C °C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. I_{SD} ≤ 6.4 A, di/dt ≤ 200 A/µs, V_{DD} ≤ 80%$V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
Rthj-case	Thermal resistance junction-case max	1	4.2	°C/W
Rthj-amb	Thermal resistance junction-ambient max	62.5		°C/W
T_l	Maximum lead temperature for soldering purpose	300		°C

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	6.4	A
E_{AS}	Single pulse avalanche energy (starting T_j=25 °C, I_D=I_{AR}, V_{DD}=50 V)	200	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	650			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, @125 °C			1 50	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 3.2 A		1	1.2	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15 V, I_D = 3.2 A		6		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0		1145 130 28		pF pF pF
$C_{oss\ eq}$(2).	Equivalent output capacitance	V_{GS} = 0, V_{DS} = 0 to 400 V		55		pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 520 V, I_D = 6.4 A, V_{GS} = 10 V (see *Figure 18*)		41 7.5 22		nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD} = 325 V, I_D = 3.2 A R_G = 4.7 Ω V_{GS} = 10 V (see *Figure 17*)		20 12		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	V_{DD} = 325 V, I_D = 3.2 A R_G = 4.7 Ω V_{GS} = 10 V (See *Figure 17*)		45 15		ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				6.4 25.6	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 6.4 A, V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 6.4 A, di/dt = 100 A/µs V_{DD} = 50 V, T_j = 150 °C (see *Figure 19*)		400 2600 13		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

Table 9. Gate-source zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO} (1)	Gate-source breakdown voltage	Igs=±1 mA (open drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

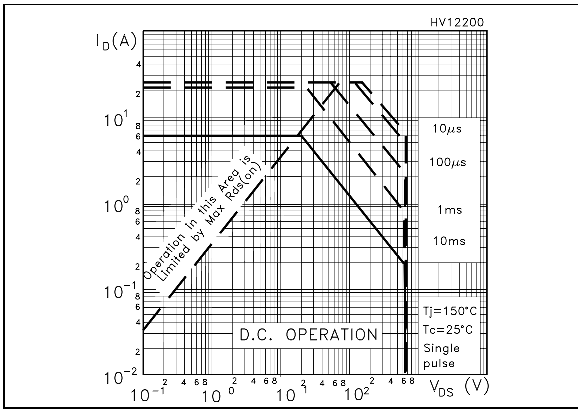


Figure 2. Safe operating area for TO-220

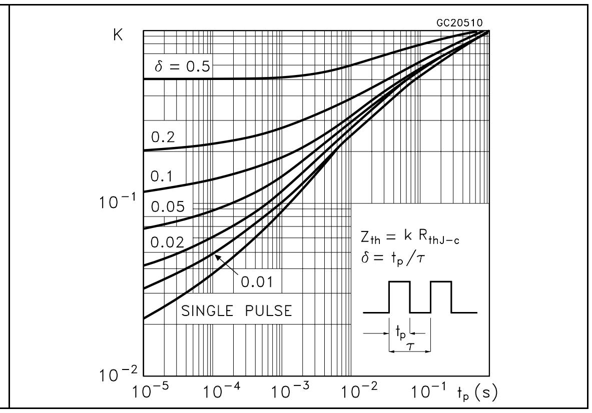


Figure 3. Thermal impedance for TO-220

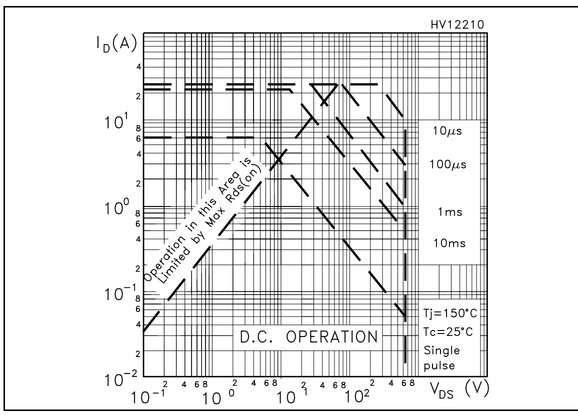


Figure 4. Safe operating area for TO-220FP

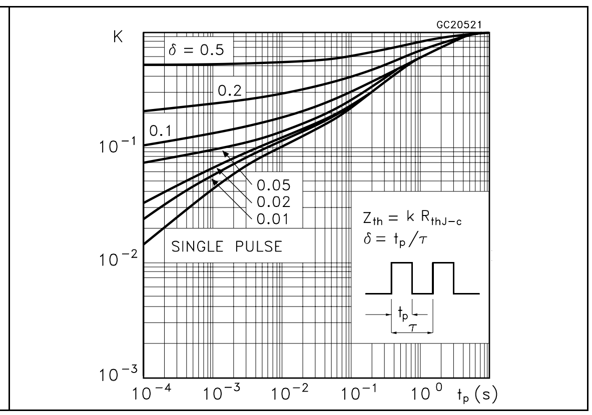


Figure 5. Thermal impedance for TO-220FP

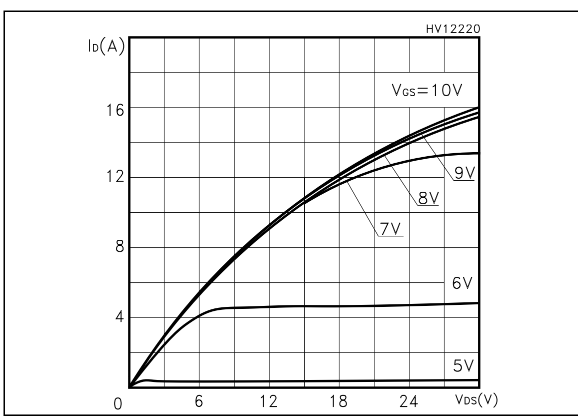


Figure 6. Output characteristics

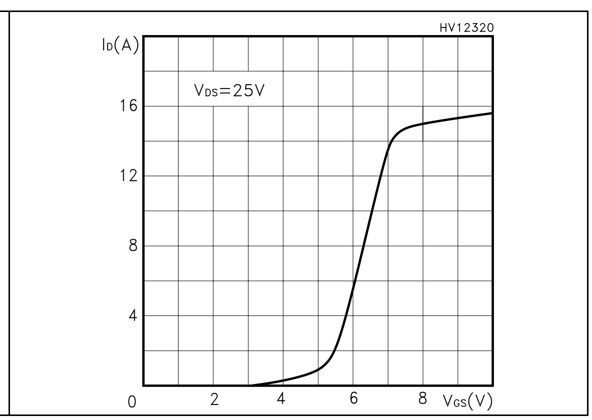


Figure 7. Transfer characteristics

Figure 8. Transconductance

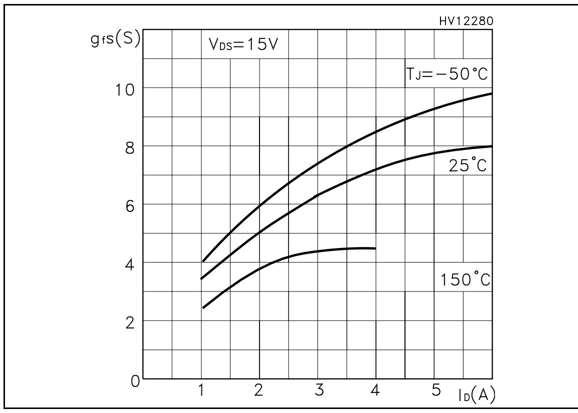


Figure 9. Static drain-source on resistance

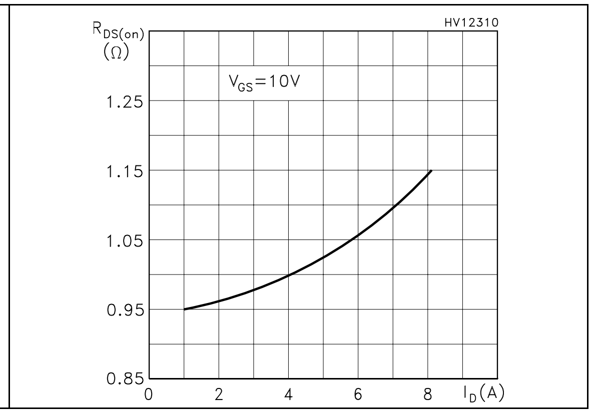


Figure 10. Gate charge vs gate-source voltage

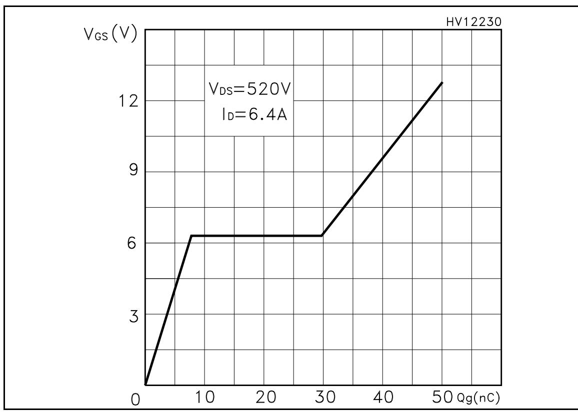


Figure 11. Capacitance variations

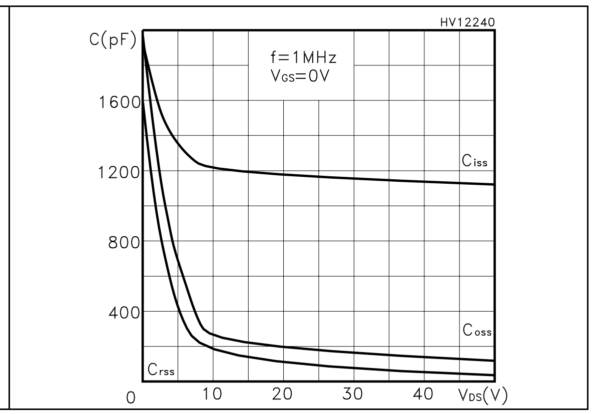


Figure 12. Normalized gate threshold voltage vs temperature

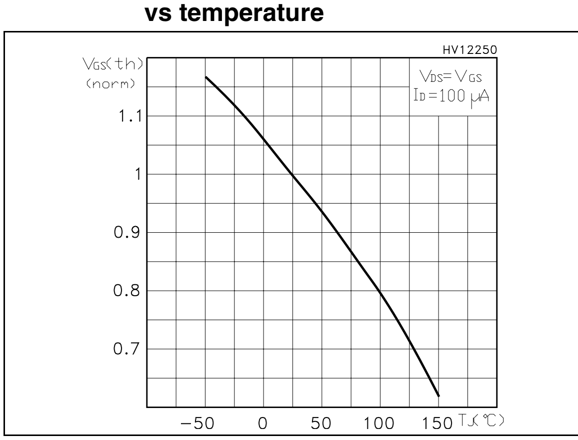


Figure 13. Normalized on resistance vs temperature

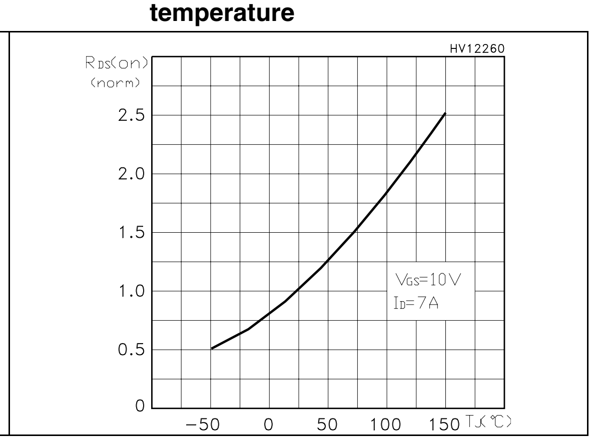


Figure 14. Source-drain diode forward characteristics

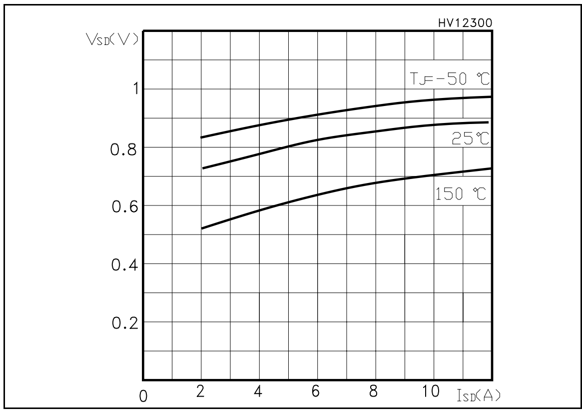


Figure 15. Normalized BV_{DSS} vs temperature

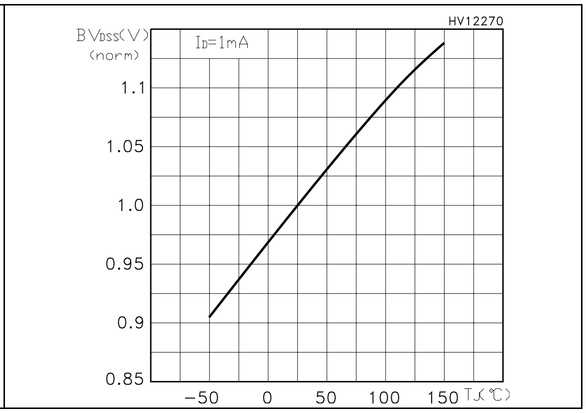
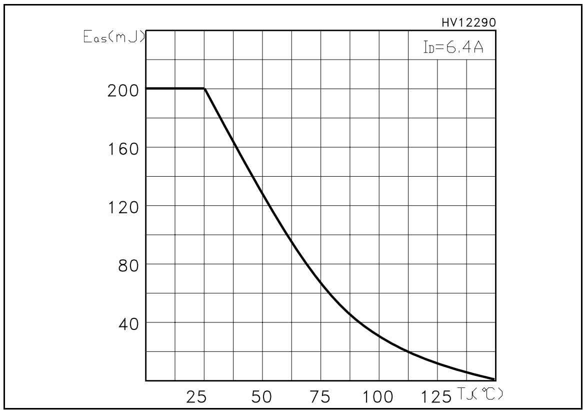


Figure 16. Maximum avalanche energy vs temperature



3 Test circuits

Figure 17. Switching times test circuit for resistive load

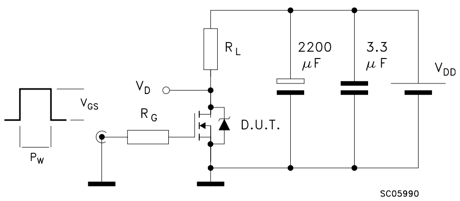


Figure 18. Gate charge test circuit

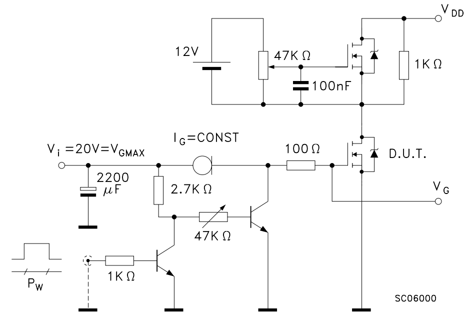


Figure 19. Test circuit for inductive load switching and diode recovery times

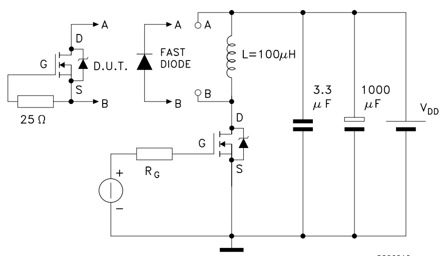


Figure 20. Unclamped Inductive load test circuit

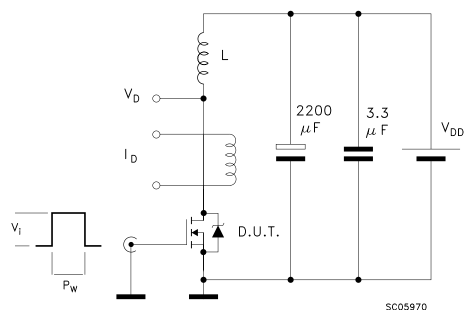


Figure 21. Unclamped inductive waveform

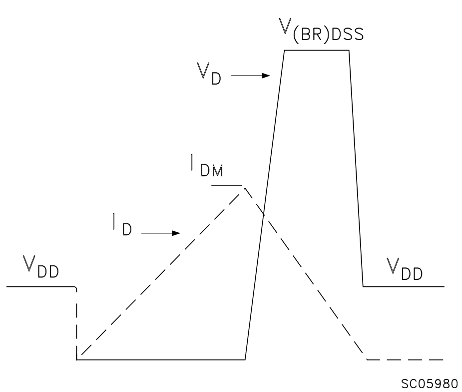
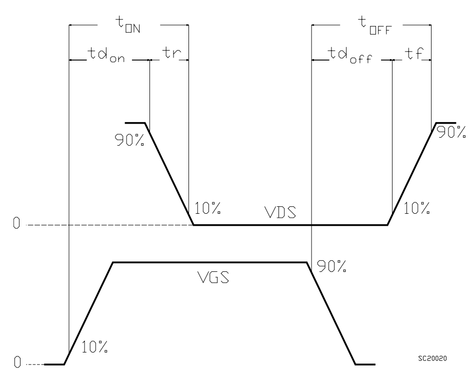


Figure 22. Switching time waveform

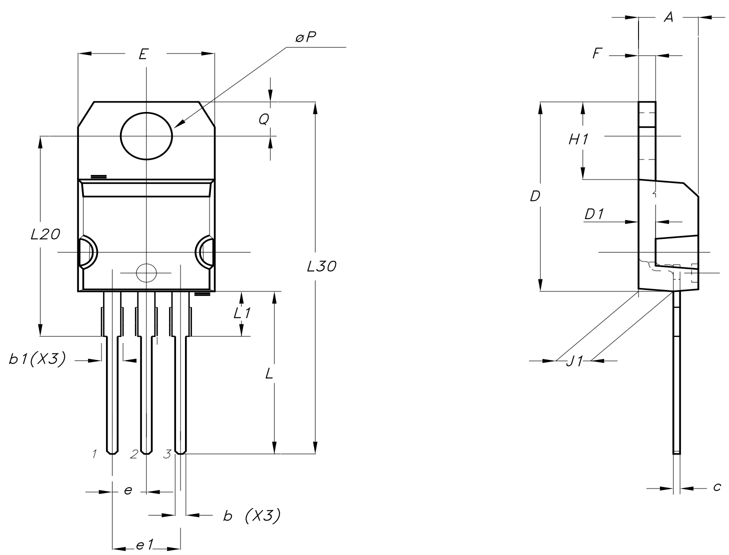


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

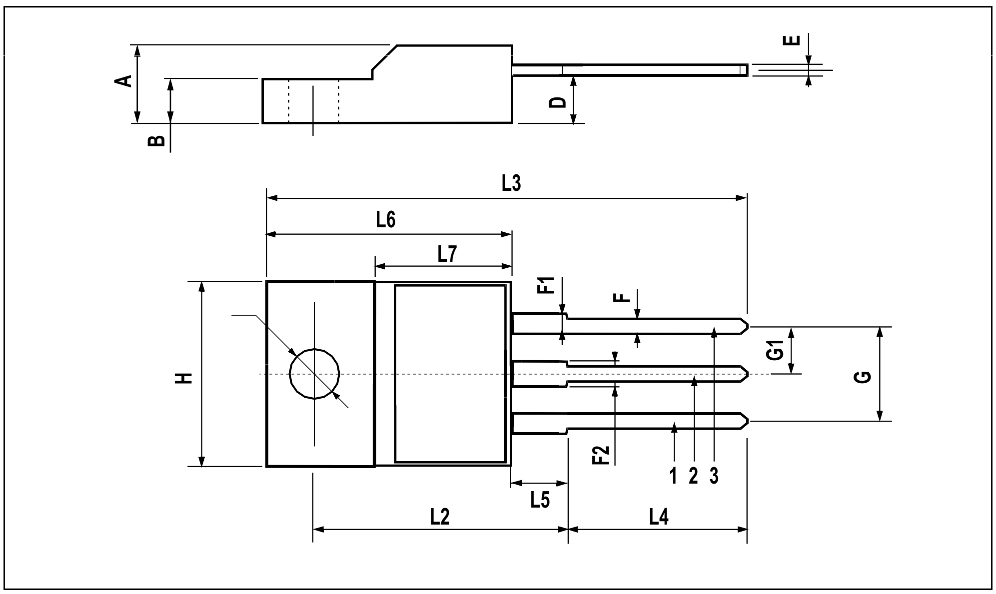
TO-220 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
∅P	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



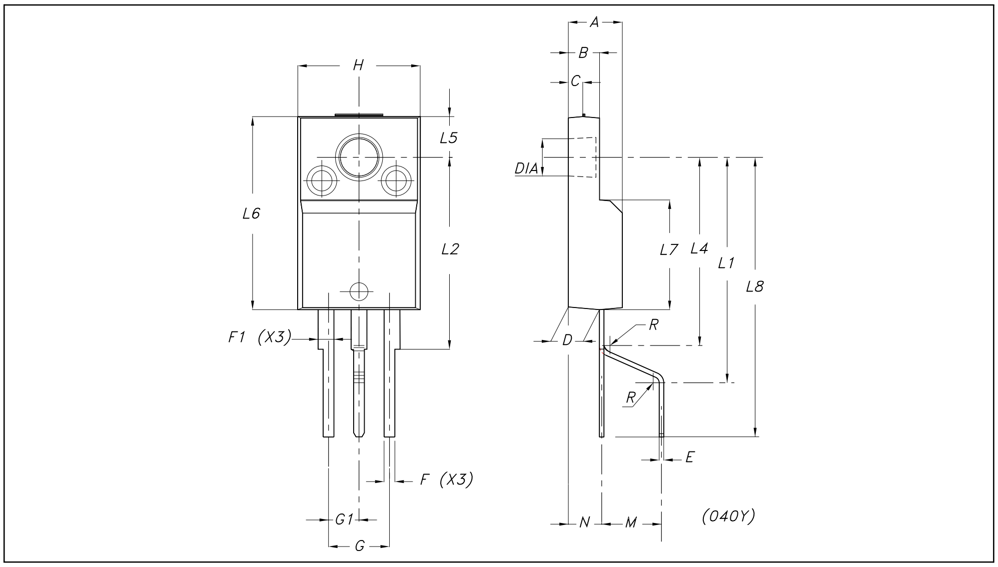
TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



TO-220FP(040Y) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.009		0.106
C	1		1.4	0.039		0.055
D	2.4		2.75	0.094		0.108
E	0.4		0.7	0.015		0.027
F	0.75		1	0.029		0.039
F1	1.15		1.7	0.045		0.066
G	4.68		5.48	0.184		0.215
G1	2.24		2.84	0.088		0.111
H	10		10.4	0.393		0.409
L1	18.4		19.2	0.724		0.755
L2		16			0.629	
L4	15.3		16.1	0.602		0.633
L5		3.4			0.133	
L6	15.9		16.4	0.625		0.665
L7	9		9.3	0.354		0.366
L8	22.5		23.6	0.885		0.929
M	4.6		5.4	0.181		0.212
N	2.29		3.29	0.090		0.129
Dia	3		3.2			
R	0.5			0.019		



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
11-Sep-2006	2	Complete version
19-Dec-2007	3	The document has been reformatted

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