



STS15N4LLF5

N-channel 40 V, 0.00625 Ω , 15 A, SO-8
STripFET™ Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)} max.	I _D
STS15N4LLF5	40 V	< 0.0076 Ω	15 A

- Optimal R_{DS(on)} × Q_g trade-off @ 4.5 V
- Conduction losses reduced
- Switching losses reduced

Applications

- Switching application

Description

This STripFET™ Power MOSFET technology is among the latest improvements, which have been especially tailored to achieve very low on-state resistance providing also one of the best-in-class figure of merit (FOM).

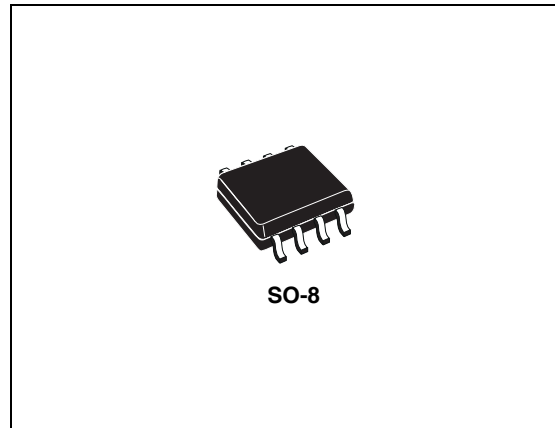


Figure 1. Internal schematic diagram

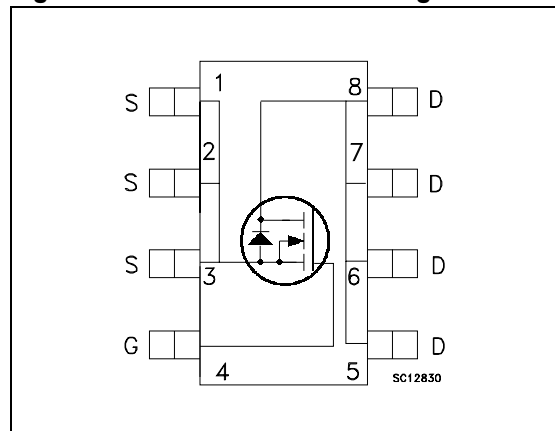


Table 1. Device summary

Order code	Marking	Package	Packaging
STS15N4LLF5	15C4L	SO-8	Tape and reel

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves)	6
3	Test circuits	8
4	Package mechanical data	9
5	Revision history	11

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	40	V
V_{GS}	Gate-source voltage	± 16	V
$V_{GS}^{(1)}$	Gate- source voltage	± 18	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	15	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	10	A
$I_{DM}^{(2)}$	Drain current (pulsed)	63.6	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	3	W
$E_{AS}^{(3)}$	Single pulse avalanche energy	1090	mJ

1. Guaranteed for test time $\leq 15\text{ms}$
2. Pulse width limited by T_{jmax}
3. Starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = 7.5\text{ A}$, $V_{DD} = 25\text{ V}$

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	47	$^\circ\text{C/W}$
T_l	Maximum lead temperature for soldering	-55 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature	-55 to 150	$^\circ\text{C}$

1. When mounted of FR-4 board with 1 inch² pad, 2oz of Cu and $t < 10\text{ sec}$

2 Electrical characteristics

($T_J = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0$	40			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{max rating}$, $V_{DS} = \text{max rating @ } 125^\circ\text{C}$			10 100	μA μA
I_{GSS}	Gate body leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 16\text{ V}$			± 200	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 7.5\text{ A}$ $V_{GS} = 4.5\text{ V}$, $I_D = 7.5\text{ A}$		0.00625 0.0076	0.0067 0.0083	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	1570	-	pF
C_{oss}	Output capacitance			257		pF
C_{rss}	Reverse transfer capacitance			32		pF
Q_g	Total gate charge	$V_{DD} = 15\text{ V}$, $I_D = 18\text{ A}$	-	12.9	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 4.5\text{ V}$		3.9		nC
Q_{gd}	Gate-drain charge	(see Figure 14)		5.3		nC
R_G	Gate input resistance	$f = 1\text{ MHz}$ Gate DC Bias = 0 Test signal level = 20 mV open drain	-	1.5	-	Ω

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}$, $I_D = 9\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 16)	-	14	-	ns
t_r	Rise time			42		ns
$t_{d(off)}$	Turn-off delay time	(see Figure 16)	-	37	-	ns
t_f	Fall time			5.2		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		18	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		72	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 18 \text{ A}, V_{GS} = 0$	-		1.2	V
t_{rr}	Reverse recovery time	$I_{SD} = 18 \text{ A}, V_{DD} = 25 \text{ V},$ $di/dt = 100 \text{ A}/\mu\text{s},$ $T_j = 150 \text{ }^\circ\text{C}$ <i>(see Figure 15)</i>	-	27.2		ns
Q_{rr}	Reverse recovery charge		-	24.5		nC
I_{RRM}	Reverse recovery current		-	1.8		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

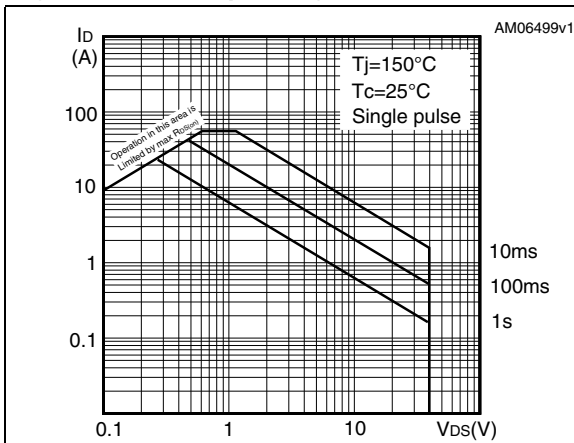


Figure 3. Thermal impedance

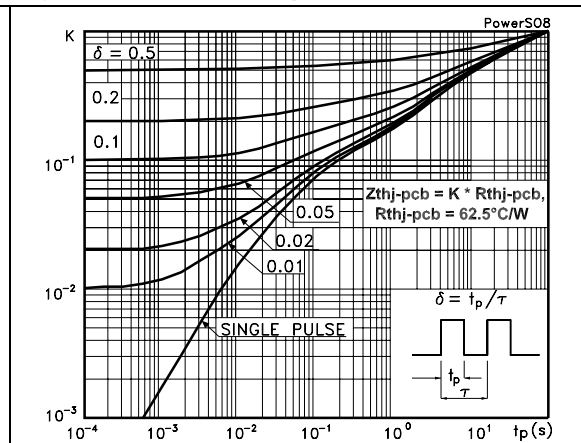


Figure 4. Output characteristics

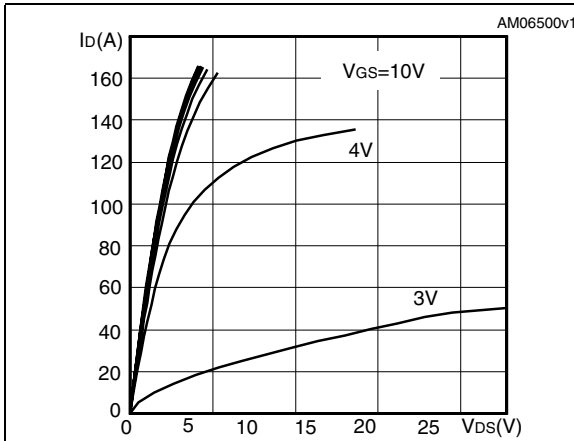


Figure 5. Transfer characteristics

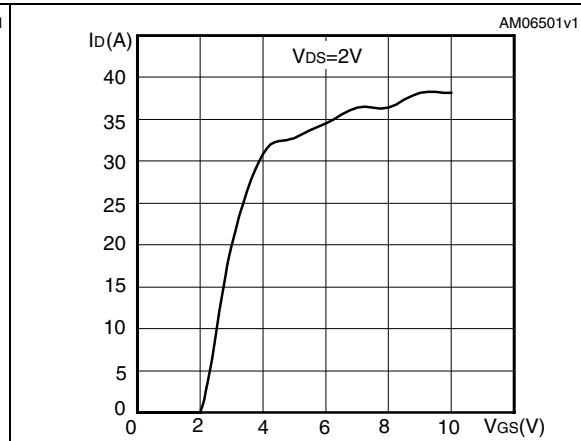


Figure 6. Normalized B_{VDS} vs temperature

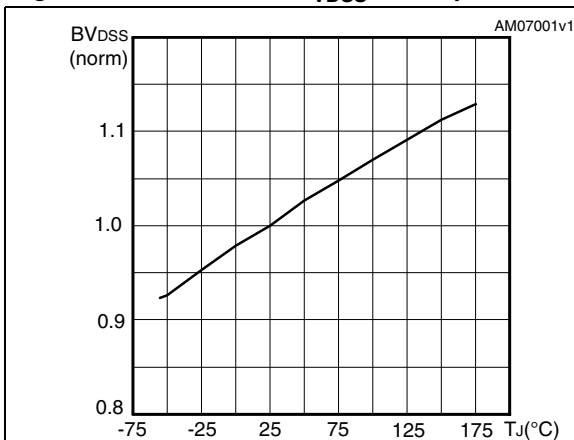


Figure 7. Static drain-source on resistance

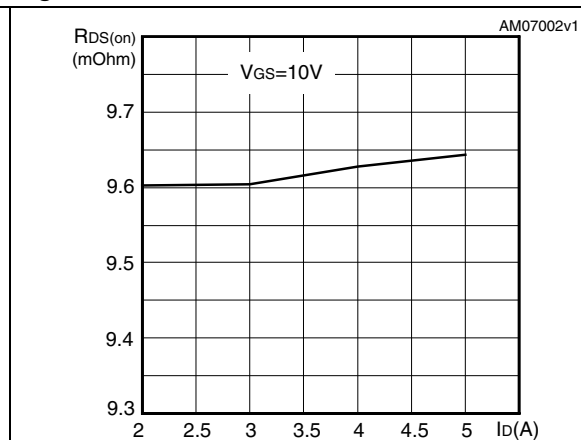


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

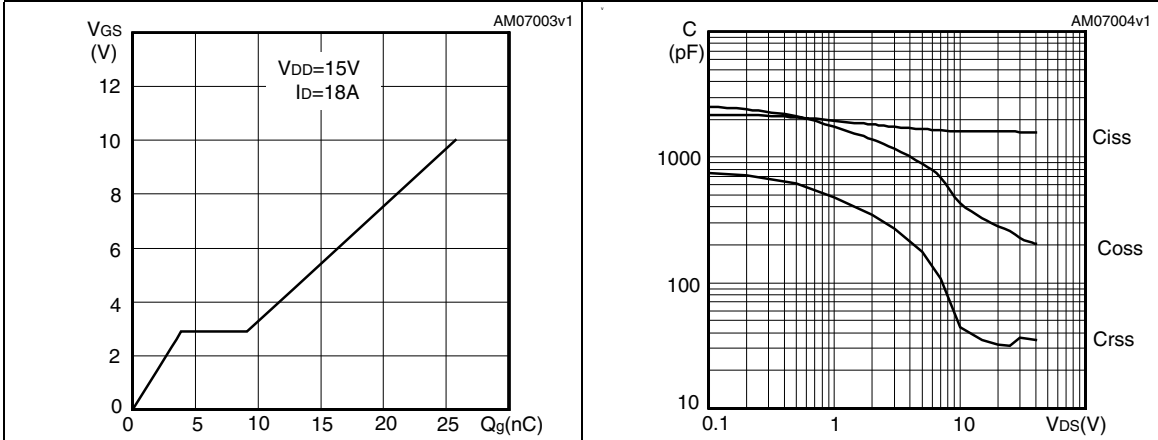


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

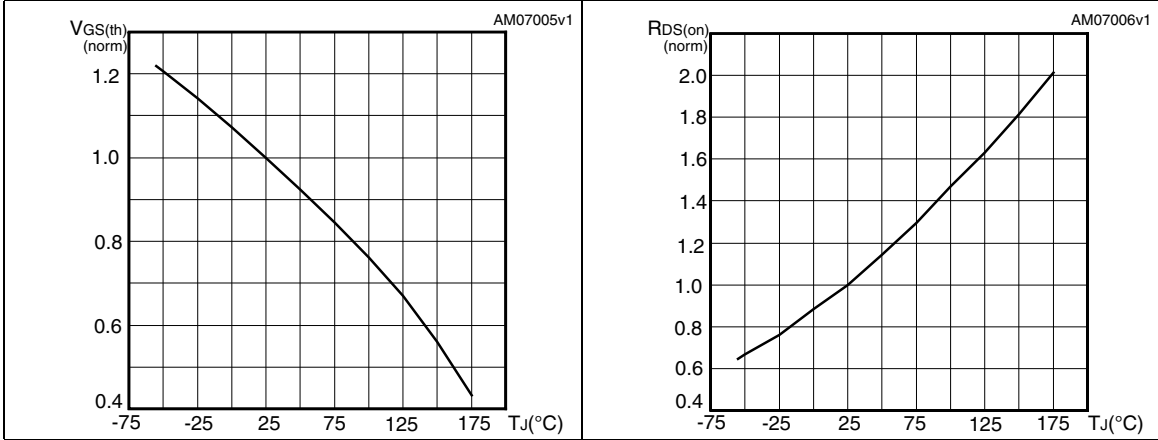
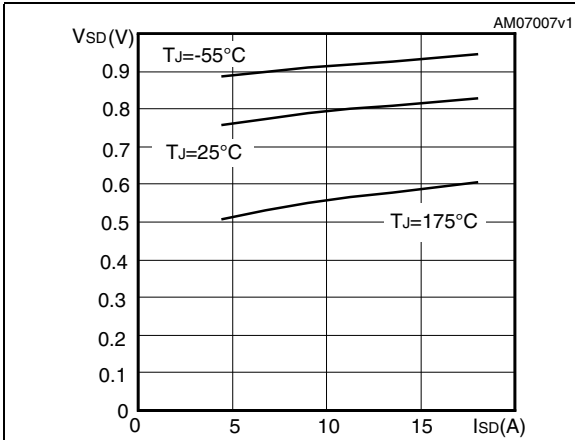


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

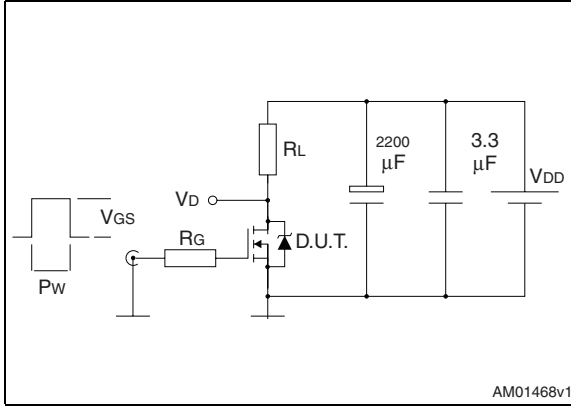


Figure 14. Gate charge test circuit

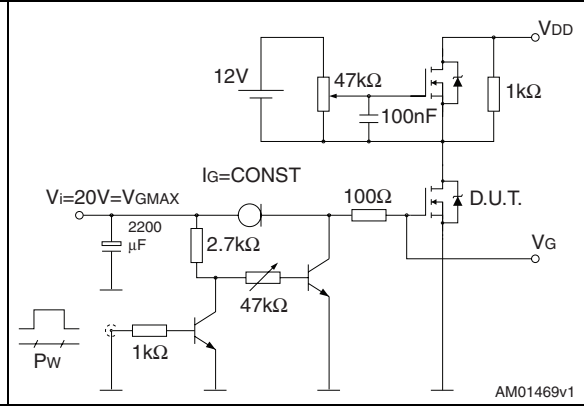


Figure 15. Test circuit for inductive load switching and diode recovery times

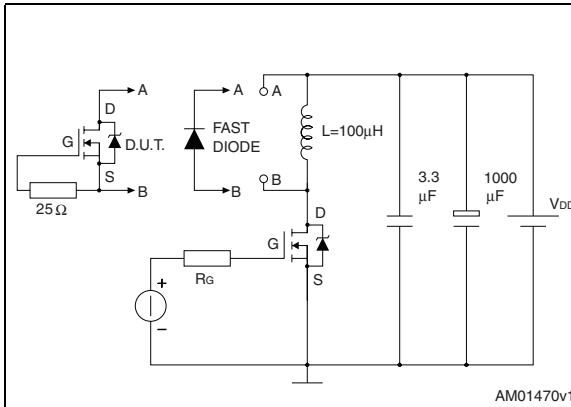


Figure 16. Unclamped inductive load test circuit

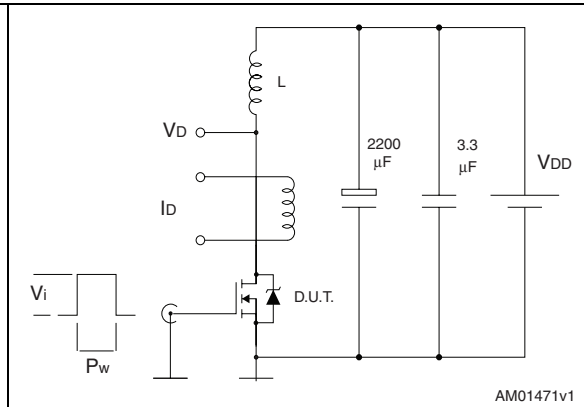


Figure 17. Unclamped inductive waveform

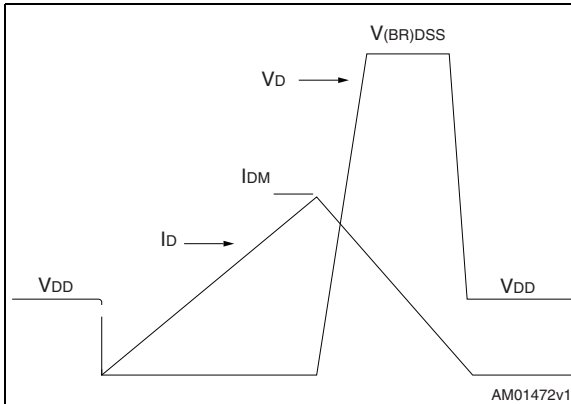
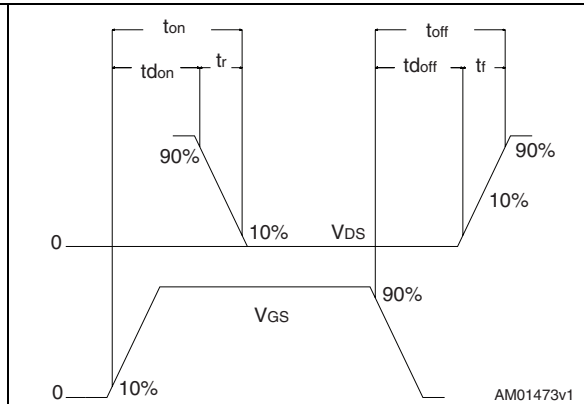


Figure 18. Switching time waveform



4 Package mechanical data

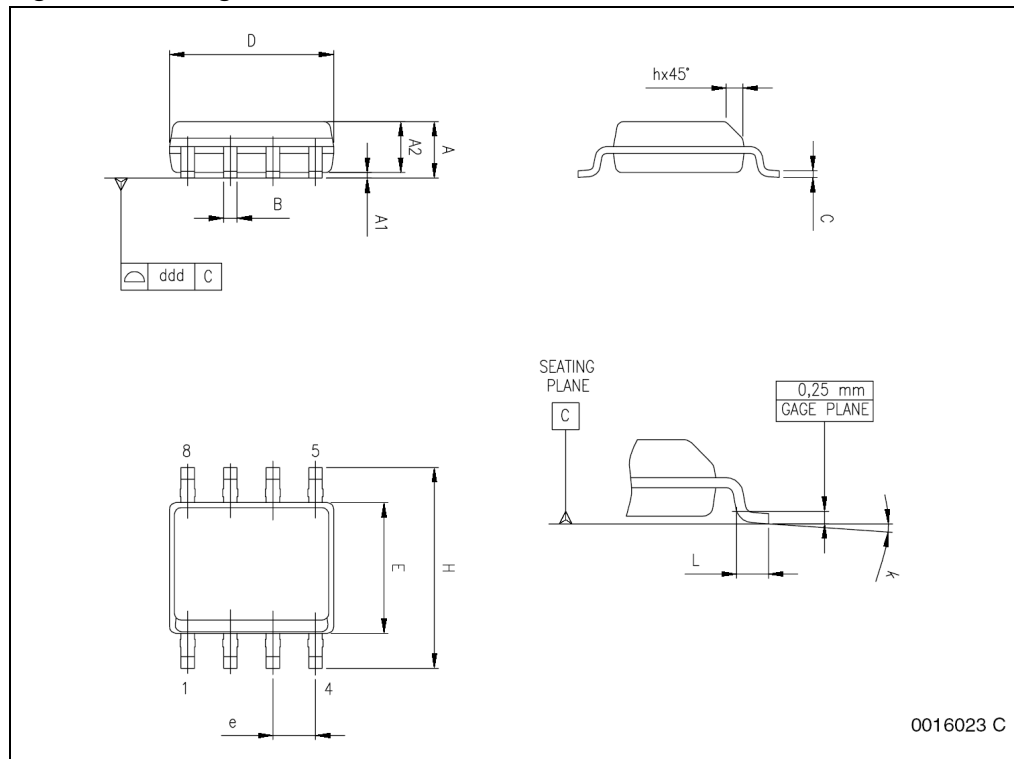
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Table 1. SO-8 mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D ⁽¹⁾	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm (.006inch) in total (both side).

Figure 19. Package dimensions



5 Revision history

Table 8. Revision history

Date	Revision	Changes
07-Apr-2010	1	First release

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