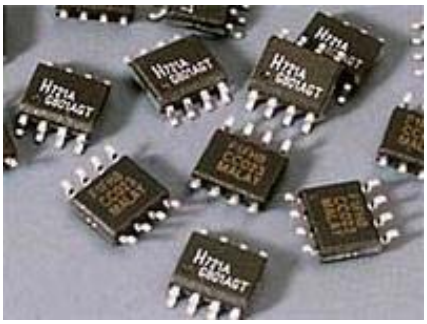

Part Number: **SP721APP**

Technology: **Silicon Protection Arrays**

Series: **SP721 Lead-Free/Green**

SP721 Lead-Free/Green Series - SCR/Diode Array for ESD and Overvoltage Protection

The SP721 is an array of SCR/Diode bipolar structures for ESD and over-voltage protection to sensitive input circuits. The SP721 has 2 protection SCR/Diode structures per input. There are a total of 6 available inputs that can be used to protect up to 6 external signal or bus lines. Over voltage protection is from the IN (Pins 1-3 and Pins 5-7) to V+ or V-.

The SCR structures are designed for fast triggering at a threshold of one +VBE diode threshold above V+ (Pin 8) or a –VBE diode threshold below V- (Pin 4). From an IN input, a clamp to V+ is activated if a transient pulse causes the input to be increased to a voltage level greater than one VBE above V+. A similar clamp to V- is activated if a negative pulse, one VBE less than V-, is applied to an IN input.
Read More

Electrical Characteristics

Property	Value
IEC 61000-4-2	15
IEC-61000-2	8
MIL-STD-883	15
Pkg Size	PDIP
Channels	6
Polarity	Bipolar
V_R	35
V_{BUS} (max)	35
I - leakage	0.02
I_S	0.2
C_{TYP} (pF)	3

RoHS Pb GREEN SP721Lead-Free/Green

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The SCR structures are designed for fast triggering at a threshold of one $+V_{BE}$ diode threshold above V+ (Pin 8) or a $-V_{BE}$ diode threshold below V- (Pin 4). From an IN input, a clamp to V+ is activated if a transient pulse causes the input to be increased to a voltage level greater than one V_{BE} above V+. A similar clamp to V- is activated if a negative pulse, one V_{BE} less than V-, is applied to an IN input. Standard ESD Human Body Model (HBM) Capability is:

HBM STANDARD	MODE	R	C	ESD (V)
IEC 61000-4-2	Air	330Ω	150pF	>15kV
	Direct	330Ω	150pF	>4kV
	Direct, Dual Pins	330Ω	150pF	>8kV
MIL-STD-3015.7	Direct, In-Circuit	1.5kΩ	100pF	>15kV

Refer to Figure 1 and Table 1 for further detail. Refer to Application Notes AN9304 and AN9612 for additional information.

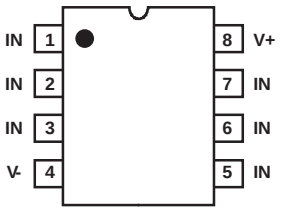
Ordering Information

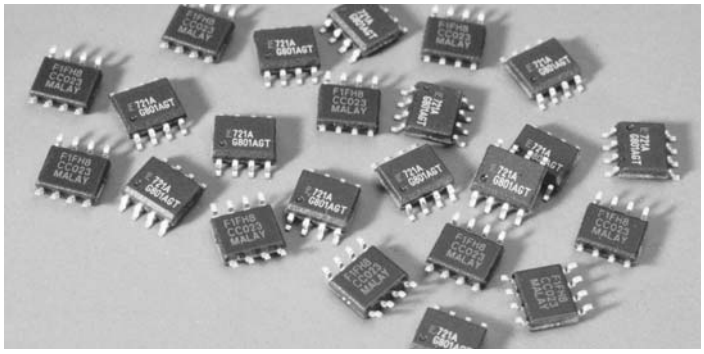
PART NO.	TEMP. RANGE (°C)	PACKAGE	ENVIRONMENTAL INFORMATON	MARKING	Min. Order
SP721APP	-40 to 105	8 Ld PDIP	Lead-free	721APP	2000
SP721ABG	-40 to 105	8 Ld SOIC	Green	721AG	1960
SP721ABTG	-40 to 105	8 Ld SOIC Tape and Reel	Green	721AG	2500

Pinout

SP721 (PDIP, SOIC)

TOP VIEW





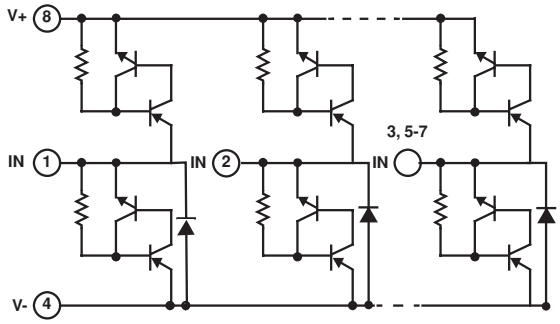
Features

- ESD Interface Capability for HBM Standards
  - MIL STD 3015.7 . . . . . 15kV
  - IEC 61000-4-2, Direct Discharge,
  - Single Input. . . . . 4kV (Level 2)
  - Two Inputs in Parallel . . . . . 8kV (Level 4)
  - IEC 61000-4-2, Air Discharge . . . . . 15kV (Level 4)
- High Peak Current Capability
  - IEC 61000-4-5 (8/20µs). . . . . ±3A
  - Single Pulse, 100µs Pulse Width . . . . . ±2A
  - Single Pulse, 4µs Pulse Width . . . . . ±5A
- Designed to Provide Over-Voltage Protection
  - Single-Ended Voltage Range to . . . . . +30V
  - Differential Voltage Range to. . . . . ±15V
- Fast Switching . . . . . 2ns Rise Time
- Low Input Leakages . . . . . 1nA at 25°C Typical
- Low Input Capacitance. . . . . 3pF Typical
- An Array of 6 SCR/Diode Pairs
- Operating Temperature Range . . . . . -40°C to 105°C

Applications

- Microprocessor/Logic Input Protection
- Data Bus Protection
- Analog Device Input Protection
- Voltage Clamp

Functional Block Diagram



RoHS Pb GREEN SP721 Lead-Free/Green

Absolute Maximum Ratings

Continuous Supply Voltage, (V+) - (V-). . . . . +35V
Forward Peak Current, I_{IN} to V_{CC} , I_{IN} to GND
(Refer to Figure 6). . . . . ±2A, 100µs
ESD Ratings and Capability (Figure 1, Table 1)
Load Dump and Reverse Battery (Note 2)

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
PDIP Package 160
SOIC Package 170
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Lead Temperature (Soldering 10s). . . . . .300°C
(SOIC Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:
1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

T A = -40°C to 105°C, V_{IN} = 0.5V_{CC} , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range, V_{SUPPLY} = [(V+) - (V-)]	V_{SUPPLY}		-	2 to 30	-	V
Forward Voltage Drop IN to V- IN to V+	 V_{FWDL} V_{FWDH}	 I_{IN} = 1A (Peak Pulse)	 - -	 2 2	 - -	 V V
Input Leakage Current	I_{IN}		-20	5	+20	nA
Quiescent Supply Current	$I_{QUIESCENT}$		-	50	200	nA
Equivalent SCR ON Threshold		Note 3	-	1.1	-	V
Equivalent SCR ON Resistance		V_{FWD}/I_{FWD}; Note 3	-	1	-	Ω
Input Capacitance	C_{IN}		-	3	-	pF
Input Switching Speed	t_{ON}		-	2	-	ns

NOTES:
2. In automotive and battery operated systems, the power supply lines should be externally protected for load dump and reverse battery. When the V+ and V- Pins are connected to the same supply voltage source as the device or control line under protection, a current limiting resistor should be connected in series between the external supply and the SP721 supply pins to limit reverse battery current to within the rated maximum limits. Bypass capacitors of typically 0.01µF or larger from the V+ and V- Pins to ground are recommended.
3. Refer to the Figure 3 graph for definitions of equivalent "SCR ON Threshold" and "SCR ON Resistance". These characteristics are given here for thumb-rule information to determine peak current and dissipation under EOS conditions.

ESD Capability

ESD capability is dependent on the application and defined test standard.The evaluation results for various test standards and methods based on Figure 1 are shown in Table 1.

For the "Modified" MIL-STD-3015.7 condition that is defined as an "in-circuit" method of ESD testing, the V+ and V- pins have a return path to ground and the SP721 ESD capability is typically greater than 15kV from 100pF through 1.5kΩ. By strict definition of MIL-STD-3015.7 using "pin-to-pin" device testing, the ESD voltage capability is greater than 6kV. The MIL-STD-3015.7 results were determined from AT&T ESD Test Lab measurements.

The HBM capability to the IEC 61000-4-2 standard is greater than 15kV for air discharge (Level 4) and greater than 4kV for direct discharge (Level 2). Dual pin capability (2 adjacent pins in parallel) is well in excess of 8kV (Level 4).

For ESD testing of the SP721 to EIAJ IC121 Machine Model (MM) standard, the results are typically better than 1kV from 200pF with no series resistance.

TABLE 1. ESD TEST CONDITIONS

STANDARD	TYPE/MODE	R_D	C_D	$\pm V_D$
MIL-STD-3015.7	Modified HBM	1.5kΩ	100pF	15kV
	Standard HBM	1.5kΩ	100pF	6kV
IEC 61000-4-2	HBM, Air Discharge	330Ω	150pF	15kV
	HBM, Direct Discharge	330Ω	150pF	4kV
	HBM, Direct Discharge, Two Parallel Input Pins	330Ω	150pF	8kV
EIAJ IC121	Machine Model	0kΩ	200pF	1kV

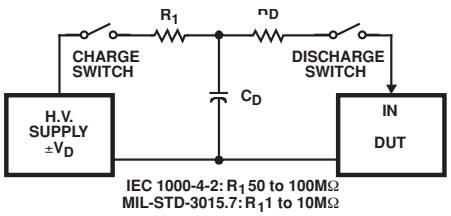
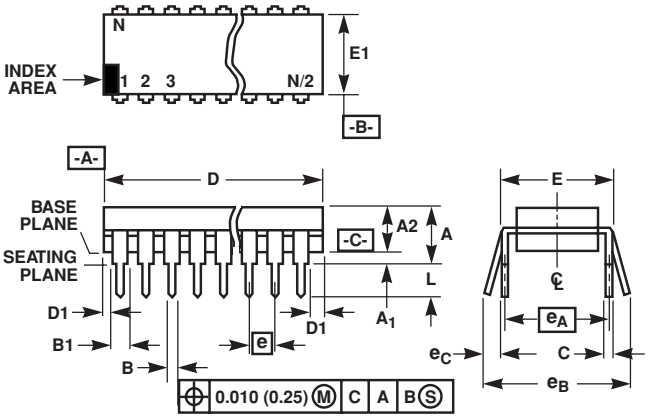


FIGURE 1. ELECTROSTATIC DISCHARGE TEST

RoHS Pb GREEN SP721Lead-Free/Green

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)

8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9