Features

- Industry-standard Architecture
  - Low-cost, Easy-to-use Software Tools
- High-speed, Electrically Erasable Programmable Logic Devices
  - 5 ns Maximum Pin-to-pin Delay
- CMOS- and TTL-compatible Inputs and Outputs
  - Latch Feature Holds Inputs to Previous Logic States
- Pin-controlled Standby Power (10 µA Typical)
- Advanced Flash Technology
  - Reprogrammable
  - 100% Tested
- High-reliability CMOS Process
  - 20-year Data Retention
  - 100 Erase/Write Cycles
  - 2,000V ESD Protection
  - 200 mA Latch-up Immunity
- Dual Inline and Surface Mount Packages in Standard Pinouts
- PCI-compliant
- True Input Transition Detection “Z” and “QZ” Version
- Green Package Options (Pb/Halide-free/RoHS Compliant) Available

1. Description

The ATF22V10C is a high-performance CMOS (electrically erasable) programmable logic device (PLD) that utilizes Atmel’s proven electrically erasable Flash memory technology. Speeds down to 5 ns and power dissipation as low as 100 µA are offered. All speed ranges are specified over the full 5V ± 10% range for industrial temperature ranges, and 5V ± 5% for commercial temperature ranges.

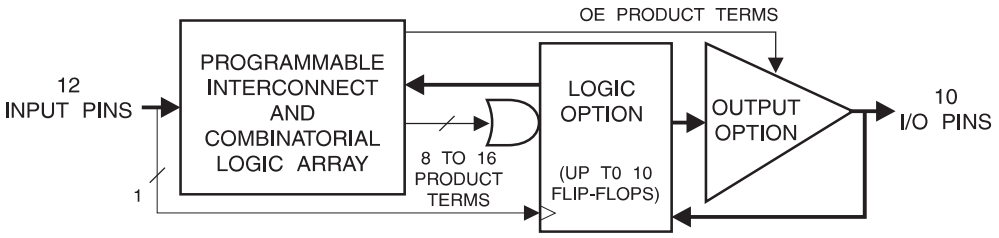
Several low-power options allow selection of the best solution for various types of power-limited applications. Each of these options significantly reduces total system power and enhances system reliability.

High-performance EE PLD

ATF22V10C
ATF22V10CQ

See separate datasheet for ATF22V10CZ and ATF22V10CQZ options.

Figure 1-1. Logic Diagram



2. Pin Configurations

Table 2-1. Pin Configurations (All Pinouts Top View)

Pin Name	Function
CLK	Clock
IN	Logic Inputs
I/O	Bi-directional Buffers
GND	Ground
VCC	+5V Supply
PD	Power-down

Figure 2-1. TSSOP

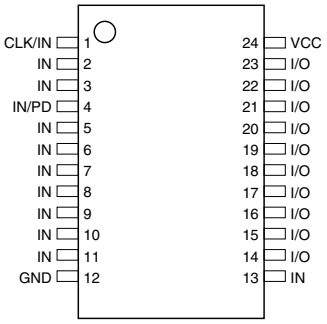


Figure 2-2. DIP/SOIC

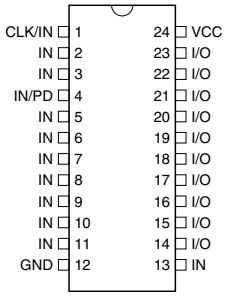
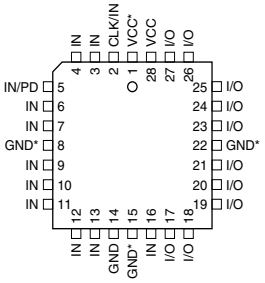


Figure 2-3. PLCC



Note: For all PLCCs (except “-5”), pins 1, 8, 15 and 22 can be left unconnected. However, if they are connected, superior performance will be achieved.

3. Absolute Maximum Ratings*

Temperature under Bias	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on Input Pins with Respect to Ground during Programming	-2.0V to +14.0V(1)
Programming Voltage with Respect to Ground	-2.0V to +14.0V(1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC, which may overshoot to 7.0V for pulses of less than 20 ns.

4. DC and AC Operating Conditions

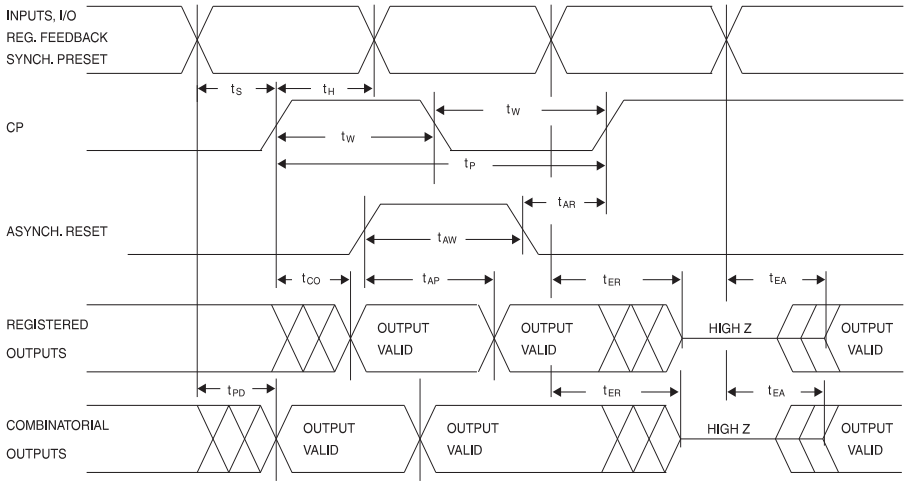
	Commercial	Industrial
Operating Temperature (Ambient)	0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply	5V ± 5%	5V ± 10%

4.1 DC Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{IL}	Input or I/O Low Leakage Current	$0 \le V_{IN} \le V_{IL}$ (Max)				-35.0	-10.0	µA
I_{IH}	Input or I/O High Leakage Current	$3.5 \le V_{IN} \le V_{CC}$					10.0	µA
I_{CC}	Power Supply Current, Standby	V_{CC} = Max, V_{IN} = Max, Outputs Open	C-5, 7, 10	Com.		85.0	130.0	mA
			C-10	Ind.		90.0	140.0	mA
			C-15	Com.		65.0	90.0	mA
			C-15	Ind.		65.0	115.0	mA
			CQ-15	Com.		35.0	55.0	mA
			CQ-15	Ind.		35.0	70.0	mA
I_{CC2}	Clocked Power Supply Current	V_{CC} = Max, Outputs Open, f = 15 MHz	C-5, 7, 10	Com.			150.0	mA
			C-10	Ind.			160.0	mA
			C-15	Com.		70.0	90.0	mA
			C-15	Ind.		70.0	90.0	mA
			CQ-15	Com.		40.0	60.0	mA
			CQ-15	Ind.		40.0	80.0	mA
I_{PD}	Power Supply Current, PD Mode	V_{CC} = Max		Com.		10.0	100.0	µA
		V_{IN} = 0, Max		Ind.		10.0	100.0	µA
I_{OS}[1]	Output Short Circuit Current	V_{OUT} = 0.5V					-130.0	mA
V_{IL}	Input Low Voltage				-0.5		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC}+0.75	V
V_{OL}	Output Low Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min	I_{OL} = 16 mA	Com., Ind.			0.5	V
			I_{OL} = 12 mA	Mil.			0.5	V
V_{OH}	Output High Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min	I_{OH} = -4.0 mA		2.4			V

Note: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.

4.2 AC Waveforms [1]



Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

4.3 AC Characteristics[1]

Symbol	Parameter	-5		-7		-10		-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output	1.0	5.0	3.0	7.5	3.0	10.0	3.0	15.0	ns
t_{CO}	Clock to Output	1.0	4.0	2.0	4.5[2]	2.0	6.5	2.0	8.0	ns
t_{CF}	Clock to Feedback		2.5		2.5		2.5		2.5	ns
t_S	Input or Feedback Setup Time	3.0		3.5		4.5		10.0		ns
t_H	Hold Time	0		0		0		0		ns
f_{MAX}	External Feedback $1/(t_S + t_{CO})$	142.0		125.0[3]		90.0		55.5		MHz
	Internal Feedback $1/(t_S + t_{CF})$	166.0		142.0		117.0		80.0		MHz
	No Feedback $1/(t_{WH} + t_{WL})$	166.0		166.0		125.0		83.3		MHz
t_W	Clock Width (t_{WL} and t_{WH})	3.0		3.0		3.0		6.0		ns
t_{EA}	Input or I/O to Output Enable	2.0	6.0	3.0	7.5	3.0	10.0	3.0	15.0	ns
t_{ER}	Input or I/O to Output Disable	2.0	5.0	3.0	7.5	3.0	9.0	3.0	15.0	ns
t_{AP}	Input or I/O to Asynchronous Reset of Register	3.0	7.0	3.0	10.0	3.0	12.0	3.0	20.0	ns
t_{AW}	Asynchronous Reset Width	5.5		7.0		8.0			15.0	ns
t_{AR}	Asynchronous Reset Recovery Time	4.0		5.0		6.0			10.0	ns
t_{SP}	Setup Time, Synchronous Preset	4.0		4.5		6.0			10.0	ns
t_{SPR}	Synchronous Preset to Clock Recovery Time	4.0		5.0		8.0			10.0	ns

Notes: 1. See ordering information for valid part numbers.
2. 5.5 ns for DIP package devices.
3. 111 MHz for DIP package devices.

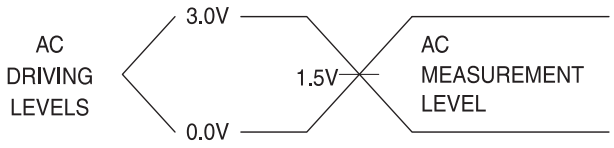
4.4 Power-down AC Characteristics[1][2][3]

Symbol	Parameter	-5		-7		-10		-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{IVDH}	Valid Input before PD High	5.0		7.5		10.0		15.0		ns
t_{GVDH}	Valid $\overline{OE}$ before PD High	0		0		0		0		ns
t_{CVDH}	Valid Clock before PD High	0		0		0				ns
t_{DHIX}	Input Don't Care after PD High		5.0		7.0		10.0		15.0	ns
t_{DHGX}	$\overline{OE}$ Don't Care after PD High		5.0		7.0		10.0		15.0	ns
t_{DHCX}	Clock Don't Care after PD High		5.0		7.0		10.0		15.0	ns
t_{DLIV}	PD Low to Valid Input		5.0		7.5		10.0		15.0	ns
t_{DLGV}	PD Low to Valid $\overline{OE}$		15.0		20.0		25.0		30.0	ns
t_{DLCV}	PD Low to Valid Clock		15.0		20.0		25.0		30.0	ns
t_{DLOV}	PD Low to Valid Output		20.0		25.0		30.0		35.0	ns

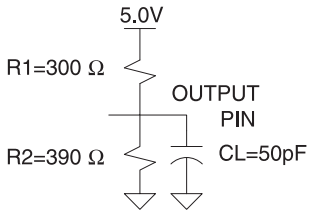
Notes: 1. Output data is latched and held.
2. High-Z outputs remain high-Z.
3. Clock and input transitions are ignored.

4.5 Input Test Waveforms

4.5.1 Input Test Waveforms and Measurement Levels



4.5.2 Commercial Output Test Loads



4.6 Pin Capacitance

Table 4-1. Pin Capacitance (f = 1 MHz, T = 25°C[1])

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0V
C_{OUT}	6	8	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

7. Programming/Erasing

Programming/erasing is performed using standard PLD programmers. See “CMOS PLD Programming Hardware & Software Support” for information on software/programming.

Table 7-1. Programming/Erasing

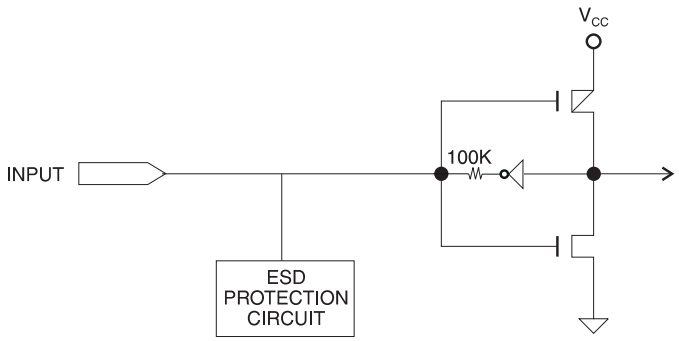
Parameter	Description	Typ	Max	Units
t_{PR}	Power-up Reset Time	600	1,000	ns
V_{RST}	Power-up Reset Voltage	3.8	4.5	V

8. Input and I/O Pin-keeper Circuits

The ATF22V10C contains internal input and I/O pin-keeper circuits. These circuits allow each ATF22V10C pin to hold its previous value even when it is not being driven by an external source or by the device’s output buffer. This helps to ensure that all logic array inputs are at known valid logic levels. This reduces system power by preventing pins from floating to indeterminate levels. By using pin-keeper circuits rather than pull-up resistors, there is no DC current required to hold the pins in either logic state (high or low).

These pin-keeper circuits are implemented as weak feedback inverters, as shown in the Input Diagram below. These keeper circuits can easily be overdriven by standard TTL- or CMOS-compatible drivers. The typical overdrive current required is 40 µA.

Figure 8-1. Input Diagram



12.2 ATF22V10CQ Green Package Options (Pb/Halide-free/RoHS Compliant)

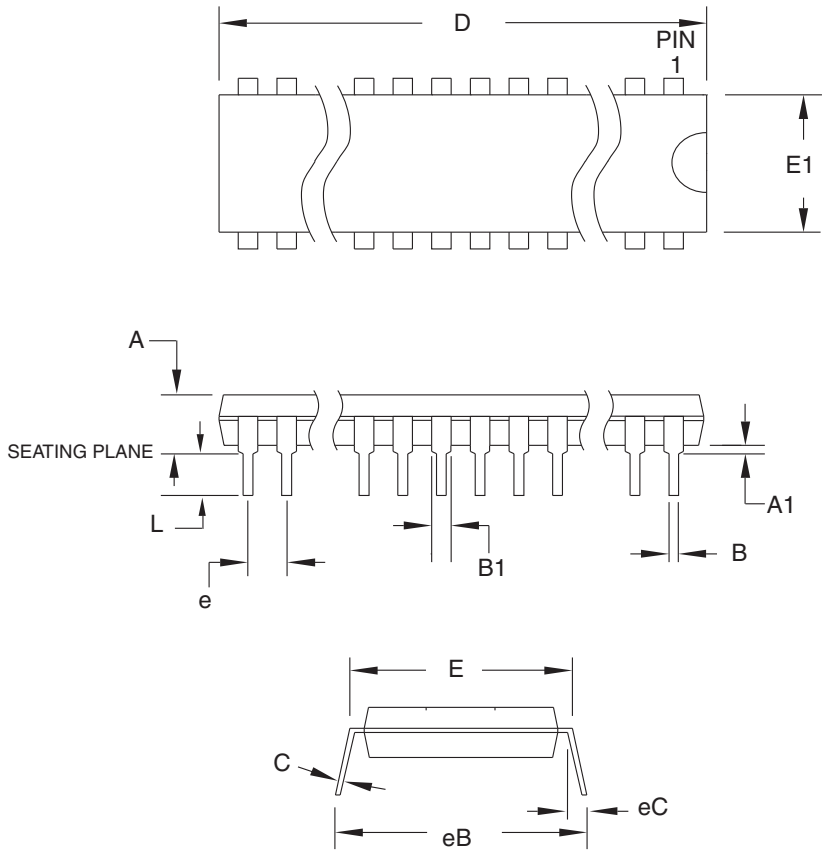
t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
5	3	4	ATF22V10C-5JX	28J	Commercial (0° C to 70° C)
7.5	3.5	4.5	ATF22V10C-7PX ATF22V10C-7SX	24P3 24S	Commercial (0° C to 70° C)
7.5	3.5	4.5	ATF22V10C-7JU	28J	Industrial (-40°C to 85° C)
10	4.5	6.5	ATF22V10C-10JU ATF22V10C-10PU ATF22V10C-10SU ATF22V10C-10XU	28J 24P3 24S 24X	Industrial (-40° C to 85° C)
15	10	8	ATF22V10C-15JU ATF22V10C-15PU	28J 24P3	Industrial (-40° C to 85° C)
			ATF22V10CQ-15JU	28J	Industrial (-40° C to 85° C)

12.3 Using “C” Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the “I” to the “C” device (7 ns “C” = 10 ns “I”) and de-rate power by 30%.

Package Type	
28J	28-lead, Plastic J-leaded Chip Carrier (PLCC)
24P3	24-pin, 0.300" Wide, Plastic Dual Inline Package (PDIP)
24S	24-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
24X	24-lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline (TSSOP)

13.2 24P3 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	5.334	
A1	0.381	–	–	
D	31.623	–	32.131	Note 2
E	7.620	–	8.255	
E1	6.096	–	7.112	Note 2
B	0.356	–	0.559	
B1	1.270	–	1.651	
L	2.921	–	3.810	
C	0.203	–	0.356	
eB	–	–	10.922	
eC	0.000	–	1.524	
e	2.540 TYP			

Notes:
1. This package conforms to JEDEC reference MS-001, Variation AF.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

	TITLE	DRAWING NO.
	24P3, 24-lead (0.300"/7.62 mm Wide) Plastic Dual Inline Package (PDIP)	24P3