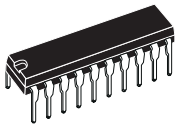
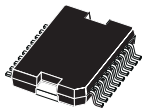
L6205

DMOS DUAL FULL BRIDGE DRIVER

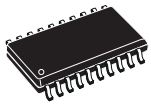
- OPERATING SUPPLY VOLTAGE FROM 8 TO 52V
- 5.6A OUTPUT PEAK CURRENT (2.8A DC)
- $R_{DS(ON)}$ 0.3Ω TYP. VALUE @ T_j = 25 °C
- OPERATING FREQUENCY UP TO 100KHz
- NON DISSIPATIVE OVERCURRENT PROTECTION
- PARALLELED OPERATION
- CROSS CONDUCTION PROTECTION
- THERMAL SHUTDOWN
- UNDER VOLTAGE LOCKOUT
- INTEGRATED FAST FREE WHEELING DIODES



PowerDIP20 (16+2+2)



PowerSO20



SO20 (16+2+2)

ORDERING NUMBERS:
L6205N (PowerDIP20)
L6205PD (PowerSO20)
L6205D (SO20)

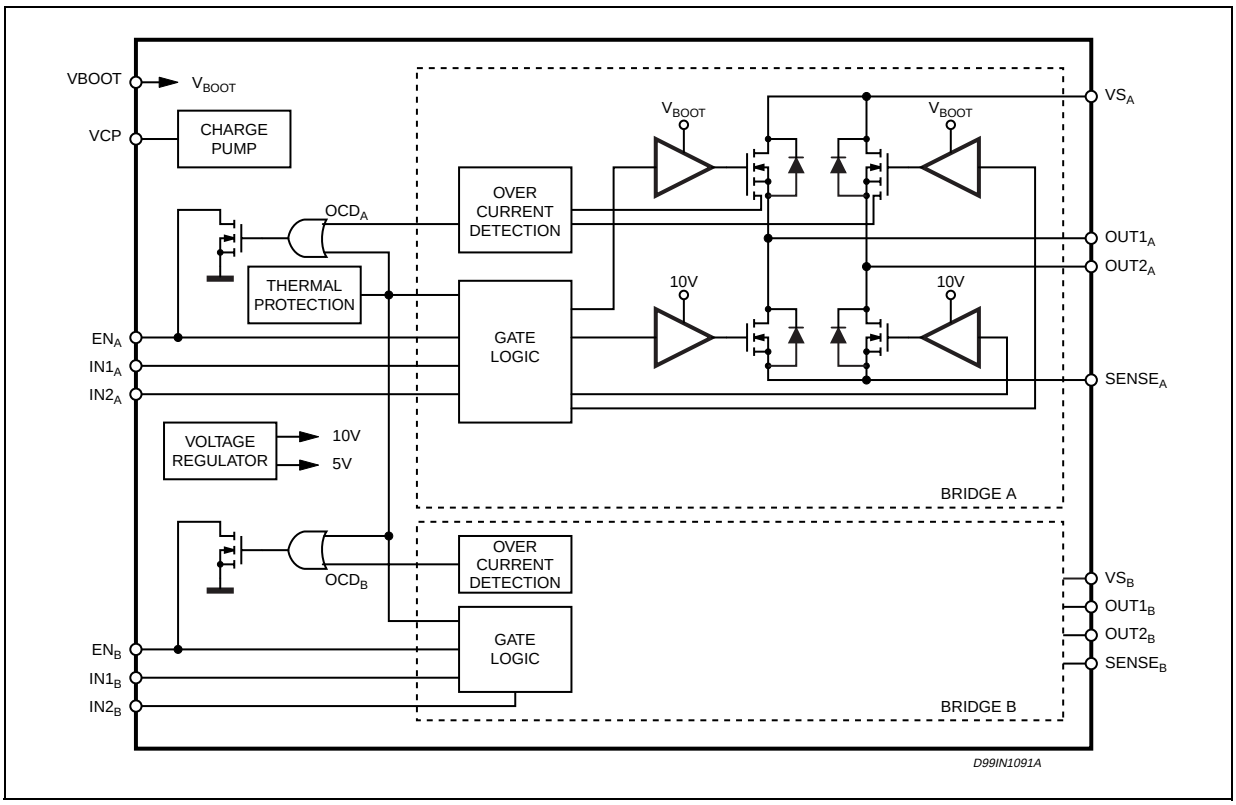
TYPICAL APPLICATIONS

- BIPOLAR STEPPER MOTOR
- DUAL OR QUAD DC MOTOR

DESCRIPTION

The L6205 is a DMOS Dual Full Bridge designed for motor control applications, realized in MultiPower-BCD technology, which combines isolated DMOS Power Transistors with CMOS and bipolar circuits on the same chip. Available in PowerDIP20 (16+2+2), PowerSO20 and SO20(16+2+2) packages, the L6205 features a non-dissipative protection of the high side PowerMOSFETs and thermal shutdown.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test conditions	Value	Unit
V_S	Supply Voltage	$V_{SA} = V_{SB} = V_S$	60	V
V_{OD}	Differential Voltage between VS_A, $OUT1_A$, $OUT2_A$, $SENSE_A$ and VS_B, $OUT1_B$, $OUT2_B$, $SENSE_B$	$V_{SA} = V_{SB} = V_S = 60V$; $V_{SENSEA} = V_{SENSEB} = GND$	60	V
V_{BOOT}	Bootstrap Peak Voltage	$V_{SA} = V_{SB} = V_S$	$V_S + 10$	V
V_{IN},V_{EN}	Input and Enable Voltage Range		-0.3 to +7	V
V_{SENSEA}, V_{SENSEB}	Voltage Range at pins $SENSE_A$ and $SENSE_B$		-1 to +4	V
$I_{S(peak)}$	Pulsed Supply Current (for each V_S pin), internally limited by the overcurrent protection	$V_{SA} = V_{SB} = V_S$; $t_{PULSE} < 1ms$	7.1	A
I_S	RMS Supply Current (for each V_S pin)	$V_{SA} = V_{SB} = V_S$	2.8	A
T_{stg}, T_{OP}	Storage and Operating Temperature Range		-40 to 150	°C

RECOMMENDED OPERATING CONDITIONS

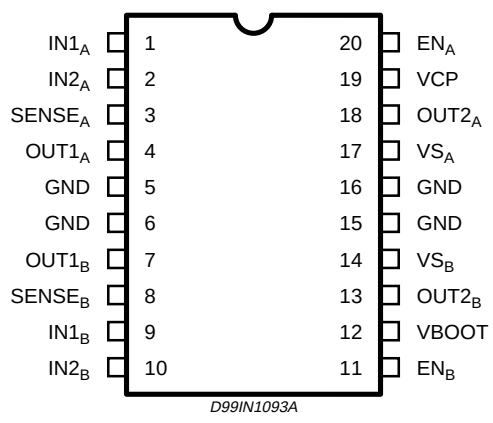
Symbol	Parameter	Test Conditions	MIN	MAX	Unit
V_S	Supply Voltage	$V_{SA} = V_{SB} = V_S$	8	52	V
V_{OD}	Differential Voltage Between VS_A, $OUT1_A$, $OUT2_A$, $SENSE_A$ and VS_B, $OUT1_B$, $OUT2_B$, $SENSE_B$	$V_{SA} = V_{SB} = V_S$; $V_{SENSEA} = V_{SENSEB}$		52	V
V_{SENSEA}, V_{SENSEB}	Voltage Range at pins $SENSE_A$ and $SENSE_B$	(pulsed $t_W < t_{rr}$) (DC)	-6 -1	6 1	V V
I_{OUT}	RMS Output Current			2.8	A
T_j	Operating Junction Temperature		-25	+125	°C
f_{sw}	Switching Frequency			100	KHz

THERMAL DATA

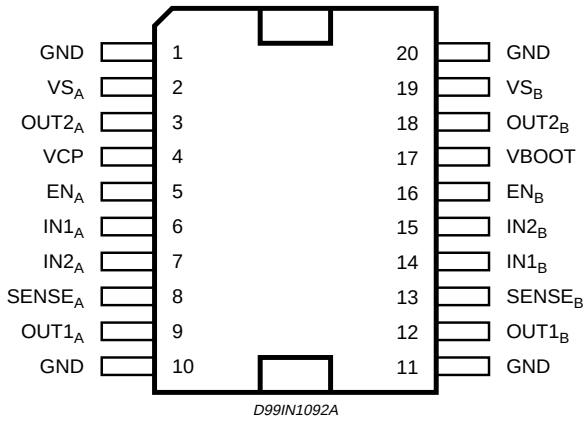
Symbol	Description	PowerDIP20	SO20	PowerSO20	Unit
$R_{th\text{-}j\text{-}pins}$	MaximumThermal Resistance Junction-Pins	12	14	-	°C/W
$R_{th\text{-}j\text{-}case}$	Maximum Thermal Resistance Junction-Case	-	-	1	°C/W
$R_{th\text{-}j\text{-}amb1}$	MaximumThermal Resistance Junction-Ambient [1]	40	51	-	°C/W
$R_{th\text{-}j\text{-}amb1}$	Maximum Thermal Resistance Junction-Ambient [2]	-	-	35	°C/W
$R_{th\text{-}j\text{-}amb1}$	MaximumThermal Resistance Junction-Ambient [3]	-	-	15	°C/W
$R_{th\text{-}j\text{-}amb2}$	Maximum Thermal Resistance Junction-Ambient [4]	56	77	62	°C/W

(1) Mounted on a multi-layer FR4 PCB with a dissipating copper surface on the bottom side of 6cm^2 (with a thickness of 35µm).
(2) Mounted on a multi-layer FR4 PCB with a dissipating copper surface on the top side of 6cm^2 (with a thickness of 35µm).
(3) Mounted on a multi-layer FR4 PCB with a dissipating copper surface on the top side of 6cm^2 (with a thickness of 35µm), 16 via holes and a ground layer.
(4) Mounted on a multi-layer FR4 PCB without any heat sinking surface on the board.

PIN CONNECTIONS (Top View)



PowerDIP20/SO20



PowerSO20 (5)

(5) The slug is internally connected to pins 1,10,11 and 20 (GND pins).

PIN DESCRIPTION

PACKAGE		Name	Type	Function
SO20/ PowerDIP20	PowerSO20			
PIN #	PIN #			
1	6	$IN1_A$	Logic Input	Bridge A Logic Input 1.
2	7	$IN2_A$	Logic Input	Bridge A Logic Input 2.
3	8	$SENSE_A$	Power Supply	Bridge A Source Pin. This pin must be connected to Power Ground directly or through a sensing power resistor.
4	9	$OUT1_A$	Power Output	Bridge A Output 1.
5, 6, 15, 16	1, 10, 11, 20	GND	GND	Signal Ground terminals. In PowerDIP and SO packages, these pins are also used for heat dissipation toward the PCB.
7	12	$OUT1_B$	Power Output	Bridge B Output 1.
8	13	$SENSE_B$	Power Supply	Bridge B Source Pin. This pin must be connected to Power Ground directly or through a sensing power resistor.
9	14	$IN1_B$	Logic Input	Bridge B Logic Input 1.
10	15	$IN2_B$	Logic Input	Bridge B Logic Input 2.
11	16	EN_B	Logic Input (6)	Bridge B Enable. LOW logic level switches OFF all Power MOSFETs of Bridge B. This pin is also connected to the collector of the Overcurrent and Thermal Protection transistor to implement over current protection. If not used, it has to be connected to +5V through a resistor.
12	17	VBOOT	Supply Voltage	Bootstrap Voltage needed for driving the upper PowerMOSFETs of both Bridge A and Bridge B.
13	18	$OUT2_B$	Power Output	Bridge B Output 2.
14	19	VS_B	Power Supply	Bridge B Power Supply Voltage. It must be connected to the supply voltage together with pin VS_A.
17	2	VS_A	Power Supply	Bridge A Power Supply Voltage. It must be connected to the supply voltage together with pin VS_B.
18	3	$OUT2_A$	Power Output	Bridge A Output 2.
19	4	VCP	Output	Charge Pump Oscillator Output.
20	5	EN_A	Logic Input (6)	Bridge A Enable. LOW logic level switches OFF all Power MOSFETs of Bridge A. This pin is also connected to the collector of the Overcurrent and Thermal Protection transistor to implement over current protection. If not used, it has to be connected to +5V through a resistor.

(6) Also connected at the output drain of the Overcurrent and Thermal protection MOSFET. Therefore, it has to be driven putting in series a resistor with a value in the range of 2.2kΩ - 180KΩ, recommended 100kΩ

ELECTRICAL CHARACTERISTICS

(T_{amb} = 25 °C, V_S = 48V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{Sth(ON)}$	Turn-on Threshold		6.6	7	7.4	V
$V_{Sth(OFF)}$	Turn-off Threshold		5.6	6	6.4	V
I_S	Quiescent Supply Current	All Bridges OFF; T_j = -25°C to 125°C (7)		5	10	mA
$T_{j(OFF)}$	Thermal Shutdown Temperature			165		°C
Output DMOS Transistors						
$R_{DS(ON)}$	High-Side Switch ON Resistance	T_j = 25 °C		0.34	0.4	Ω
		T_j =125 °C (7)		0.53	0.59	Ω
	Low-Side Switch ON Resistance	T_j = 25 °C		0.28	0.34	Ω
		T_j =125 °C (7)		0.47	0.53	Ω
I_{DSS}	Leakage Current	EN = Low; OUT = V_S			2	mA
		EN = Low; OUT = GND	-0.15			mA
Source Drain Diodes						
V_{SD}	Forward ON Voltage	I_{SD} = 2.8A, EN = LOW		1.15	1.3	V
t_{rr}	Reverse Recovery Time	I_f = 2.8A		300		ns
t_{fr}	Forward Recovery Time			200		ns
Logic Input						
V_{IL}	Low level logic input voltage		-0.3		0.8	V
V_{IH}	High level logic input voltage		2		7	V
I_{IL}	Low Level Logic Input Current	GND Logic Input Voltage	-10			µA
I_{IH}	High Level Logic Input Current	7V Logic Input Voltage			10	µA
$V_{th(ON)}$	Turn-on Input Threshold			1.8	2.0	V
$V_{th(OFF)}$	Turn-off Input Threshold		0.8	1.3		V
$V_{th(HYS)}$	Input Threshold Hysteresis		0.25	0.5		V
Switching Characteristics						
$t_{D(on)EN}$	Enable to out turn ON delay time (8)	I_{LOAD} =2.8A, Resistive Load	100	250	400	ns
$t_{D(on)IN}$	Input to out turn ON delay time	I_{LOAD} =2.8A, Resistive Load (dead time included)		1.6		µs
t_{RISE}	Output rise time(8)	I_{LOAD} =2.8A, Resistive Load	40		250	ns
$t_{D(off)EN}$	Enable to out turn OFF delay time (8)	I_{LOAD} =2.8A, Resistive Load	300	550	800	ns

ELECTRICAL CHARACTERISTICS (continued)
(T_{amb} = 25 °C, V_S = 48V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{D(off)IN}$	Input to out turn OFF delay time	I_{LOAD} =2.8A, Resistive Load		600		ns
t_{FALL}	Output Fall Time (8)	I_{LOAD} =2.8A, Resistive Load	40		250	ns
t_{dt}	Dead Time Protection		0.5	1		µs
f_{CP}	Charge pump frequency	-25°C<T_j <125°C		0.6	1	MHz
Over Current Protection						
I_{SOVER}	Input Supply Overcurrent Protection Threshold	T_j = -25°C to 125°C (7)	4	5.6	7.1	A
R_{OPDR}	Open Drain ON Resistance	I = 4mA		40	60	Ω
$t_{OCD(ON)}$	OCD Turn-on Delay Time (9)	I = 4mA; C_{EN} < 100pF		200		ns
$t_{OCD(OFF)}$	OCD Turn-off Delay Time (9)	I = 4mA; C_{EN} < 100pF		100		ns

(7) Tested at 25°C in a restricted range and guaranteed by characterization.
(8) See Fig. 1.
(9) See Fig. 2.

Figure 1. Switching Characteristic Definition