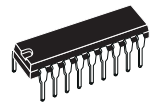
L6201
L6202 - L6203

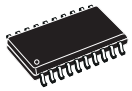
DMOS FULL BRIDGE DRIVER

- SUPPLY VOLTAGE UP TO 48V
- 5A MAX PEAK CURRENT (2A max. for L6201)
- TOTAL RMS CURRENT UP TO L6201: 1A; L6202: 1.5A; L6203/L6201PS: 4A
- $R_{DS\ (ON)}$ 0.3 Ω (typical value at 25 °C)
- CROSS CONDUCTION PROTECTION
- TTL COMPATIBLE DRIVE
- OPERATING FREQUENCY UP TO 100 KHz
- THERMAL SHUTDOWN
- INTERNAL LOGIC SUPPLY
- HIGH EFFICIENCY

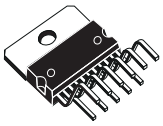
MULTIPOWER BCD TECHNOLOGY



Powerdip 12+3+3



SO20 (12+4+4)



Multiwatt11

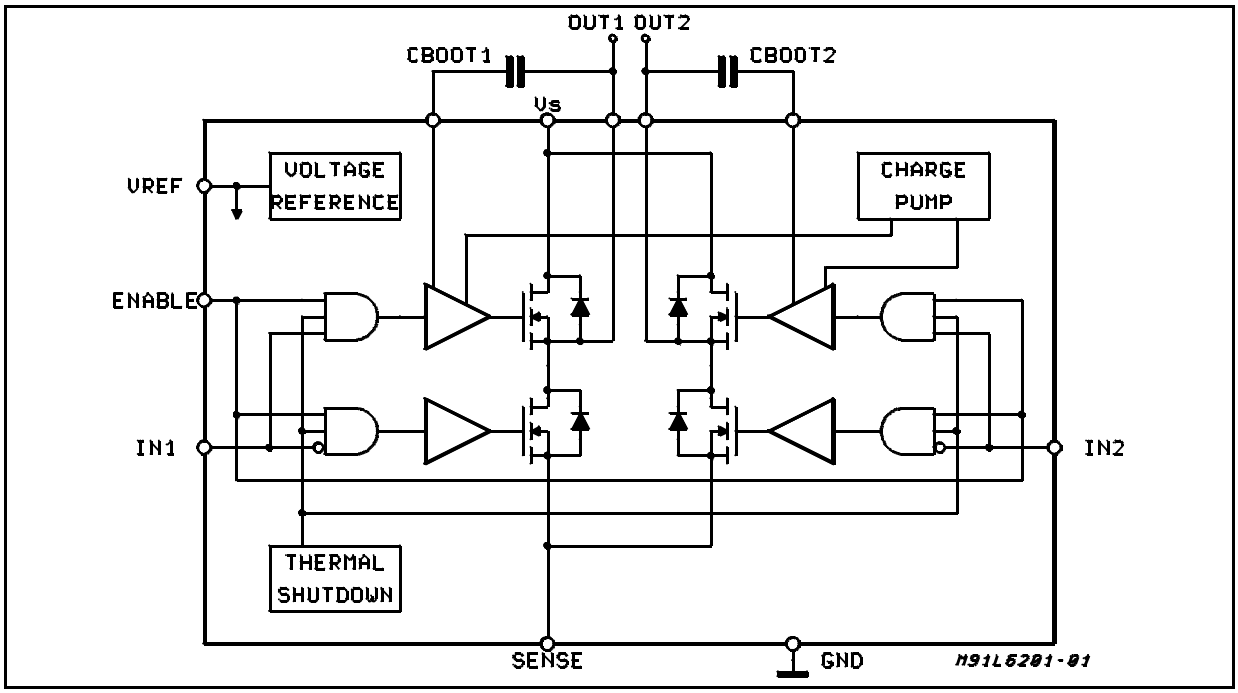
PowerSO20

ORDERING NUMBERS:
L6201 (SO20)
L6201PS (PowerSO20)
L6202 (Powerdip18)
L6203 (Multiwatt)

DESCRIPTION

The I.C. is a full bridge driver for motor control applications realized in Multipower-BCD technology which combines isolated DMOS power transistors with CMOS and Bipolar circuits on the same chip. By using mixed technology it has been possible to optimize the logic circuitry and the power stage to achieve the best possible performance. The DMOS output transistors can operate at supply voltages up to 42V and efficiently at high switching speeds. All the logic inputs are TTL, CMOS and μC compatible. Each channel (half-bridge) of the device is controlled by a separate logic input, while a common enable controls both channels. The I.C. is mounted in three different packages.

BLOCK DIAGRAM



PINS FUNCTIONS

Device				Name	Function
L6201	L6201PS	L6202	L6203		
1	16	1	10	SENSE	A resistor R_{sense} connected to this pin provides feedback for motor current control.
2	17	2	11	ENABLE	When a logic high is present on this pin the DMOS POWER transistors are enabled to be selectively driven by IN1 and IN2.
3	2,3,9,12, 18,19	3		N.C.	Not Connected
4,5	–	4	6	GND	Common Ground Terminal
–	1, 10	5		GND	Common Ground Terminal
6,7	–	6		GND	Common Ground Terminal
8	–	7		N.C.	Not Connected
9	4	8	1	OUT2	Ouput of 2nd Half Bridge
10	5	9	2	V_S	Supply Voltage
11	6	10	3	OUT1	Output of first Half Bridge
12	7	11	4	BOOT1	A boostrap capacitor connected to this pin ensures efficient driving of the upper POWER DMOS transistor.
13	8	12	5	IN1	Digital Input from the Motor Controller
14,15	–	13	6	GND	Common Ground Terminal
–	11, 20	14		GND	Common Ground Terminal
16,17	–	15		GND	Common Ground Terminal
18	13	16	7	IN2	Digital Input from the Motor Controller
19	14	17	8	BOOT2	A boostrap capacitor connected to this pin ensures efficient driving of the upper POWER DMOS transistor.
20	15	18	9	V_{ref}	Internal voltage reference. A capacitor from this pin to GND is recommended. The internal Ref. Voltage can source out a current of 2mA max.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Power Supply	52	V
V_{OD}	Differential Output Voltage (between Out1 and Out2)	60	V
V_{IN}, V_{EN}	Input or Enable Voltage	– 0.3 to + 7	V
I_o	Pulsed Output Current for L6201PS/L6202/L6203 (Note 1) – Non Repetitive (< 1 ms) for L6201 for L6201PS/L6202/L6203 DC Output Current for L6201 (Note 1)	5 5 10 1	A A A A
V_{sense}	Sensing Voltage	– 1 to + 4	V
V_b	Boostrap Peak Voltage	60	V
P_{tot}	Total Power Dissipation: T_{pins} = 90°C for L6201 for L6202 T_{case} = 90°C for L6201PS/L6203 T_{amb} = 70°C for L6201 (Note 2) for L6202 (Note 2) for L6201PS/L6203 (Note 2)	 4 5 20 0.9 1.3 2.3	 W W W W W W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to + 150	°C

Note 1: Pulse width limited only by junction temperature and transient thermal impedance (see thermal characteristics)
Note 2: Mounted on board with minimized dissipating copper area.

THERMAL DATA

Symbol	Parameter		Value				Unit
			L6201	L6201PS	L6202	L6203	
$Rt_{h\ j\text{-}pins}$	Thermal Resistance Junction-pins	max	15	–	12	–	°C/W
$Rt_{h\ j\text{-}case}$	Thermal Resistance Junction Case	max.	–	–	–	3	
$Rt_{h\ j\text{-}amb}$	Thermal Resistance Junction-ambient	max.	85	13 (*)	60	35	

(*) Mounted on aluminium substrate.

ELECTRICAL CHARACTERISTICS (Refer to the Test Circuits; T_j = 25°C, V_S = 42V, V_{sens} = 0, unless otherwise specified).

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		12	36	48	V
V_{ref}	Reference Voltage	I_{REF} = 2mA		13.5		V
I_{REF}	Output Current				2	mA
I_s	Quiescent Supply Current	EN = H V_{IN} = L EN = H V_{IN} = H I_L = 0 EN = L (Fig. 1,2,3)		10 10 8	15 15 15	mA mA mA
f_c	Commutation Frequency (*)			30	100	KHz
T_j	Thermal Shutdown			150		°C
T_d	Dead Time Protection			100		ns

TRANSISTORS

OFF						
I_{DSS}	Leakage Current	Fig. 11 V_s = 52 V			1	mA
ON						
R_{DS}	On Resistance	Fig. 4,5		0.3	0.55	Ω
$V_{DS(ON)}$	Drain Source Voltage	Fig. 9 I_{DS} = 1A **L6201** I_{DS} = 1.2A **L6202** I_{DS} = 3A **L6201PS/03**		 0.3 0.36 0.9		 V V V
V_{sens}	Sensing Voltage		– 1		4	V

SOURCE DRAIN DIODE

V_{sd}	Forward ON Voltage	Fig. 6a and b I_{SD} = 1A **L6201** EN = L I_{SD} = 1.2A **L6202** EN = L I_{SD} = 3A **L6201PS/03** EN = L		 0.9 (**) 0.9 (**) 1.35(**)		 V V V
t_{rr}	Reverse Recovery Time	$\frac{dif}{dt}$ = 25 A/µs I_F = 1A L6201 I_F = 1.2A L6202 I_F = 3A L6203		300		ns
t_{fr}	Forward Recovery Time			200		ns

LOGIC LEVELS

$V_{IN\ L}$, $V_{EN\ L}$	Input Low Voltage		– 0.3		0.8	V
$V_{IN\ H}$, $V_{EN\ H}$	Input High Voltage		2		7	V
$I_{IN\ L}$, $I_{EN\ L}$	Input Low Current	V_{IN}, V_{EN} = L			–10	µA
$I_{IN\ H}$, $I_{EN\ H}$	Input High Current	V_{IN}, V_{EN} = H		30		µA

ELECTRICAL CHARACTERISTICS (Continued)
LOGIC CONTROL TO POWER DRIVE TIMING

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_1 (V_i)	Source Current Turn-off Delay	Fig. 12		300		ns
t_2 (V_i)	Source Current Fall Time	Fig. 12		200		ns
t_3 (V_i)	Source Current Turn-on Delay	Fig. 12		400		ns
t_4 (V_i)	Source Current Rise Time	Fig. 12		200		ns
t_5 (V_i)	Sink Current Turn-off Delay	Fig. 13		300		ns
t_6 (V_i)	Sink Current Fall Time	Fig. 13		200		ns
t_7 (V_i)	Sink Current Turn-on Delay	Fig. 13		400		ns
t_8 (V_i)	Sink Current Rise Time	Fig. 13		200		ns

(*) Limited by power dissipation
(**) In synchronous rectification the drain-source voltage drop VDS is shown in fig. 4 (L6202/03); typical value for the L6201 is of 0.3V.

Figure 1: Typical Normalized I_S vs. T_j

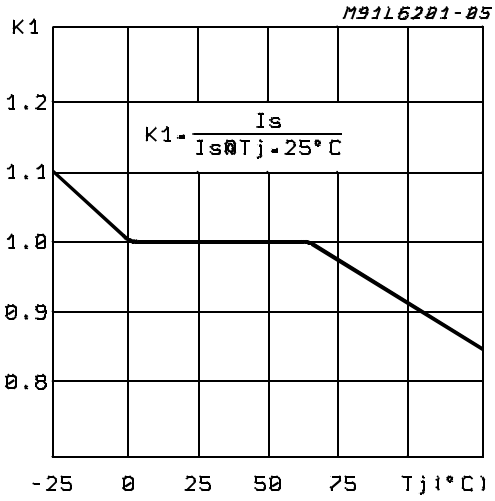


Figure 2: Typical Normalized Quiescent Current vs. Frequency

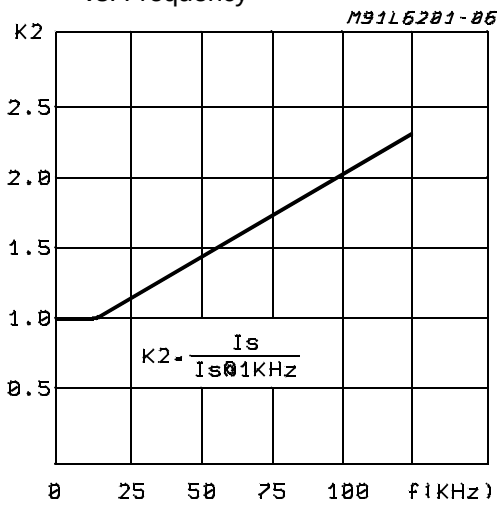


Figure 3: Typical Normalized I_S vs. V_S

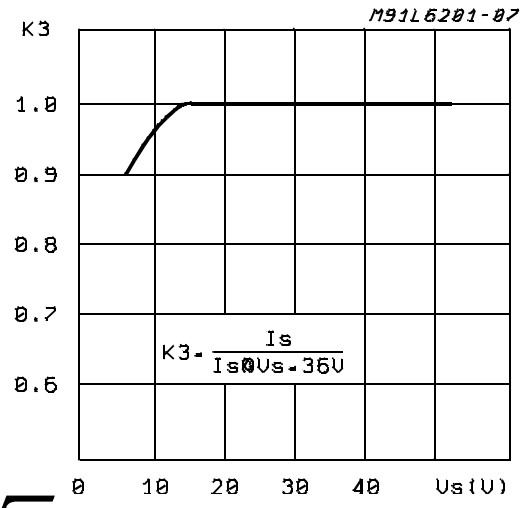


Figure 4: Typical $R_{DS\ (ON)}$ vs. V_S ~ V_{ref}