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MC68HC16Z1

Technical Supplement

25.17 MHz Electrical Characteristics

Devices in the M68HC16 Modular Microcontroller Family are built up from a selection of standard functional modules. Published electrical characteristics for MC68HC16Z1 devices are based on a16.78 MHz system clock. New products that operate at clock frequencies of 25.17 MHz are now available. This supplement consists of a new electrical characteristics appendix (Appendix A) that supplements those published in the *MC68HC16Z1 User's Manual* (MC68HC16Z1UM/AD).

The supplement contains the following updated specifications:

Table **Page**

Table A–1 Maximum Ratings

Num	Rating	Symbol	Value	Unit
1	Supply Voltage[1, 2, 3]	V_{DD}	– 0.3 to + 6.5	V
2	Input Voltage [1, 2, 3, 4, 5,7]	V_{IN}	– 0.3 to + 6.5	V
3	Instantaneous Maximum Current Single Pin Limit (all pins)[1, 3, 5, 6]	I_D	25	mA
4	Operating Maximum Current Digital Input Disruptive Current[3, 5, 6, 7, 8] $V_{NEGCLMAP} \cong -0.3$ V $V_{POSCLAMP} \cong V_{DD} + 0.3$	Ii_D	– 500 to 500	µA
5	Operating Temperature Range “C” Suffix “V” Suffix “M” Suffix	T_A	TL to TH – 40 to 85 – 40 to 105 – 40 to 125	°C
6	Storage Temperature Range	T_{stg}	– 55 to 150	°C

NOTES:

1. Permanent damage can occur if maximum ratings are exceeded. Exposure to voltages or currents in excess of recommended values affects device reliability. Device modules may not operate normally while being exposed to electrical extremes.
2. Although sections of the device contain circuitry to protect against damage from high static voltages or electrical fields, take normal precautions to avoid exposure to voltages higher than maximum-rated voltages.
3. This parameter is periodically sampled rather than 100% tested.
4. All pins except TSC.
5. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
6. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current.
7. All functional non-supply pins are internally clamped to V_{SS}. All functional pins except EXTAL and XFC are internally clamped to V_{DD}.
8. Total input current for all digital input-only and all digital input/output pins must not exceed 10 mA. Exceeding this limit can cause disruption of normal operation.

Table A–2 Typical Ratings

Num	Rating	Symbol	Value	Unit
1	Supply Voltage	V_{DD}	5.0	V
2	Operating Temperature	T_A	25	°C
3	V_{DD} Supply Current RUN LPSTOP, VCO off LPSTOP, External clock, max f_{sys}	I_{DD}	 113 125 3.75	 mA µA mA
4	Clock Synthesizer Operating Voltage	V_{DDSYN}	5.0	V
5	V_{DDSYN} Supply Current VCO on, maximum f_{sys} External Clock, maximum f_{sys} LPSTOP, VCO off V_{DD} powered down	I_{DDSYN}	 1.0 5.0 100 50	 mA mA µA µA
6	RAM Standby Voltage	V_{SB}	3.0	V
7	RAM Standby Current Normal RAM operation Standby operation	ISB	 7.0 40	 µA µA
8	Power Dissipation	P_D	570	mW

Table A–3 Thermal Characteristics

Num	Characteristic	Symbol	Value	Unit
1	Thermal Resistance[1] Plastic 132-Pin Surface Mount Plastic 144-Pin Surface Mount	Θ_{JA}	 38 49	°C/W

NOTES:

1. The average chip-junction temperature (TJ) in C can be obtained from (1):

$$T_J = T_A + (P_D \cdot \Theta_{JA})$$

where:

T_A= Ambient Temperature, °C

Θ_{JA}= Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{DD} \times V_{DD}$, Watts — Chip Internal Power

$P_{I/O}$= Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is (2):

$$P_D = K + (T_J + 273°C)$$

Solving equations (1) and (2) for K gives (3):

$$K = P_D + (T_A + 273°C) + \Theta_{JA} \times P_{D^2}$$

Where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring PD (at equilibrium) for a known TA. Using this value of K, the values of PD and TJ can be obtained by solving equations (1) and (2) iteratively for any value of TA.

Table A–4 Clock Control Timing

(V_{DD} and V_{DDSYN} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, Stable External Reference)[1]

Num	Characteristic	Symbol	Minimum	Maximum	Unit
1	PLL Reference Frequency Range	f_{ref}	25	50	kHz
2	System Frequency[2] On-Chip PLL System Frequency External Clock Operation	f_{sys}	dc 0.131 dc	25.17 25.17 25.17	MHz
3	PLL Lock Time[3,5,6,7]	t_{lpll}	—	20	ms
4	VCO Frequency[4]	f_{VCO}	—	2 (f_{sys} max)	MHz
5	Limp Mode Clock Frequency SYNCR X bit = 0 SYNCR X bit = 1	f_{limp}	— —	f_{sys} max /2 f_{sys} max	MHz
6	CLKOUT Jitter[5,6,7,8] Short term (5 µs interval) Long term (500 µs interval)	J_{clk}	–1.0 –0.5	1.0 0.5	%

NOTES:

1. Tested with a 32.768 kHz reference.
2. All internal registers retain data at 0 Hz.
3. Assumes that stable V_{DDSYN} is applied, and that the crystal oscillator is stable. Lock time is measured from the time V_{DD} and V_{DDSYN} are valid until $\overline{\text{RESET}}$ is released. This specification also applies to the period required for PLL lock after changing the W and Y frequency control bits in the synthesizer control register (SYNCR) while the PLL is running, and to the period required for the clock to lock after LPSTOP.
4. Internal VCO frequency (f_{VCO}) is determined by SYNCR W and Y bit values.
   The SYNCR X bit controls a divide-by-two circuit that is not in the synthesizer feedback loop.
   When X = 0, the divider is enabled, and $f_{sys} = f_{VCO} \div 4$.
   When X = 1, the divider is disabled, and $f_{sys} = f_{VCO} \div 2$.
   X must equal one when operating at maximum specified f_{sys}.
5. This parameter is periodically sampled rather than 100% tested.
6. Assumes that a low-leakage external filter network is used to condition clock synthesizer input voltage. Total external resistance from the XFC pin due to external leakage must be greater than 15 M Ω to guarantee this specification. Filter network geometry can vary depending upon operating environment.
7. Proper layout procedures must be followed to achieve specifications.
8. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDSYN} and V_{SS} and variation in crystal oscillator frequency increase the J_{clk} percentage for a given interval. When jitter is a critical constraint on control system operation, this parameter should be measured during functional testing of the final system.

Table A–5 DC Characteristics

(V_{DD} and V_{DDSYN} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Num	Characteristic	Symbol	Min	Max	Unit
1	Input High Voltage	V_{IH}	0.7 (V_{DD})	V_{DD} + 0.3	V
2	Input Low Voltage	V_{IL}	V_{SS} – 0.3	0.2 (V_{DD})	V
3	Input Hysteresis[1, 2]	V_{HYS}	0.5	—	V
4	Input Leakage Current[3,16] V_{in} = V_{DD} or V_{SS}	I_{in}	– 2.5	2.5	µA
5	High Impedance (Off-State) Leakage Current[4,16] V_{in} = V_{DD} or V_{SS}	I_{OZ}	– 2.5	2.5	µA
6	CMOS Output High Voltage[5,6,16] I_{OH} = –10.0 µA	V_{OH}	V_{DD} – 0.2	—	V
7	CMOS Output Low Voltage[6,16] I_{OL} = 10.0 µA	V_{OL}	—	0.2	V
8	Output High Voltage[5,6,16] I_{OH} = –0.8 mA	V_{OH}	V_{DD} –0.8	—	V
9	Output Low Voltage[7,16] I_{OL} = 1.6 mA I_{OL} = 5.3 mA I_{OL} = 12 mA	V_{OL}	— — —	0.4 0.4 0.4	V
10	Three State Control Input High Voltage	V_{IHTSC}	1.6 (V_{DD})	9.1	V
11	Data Bus Mode Select Pull-up Current[8,9] V_{in} = V_{IL} V_{in} = V_{IH}	I_{MSP}	— –15	–120 —	µA
12	V_{DD} Supply Current[10,11, 12] Run LPSTOP, crystal reference, VCO Off (STSIM = 0) LPSTOP, external clock input frequency = maximum f_{sys}	I_{DD}	— — —	140 350 5	mA µA µA
13	Clock Synthesizer Operating Voltage	V_{DDSYN}	4.75	5.25	V
14	V_{DDSYN} Supply Current[6,12] Crystal reference, VCO on, maximum f_{sys} External clock input, maximum f_{sys} Crystal reference, LPSTOP, VCO off (STSIM = 0) Crystal reference, V_{DD} powered down	I_{DDSYN}	— — — —	2 7 150 100	mA mA µA µA
15	RAM Standby Voltage[13] Specified V_{DD} applied V_{DD} = V_{SS}	V_{SB}	0.0 3.0	5.25 5.25	V
16	RAM Standby Current[10] Normal RAM operation[14] $V_{DD} > V_{SB}$ – 0.5 V Transient condition V_{SB} – 0.5 V ≥ V_{DD} ≥ V_{SS} + 0.5 V Standby operation[13] $V_{DD} < V_{SS}$ + 0.5 V	I_{SB}	— — —	10 3 50	µA mA µA
17	Power Dissipation[15, 16]	P_D	—	766	mW
18	Input Capacitance[2, 16] All input-only pins except ADC pins All input/output pins	C_{in}	— —	10 20	pF

Table A–5 DC Characteristics (Continued)

(V_{DD} and V_{DDSYN} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Num	Characteristic	Symbol	Min	Max	Unit
19	Load Capacitance[16] Group 1 I/O Pins, CLKOUT, FREEZE/QUOT, IPIPE0 Group 2 I/O Pins and $\overline{\text{CSBOOT}}$, BG/$\overline{\text{CS}}$ Group 3 I/O Pins Group 4 I/O Pins	C_L	 — — — —	 90 100 130 200	pF

NOTES:

1. Applies to:
   Port ADA[7:0] — AN[7:0]
   Port E[7:4] — SIZ[1:0], $\overline{\text{AS}}$, $\overline{\text{DS}}$
   Port F[7:0] — IRQ[7:1], MODCLK
   Port GP[7:0] — IC4/OC5/OC1, IC[3:1], OC[4:1]/OC1
   Port QS[7:0] — TXD, PCS[3:1], PCS0/$\overline{\text{SS}}$, SCK, MOSI, MISO
   $\overline{\text{BKPT}}$/DSCLK, DSI/IPIPE1, PAI, PCLK, $\overline{\text{RESET}}$, RXD, TSC
   EXTAL (when PLL enabled)
2. This parameter is periodically sampled rather than 100% tested.
3. Applies to all input-only pins except ADC pins.
4. Applies to all input/output and output pins
5. Does not apply to $\overline{\text{HALT}}$ and $\overline{\text{RESET}}$ because they are open drain pins. Does not apply to Port QS[7:0] (TXD, PCS[3:1], PCS0/$\overline{\text{SS}}$, SCK, MOSI, MISO) in wired-OR mode.
6. Applies to Group 1, 2, 4 input/output and all output pins
7. Applies to Group 1, 2, 3, 4 input/output pins, BG/$\overline{\text{CS}}$, CLKOUT, $\overline{\text{CSBOOT}}$, FREEZE/QUOT, and IPIPE0
8. Applies to DATA[15:0]
9. Use of an active pulldown device is recommended.
10. Total operating current is the sum of the appropriate I_{DD}, I_{DDSYN}, and I_{SB} values, plus I_{DDA}. I_{DD} values include supply currents for device modules powered by V_{DDE} and V_{DDI} pins.
11. Current measured at maximum system clock frequency, all modules active.
12. Tested with a 32.768 kHz crystal reference.
13. The SRAM module will not switch into standby mode as long as V_{SB} does not exceed V_{DD} by more than 0.5 volts. The SRAM array cannot be accessed while the module is in standby mode.
14. When V_{SB} is more than 0.3 V greater than V_{DD}, current flows between the V_{STBY} and V_{DD} pins, which causes standby current to increase toward the maximum transient condition specification. System noise on the V_{DD} and V_{STBY} pin can contribute to this condition.
15. Power dissipation measured at specified system clock frequency, all modules active. Power dissipation can be calculated using the expression:
    $$P_D = \text{Maximum } V_{DD} (I_{DD} + I_{DDSYN} + I_{SB}) + \text{Maximum } V_{DDA} (I_{DDA})$$
    I_{DD} includes supply currents for all device modules powered by V_{DDE} and V_{DDI} pins.
16. Input-Only Pins: EXTAL, TSC, BKPT/DSCLK, PAI, PCLK, RXD
    Output-Only Pins: $\overline{\text{CSBOOT}}$, BG/$\overline{\text{CS1}}$, CLKOUT, FREEZE/QUOT, DS0/IPIPE0, PWMA, PWMB
    Input/Output Pins:
    Group 1: Port GP[7:0] — IC4/OC5/OC1, IC[3:1], OC[4:1]/OC1
    DATA[15:0], DSI/IPIPE1
    Group 2: Port C[6:0] — ADDR[22:19]/$\overline{\text{CS}}$[9:6], FC[2:0]/$\overline{\text{CS}}$[5:3]
    Port E[7:0] — SIZ[1:0], $\overline{\text{AS}}$, $\overline{\text{DS}}$, $\overline{\text{AVEC}}$, $\overline{\text{DSACK}}$[1:0]
    Port F[7:0] — $\overline{\text{IRQ}}$[7:1], MODCLK
    Port QS[7:3] — TXD, PCS[3:1], PCS0/$\overline{\text{SS}}$, ADDR23/$\overline{\text{CS10}}$/ECLK
    ADDR[18:0], R/$\overline{\text{W}}$, $\overline{\text{BERR}}$, $\overline{\text{BR}}$/$\overline{\text{CS0}}$, $\overline{\text{BGACK}}$/$\overline{\text{CS2}}$
    Group 3: $\overline{\text{HALT}}$, $\overline{\text{RESET}}$
    Group 4: MISO, MOSI, SCK

Table A–6 AC Timing

(V_{DD} and V_{DDSYN} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)[1]

Num	Characteristic	Symbol	Min	Max	Unit
F1	Frequency of Operation[2]	f	4 (f_{ref})	25.166	MHz
1	Clock Period	t_{cyc}	39.7	—	ns
1A	ECLK Period	t_{Ecyc}	318	—	ns
1B	External Clock Input Period[3]	t_{Xcyc}	39.7	—	ns
2, 3	Clock Pulse Width	t_{CW}	15	—	ns
2A, 3A	ECLK Pulse Width	t_{ECW}	155	—	ns
2B, 3B	External Clock Input High/Low Time[3]	t_{XCHL}	19.8	—	ns
4, 5	CLKOUT Rise and Fall Time	t_{Crf}	—	5	ns
4A, 5A	Rise and Fall Time (All Outputs except CLKOUT)	t_{rf}	—	8	ns
4B, 5B	External Clock Input Rise and Fall Time[4]	t_{XCrf}	—	4	ns
6	Clock High to ADDR, FC, SIZE Valid	t_{CHAV}	0	19	ns
7	Clock High to ADDR, Data, FC, SIZE, High Impedance	t_{CHAZx}	0	39	ns
8	Clock High to ADDR, FC, SIZE, Invalid	t_{CHAZn}	0	—	ns
9	Clock Low to $\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Asserted	t_{CLSA}	2	19	ns
9A	$\overline{AS}$ to $\overline{DS}$ or $\overline{CS}$ Asserted (Read)[5]	t_{STSA}	–10	15	ns
11	ADDR, FC, SIZE Valid to $\overline{AS}$, $\overline{CS}$, (and $\overline{DS}$ Read) Asserted	t_{AVSA}	8	—	ns
12	Clock Low to $\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Negated	t_{CLSN}	2	19	ns
13	$\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Negated to ADDR, FC SIZE Invalid (Address Hold)	t_{SNAI}	8	—	ns
14	$\overline{AS}$, $\overline{CS}$ (and $\overline{DS}$ Read) Width Asserted	t_{SWA}	65	—	ns
14A	$\overline{DS}$, $\overline{CS}$ Width Asserted (Write)	t_{SWAW}	25	—	ns
14B	$\overline{AS}$, $\overline{CS}$ (and $\overline{DS}$ Read) Width Asserted (Fast Cycle)	t_{SWDW}	22	—	ns
15	$\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Width Negated[6]	t_{SN}	22	—	ns
16	Clock High to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ High Impedance	t_{CHSZ}	—	39	ns
17	$\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Negated to R/$\overline{W}$ High	t_{SNRN}	10	—	ns
18	Clock High to R/$\overline{W}$ High	t_{CHRH}	0	19	ns
20	Clock High to R/$\overline{W}$ Low	t_{CHRL}	0	19	ns
21	R/$\overline{W}$ High to $\overline{AS}$, $\overline{CS}$ Asserted	t_{RAAA}	10	—	ns
22	R/$\overline{W}$ Low to $\overline{DS}$, $\overline{CS}$ Asserted (Write)	t_{RASA}	40	—	ns
23	Clock High to Data Out Valid	t_{CHDO}	—	19	ns
24	Data Out Valid to Negating Edge of $\overline{AS}$, $\overline{CS}$ (Fast Write Cycle)	t_{DVASN}	7	—	ns
25	$\overline{DS}$, $\overline{CS}$ Negated to Data Out Invalid (Data Out Hold)	t_{SNDOI}	5	—	ns
26	Data Out Valid to $\overline{DS}$, $\overline{CS}$ Asserted (Write)	t_{DVSA}	8	—	ns

Table A–6 AC Timing (Continued)

(V_{DD} and V_{DDSYN} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)[1]

Num	Characteristic	Symbol	Min	Max	Unit
27	Data In Valid to Clock Low (Data Setup)	t_{DICL}	5	—	ns
27A	Late $\overline{BERR}$, $\overline{HALT}$ Asserted to Clock Low (Setup Time)	t_{BELCL}	10	—	ns
28	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{DSACK[1:0]}$, $\overline{BERR}$, $\overline{HALT}$, $\overline{AVEC}$ Negated	t_{SNDN}	0	50	ns
29	$\overline{DS}$, $\overline{CS}$ Negated to Data In Invalid (Data In Hold)[7]	t_{SNDI}	0	—	ns
29A	$\overline{DS}$, $\overline{CS}$ Negated to Data In High Impedance[7, 8]	t_{SHDI}	—	45	ns
30	CLKOUT Low to Data In Invalid (Fast Cycle Hold)[7]	t_{CLDI}	8	—	ns
30A	CLKOUT Low to Data In High Impedance[7]	t_{CLDH}	—	60	ns
31	$\overline{DSACK[1:0]}$ Asserted to Data In Valid[9]	t_{DADI}	—	35	ns
33	Clock Low to $\overline{BG}$ Asserted/Negated	t_{CLBAN}	—	19	ns
35	$\overline{BR}$ Asserted to $\overline{BG}$ Asserted[10]	t_{BRAGA}	1	—	t_{cyc}
37	$\overline{BGACK}$ Asserted to $\overline{BG}$ Negated	t_{GAGN}	1	2	t_{cyc}
39	$\overline{BG}$ Width Negated	t_{GH}	2	—	t_{cyc}
39A	$\overline{BG}$ Width Asserted	t_{GA}	1	—	t_{cyc}
46	R/$\overline{W}$ Width Asserted (Write or Read)	t_{RWA}	90	—	ns
46A	R/$\overline{W}$ Width Asserted (Fast Write or Read Cycle)	t_{RWAS}	55	—	ns
47A	Asynchronous Input Setup Time $\overline{BR}$, $\overline{BGACK}$, $\overline{DSACK[1:0]}$, $\overline{BERR}$, $\overline{AVEC}$, $\overline{HALT}$	t_{AIST}	5	—	ns
47B	Asynchronous Input Hold Time	t_{AIHT}	10	—	ns
48	$\overline{DSACK[1:0]}$ Asserted to $\overline{BERR}$, $\overline{HALT}$ Asserted[11]	t_{DABA}	—	27	ns
53	Data Out Hold from Clock High	t_{DOCH}	0	—	ns
54	Clock High to Data Out High Impedance	t_{CHDH}	—	23	ns
55	R/W Asserted to Data Bus Impedance Change	t_{RADC}	25	—	ns
70	Clock Low to Data Bus Driven (Show Cycle)	t_{SCLDD}	0	19	ns
71	Data Setup Time to Clock Low (Show Cycle)	t_{SCLDS}	8	—	ns
72	Data Hold from Clock Low (Show Cycle)	t_{SCLDH}	8	—	ns
73	$\overline{BKPT}$ Input Setup Time	t_{BKST}	10	—	ns
74	$\overline{BKPT}$ Input Hold Time	t_{BKHT}	10	—	ns
75	Mode Select Setup Time (DATA[15:0], $\overline{MODCLK}$, $\overline{BKPT}$)	t_{MSS}	20	—	t_{cyc}
76	Mode Select Hold Time (DATA[15:0], $\overline{MODCLK}$, $\overline{BKPT}$)	t_{MSH}	0	—	ns
77	$\overline{RESET}$ Assertion Time[12]	t_{RSTA}	4	—	t_{cyc}
78	$\overline{RESET}$ Rise Time[13,14]	t_{RSTR}	—	10	t_{cyc}

Table A–6 AC Timing (Continued)

(V_{DD} and V_{DDSYN} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)[1]

Num	Characteristic	Symbol	Min	Max	Unit
100	CLKOUT High to Phase 1 Asserted[15]	t_{CHP1A}	3	34	ns
101	CLKOUT High to Phase 2 Asserted[15]	t_{CHP2A}	3	34	ns
102	Phase 1 Valid to $\overline{AS}$ or $\overline{DS}$ Asserted[15]	t_{P1VSA}	9	—	ns
103	Phase 2 Valid to $\overline{AS}$ or $\overline{DS}$ Asserted[15]	t_{P2VSN}	9	—	ns
104	$\overline{AS}$ or $\overline{DS}$ Valid to Phase 1 Negated[15]	t_{SAP1N}	9	—	ns
105	$\overline{AS}$ or $\overline{DS}$ Negated to Phase 2 Negated[15]	t_{SNP2N}	9	—	ns

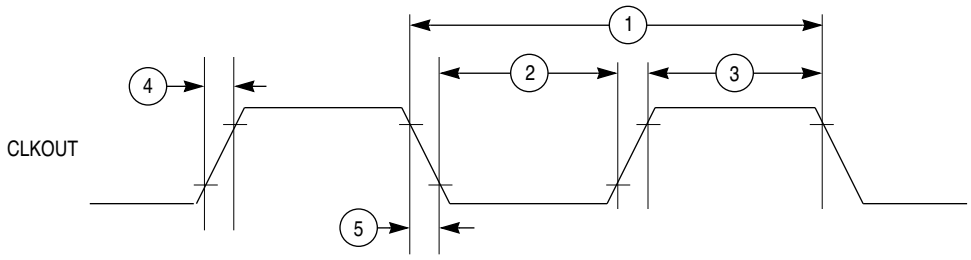
NOTES:

1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.
2. Minimum system clock frequency is four times the crystal frequency, subject to specified limits.
3. When an external clock is used, minimum high and low times are based on a 50% duty cycle. The minimum allowable t_{Xcyc} period is reduced when the duty cycle of the external clock varies. The relationship between external clock input duty cycle and minimum t_{Xcyc} is expressed:

   Minimum t_{Xcyc} period = minimum t_{XCHL} / (50% – external clock input duty cycle tolerance).
4. Parameters for an external clock signal applied while the internal PLL is disabled (MODCLK pin held low during reset). Does not pertain to an external VCO reference applied while the PLL is enabled (MODCLK pin held high during reset). When the PLL is enabled, the clock synthesizer detects successive transitions of the reference signal. If transitions occur within the correct clock period, rise/fall times and duty cycle are not critical.
5. Specification 9A is the worst-case skew between $\overline{AS}$ and $\overline{DS}$ or $\overline{CS}$. The amount of skew depends on the relative loading of these signals. When loads are kept within specified limits, skew will not cause $\overline{AS}$ and $\overline{DS}$ to fall outside the limits shown in specification 9.
6. If multiple chip selects are used, $\overline{CS}$ width negated (specification 15) applies to the time from the negation of a heavily loaded chip select to the assertion of a lightly loaded chip select. The $\overline{CS}$ width negated specification between multiple chip selects does not apply to chip selects being used for synchronous ECLK cycles.
7. Hold times are specified with respect to $\overline{DS}$ or $\overline{CS}$ on asynchronous reads and with respect to CLKOUT on fast cycle reads. The user is free to use either hold time.
8. Maximum value is equal to (t_{cyc} / 2) + 25 ns.
9. If the asynchronous setup time (specification 47A) requirements are satisfied, the $\overline{DSACK[1:0]}$ low to data setup time (specification 31) and $\overline{DSACK[1:0]}$ low to $\overline{BERR}$ low setup time (specification 48) can be ignored. The data must only satisfy the data-in to clock low setup time (specification 27) for the following clock cycle. $\overline{BERR}$ must satisfy only the late $\overline{BERR}$ low to clock low setup time (specification 27A) for the following clock cycle.
10. To ensure coherency during every operand transfer, $\overline{BG}$ is not asserted in response to $\overline{BR}$ until after all cycles of the current operand transfer are complete.
11. In the absence of $\overline{DSACK[1:0]}$, $\overline{BERR}$ is an asynchronous input using the asynchronous setup time (specification 47A).
12. After external $\overline{RESET}$ negation is detected, a short transition period (approximately 2 t_{cyc}) elapses, then the SIM drives $\overline{RESET}$ low for 512 tcyc.
13. External assertion of the $\overline{RESET}$ input can overlap internally-generated resets. To insure that an external reset is recognized in all cases, $\overline{RESET}$ must be asserted for at least 590 CLKOUT cycles.
14. External logic must pull $\overline{RESET}$ high during this period in order for normal MCU operation to begin.
15. Eight pipeline states are multiplexed into IPIPE[1:0]. The multiplexed signals have two phases.
16. Address access time = (2.5 + WS) t_{cyc} – t_{CHAV} – t_{DICL}

    Chip select access time = (2 + WS) t_{cyc} – t_{CLSA} – t_{DICL}

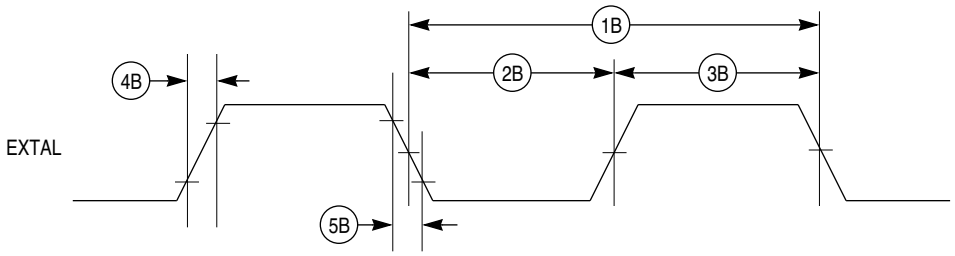
    Where: WS = number of wait states. When fast termination is used (2 clock bus) WS = –1.



NOTE: TIMING SHOWN WITH RESPECT TO 20% AND 70% V_{DD}

16 CLKOUT TIM

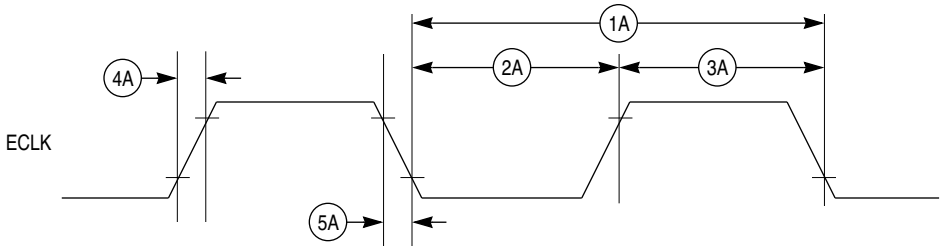
Figure A–1 CLKOUT Output Timing Diagram



NOTE: TIMING SHOWN WITH RESPECT TO 20% AND 70% V_{DD}
PULSE WIDTH SHOWN WITH RESPECT TO 50% V_{DD}

16 EXT CLK INPUT TIM

Figure A–2 External Clock Input Timing Diagram



NOTE: TIMING SHOWN WITH RESPECT TO 20% AND 70% V_{DD}

16 ECLK OUTPUT TIM

Figure A–3 ECLK Output Timing Diagram

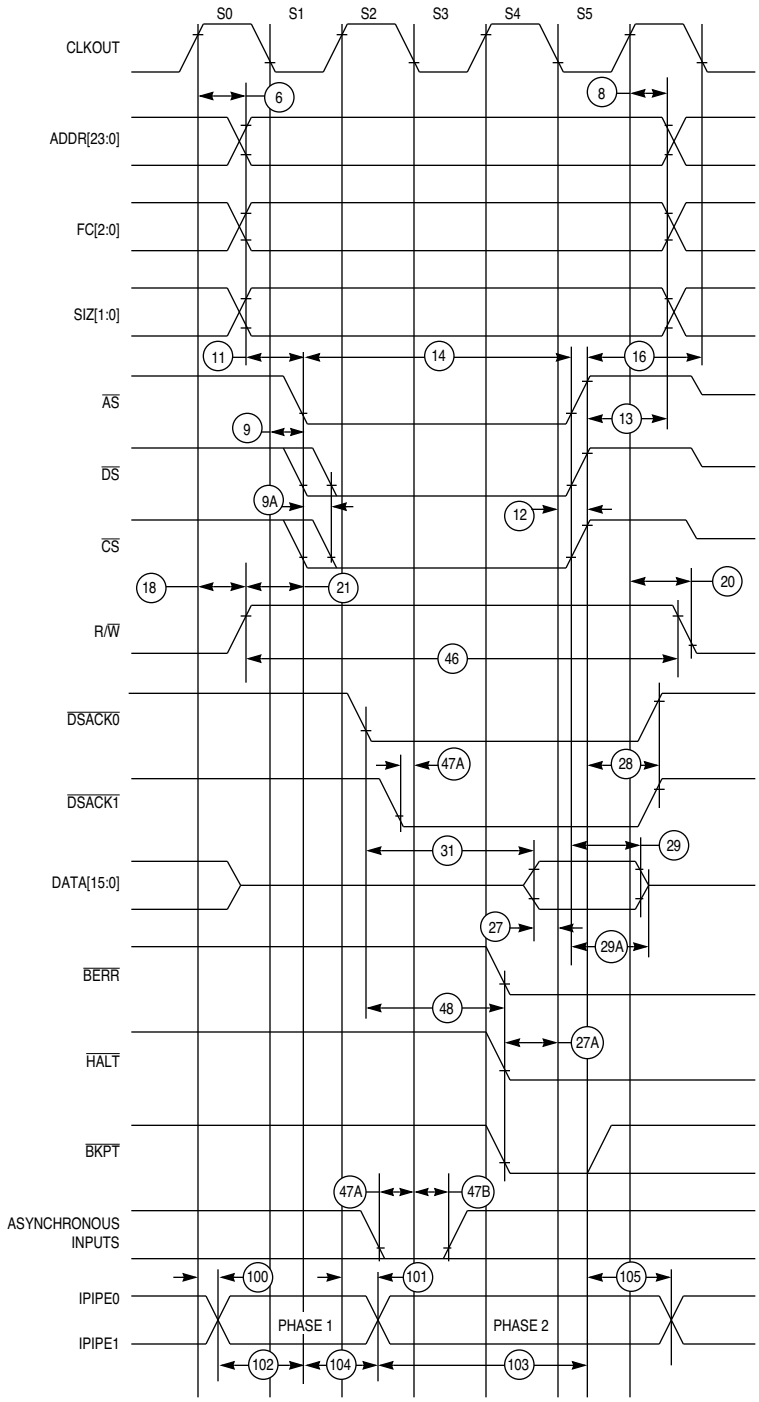


Figure A–4 Read Cycle Timing Diagram

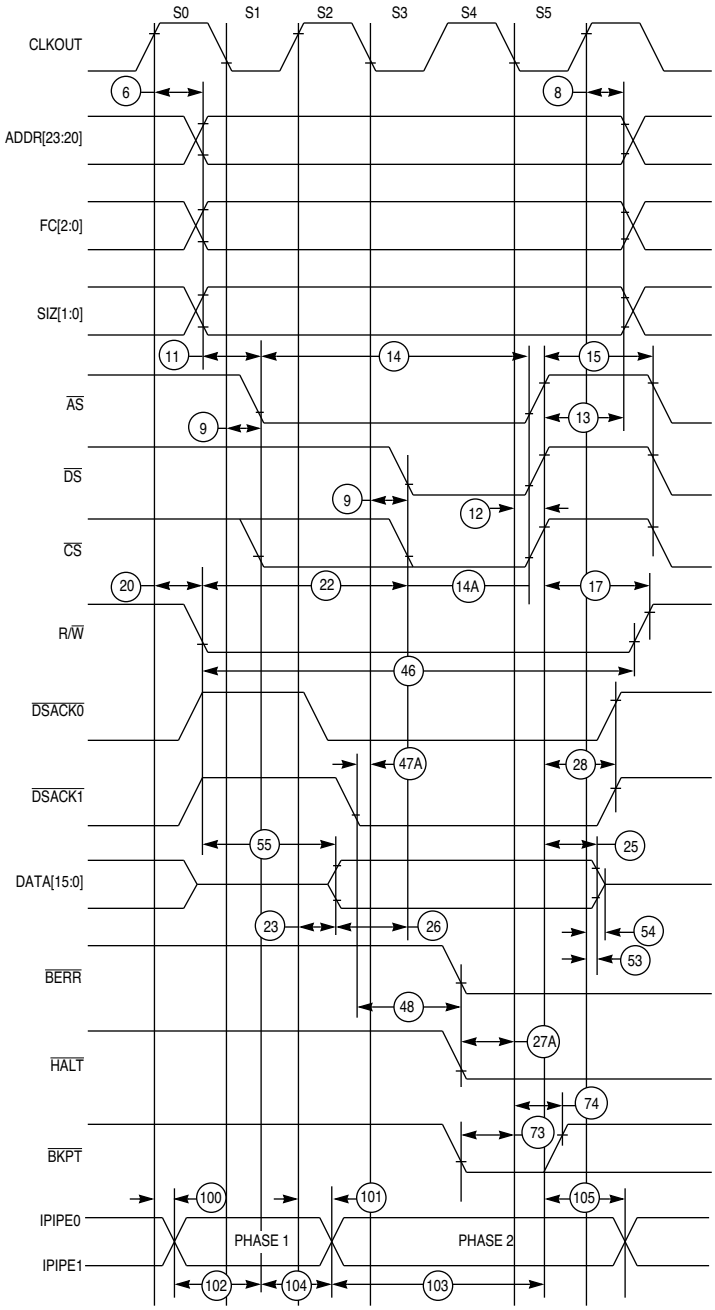


Figure A–5 Write Cycle Timing Diagram

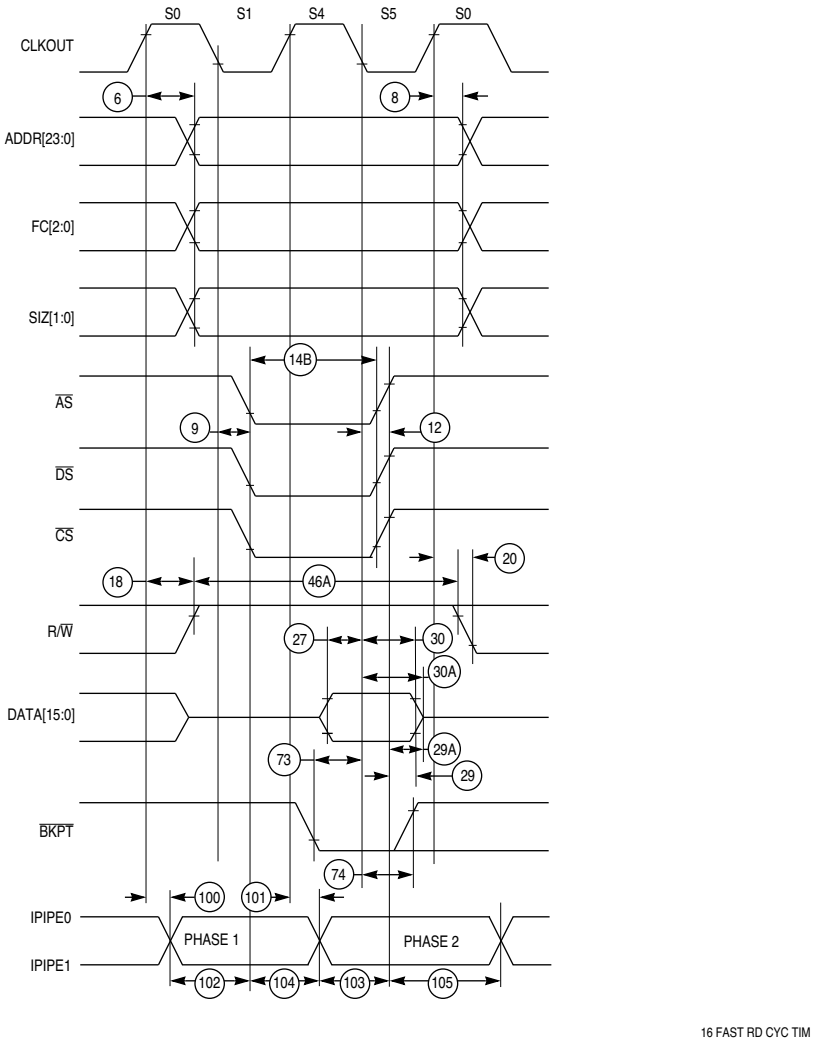


Figure A–6 Fast Termination Read Cycle Timing Diagram

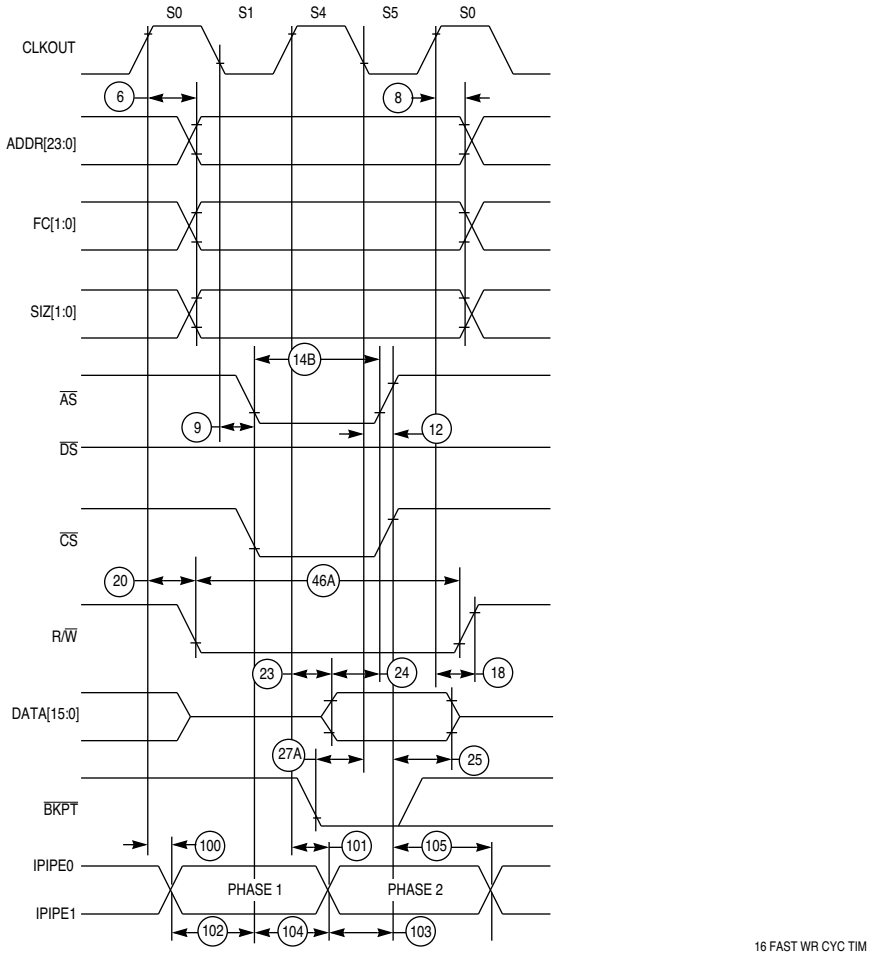


Figure A–7 Fast Termination Write Cycle Timing Diagram

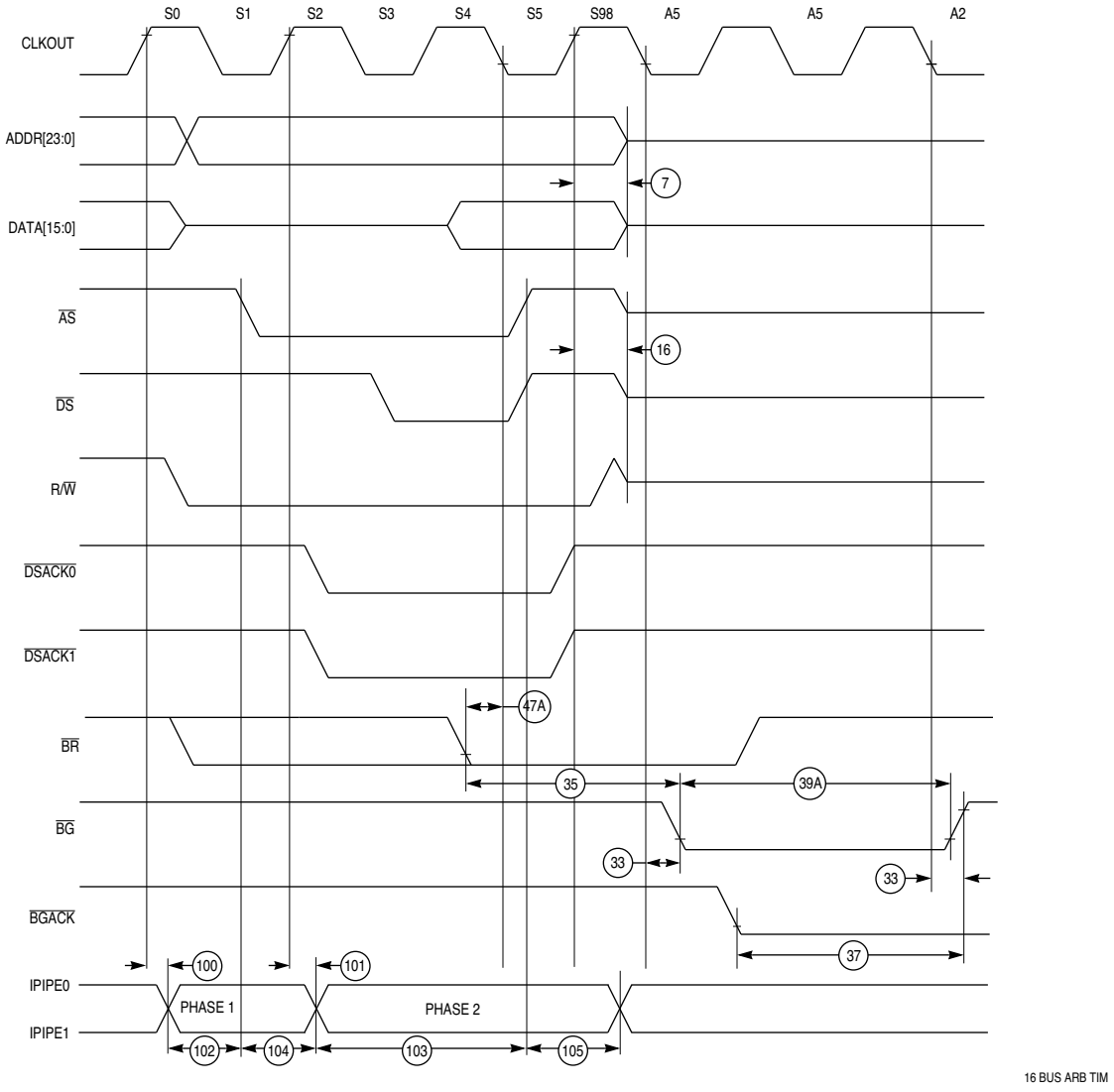
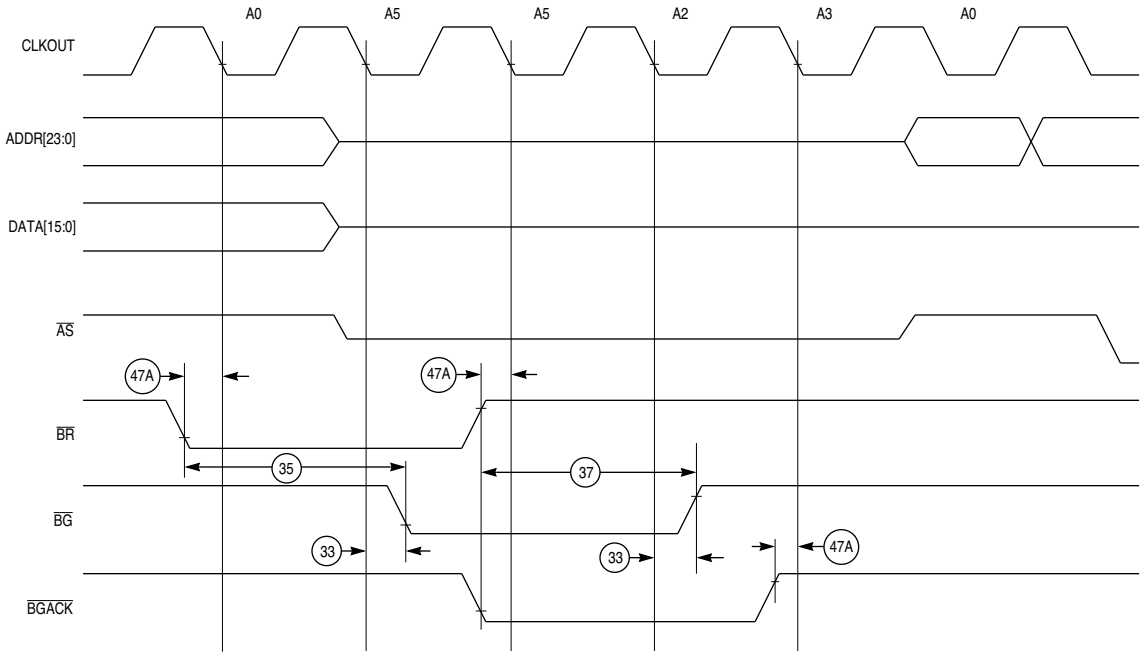
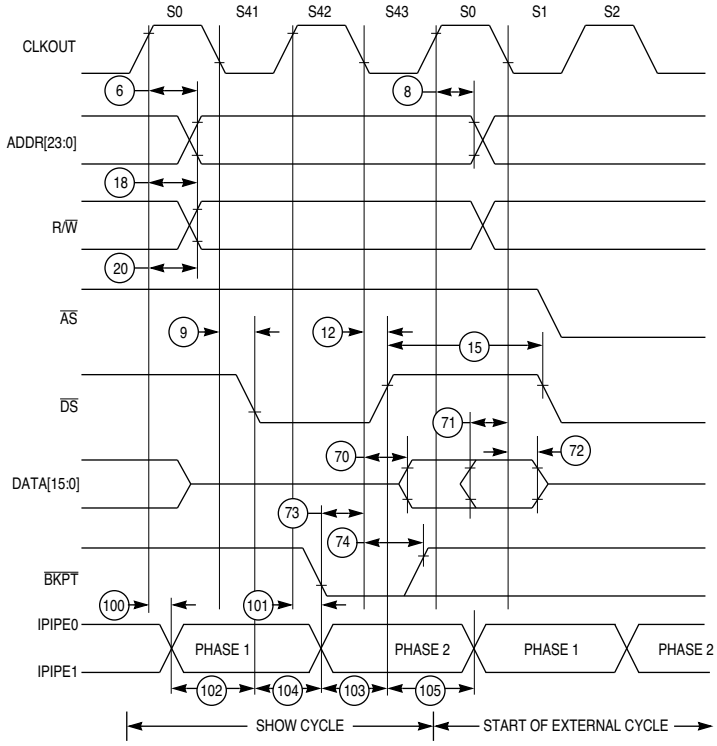


Figure A–8 Bus Arbitration Timing Diagram — Active Bus Case



16 BUS ARB TIM IDLE

Figure A–9 Bus Arbitration Timing Diagram — Idle Bus Case



NOTE:
Show cycles can stretch during clock phase S42 when bus accesses take longer than two cycles due to IMB module wait-state insertion.

16 SHW CYC TIM

Figure A–10 Show Cycle Timing Diagram

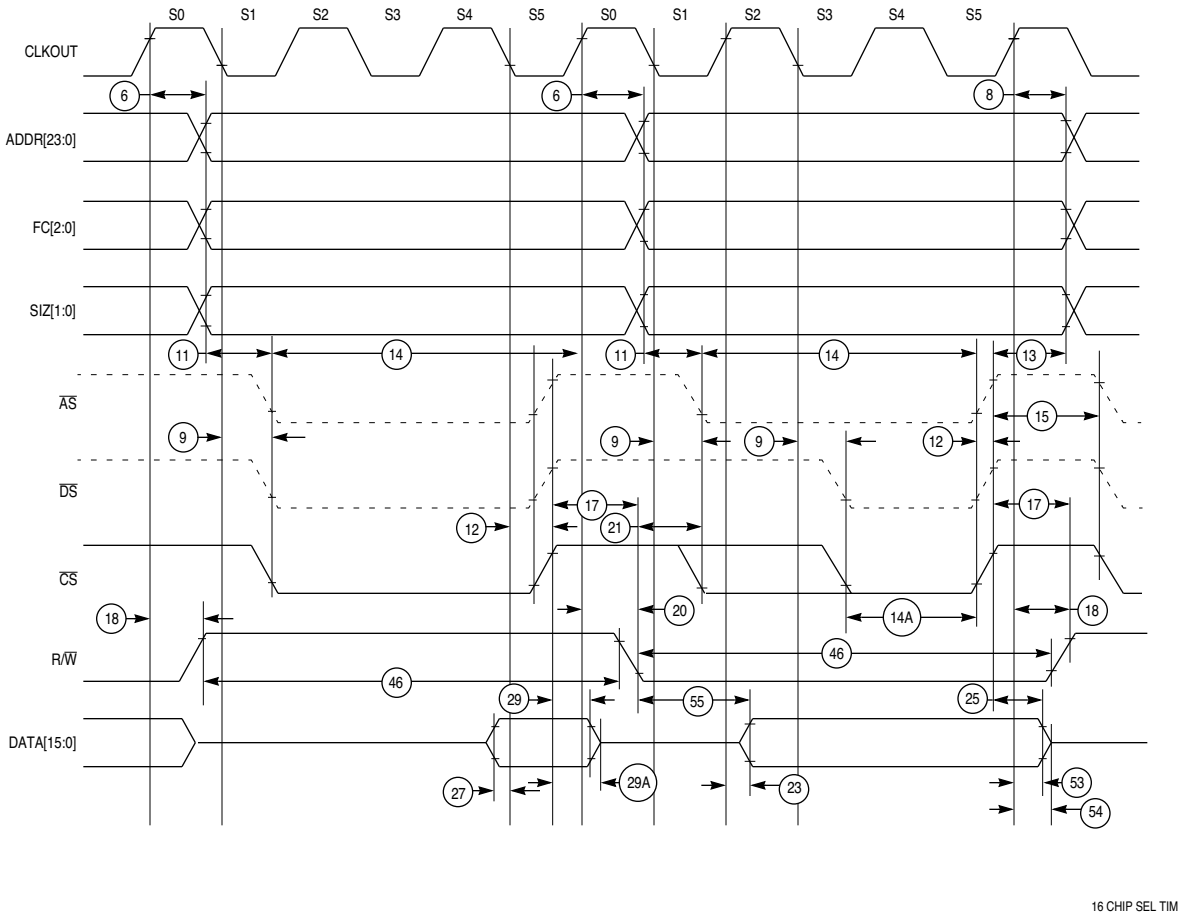


Figure A–11 Chip-Select Timing Diagram

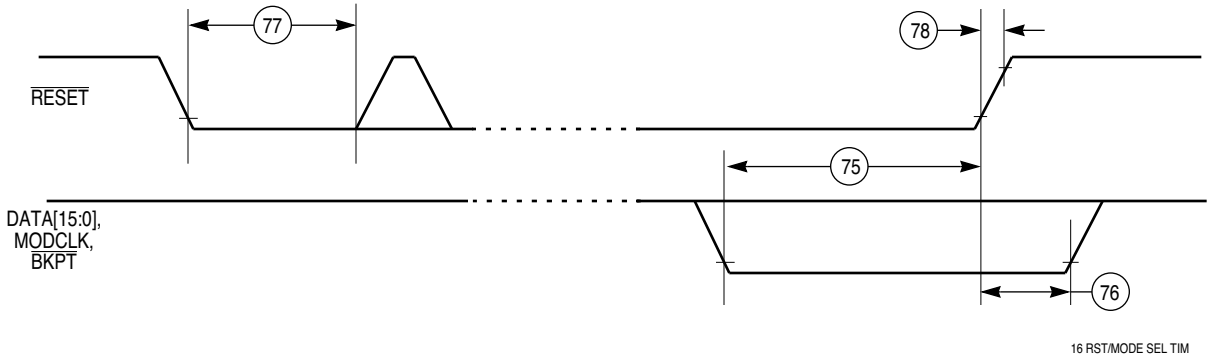


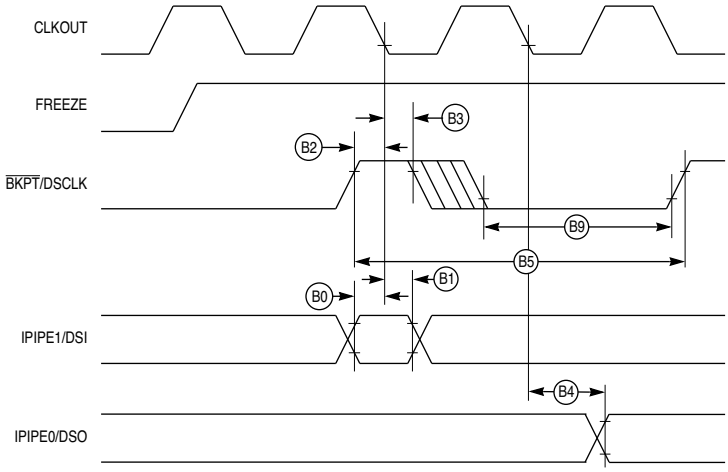
Figure A–12 Reset and Mode Select Timing Diagram

Table A–7 Background Debugging Mode Timing

(V_{DD} and V_{DDSYN} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)[1]

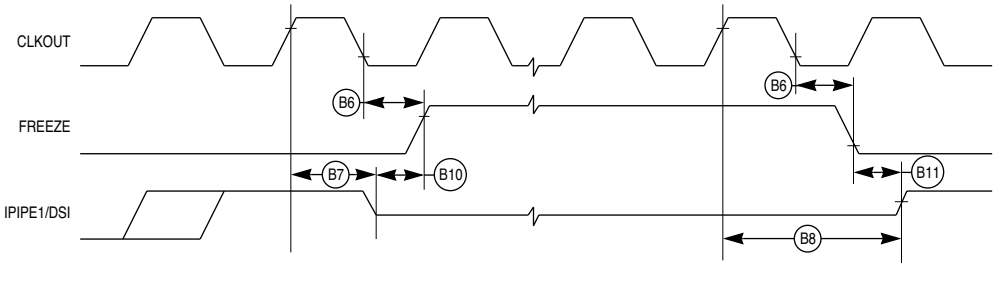
Num	Characteristic	Symbol	Min	Max	Unit
B0	DSI Input Setup Time	t_{DSISU}	10	—	ns
B1	DSI Input Hold Time	t_{DSIH}	5	—	ns
B2	DSCLK Setup Time	t_{DSCSU}	10	—	ns
B3	DSCLK Hold Time	t_{DSCH}	5	—	ns
B4	DSO Delay Time	t_{DSOD}	—	20	ns
B5	DSCLK Cycle Time	t_{DSCCYC}	2	—	t_{cyc}
B6	CLKOUT High to FREEZE Asserted/Negated	t_{FRZAN}	—	20	ns
B7	CLKOUT High to IPIPE1 High Impedance	t_{IPZ}	—	20	ns
B8	CLKOUT High to IPIPE1 Valid	t_{IP}	—	20	ns
B9	DSCLK Low Time	t_{DSCLO}	1	—	t_{cyc}
B10	IPIPE1 High Impedance to FREEZE Asserted	t_{IPFA}	TBD	—	t_{cyc}
B11	FREEZE Negated to IPIPE[0:1] Active	t_{FRIP}	TBD	—	t_{cyc}

NOTES:
1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.



16 BDM SER COM TIM

Figure A–13 BDM Serial Communication Timing Diagram



16 BDM FRZ TIM

Figure A–14 BDM Freeze Assertion Timing Diagram

Table A–8 ECLK Bus Timing

(V_{DD} and V_{DDSYN} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)[1]

Num	Characteristic	Symbol	Min	Max	Unit
E1	ECLK Low to Address Valid[2]	t_{EAD}	—	40	ns
E2	ECLK Low to Address Hold	t_{EAH}	10	—	ns
E3	ECLK Low to $\overline{CS}$ Valid ($\overline{CS}$ Delay)	t_{ECSD}	—	100	ns
E4	ECLK Low to $\overline{CS}$ Hold	t_{ECSH}	10	—	ns
E5	$\overline{CS}$ Negated Width	t_{ECSN}	20	—	ns
E6	Read Data Setup Time	t_{EDSR}	25	—	ns
E7	Read Data Hold Time	t_{EDHR}	5	—	ns
E8	ECLK Low to Data High Impedance	t_{EDHZ}	—	40	ns
E9	$\overline{CS}$ Negated to Data Hold (Read)	t_{ECDH}	0	—	ns
E10	$\overline{CS}$ Negated to Data High Impedance	t_{ECDZ}	—	1	t_{cyc}
E11	ECLK Low to Data Valid (Write)	t_{EDDW}	—	2	t_{cyc}
E12	ECLK Low to Data Hold (Write)	t_{EDHW}	5	—	ns
E13	Address Access Time (Read)[3]	t_{EACC}	255	—	ns
E14	Chip-Select Access Time (Read)[4]	t_{EACS}	195	—	ns
E15	Address Setup Time	t_{EAS}	—	1/2	t_{cyc}

NOTES:
1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.
2. When previous bus cycle is not an ECLK cycle, the address may be valid before ECLK goes low.
3. Address access time = $t_{Ecyc} - t_{EAD} - t_{EDSR}$.
4. Chip select access time = $t_{Ecyc} - t_{ECSD} - t_{EDSR}$.

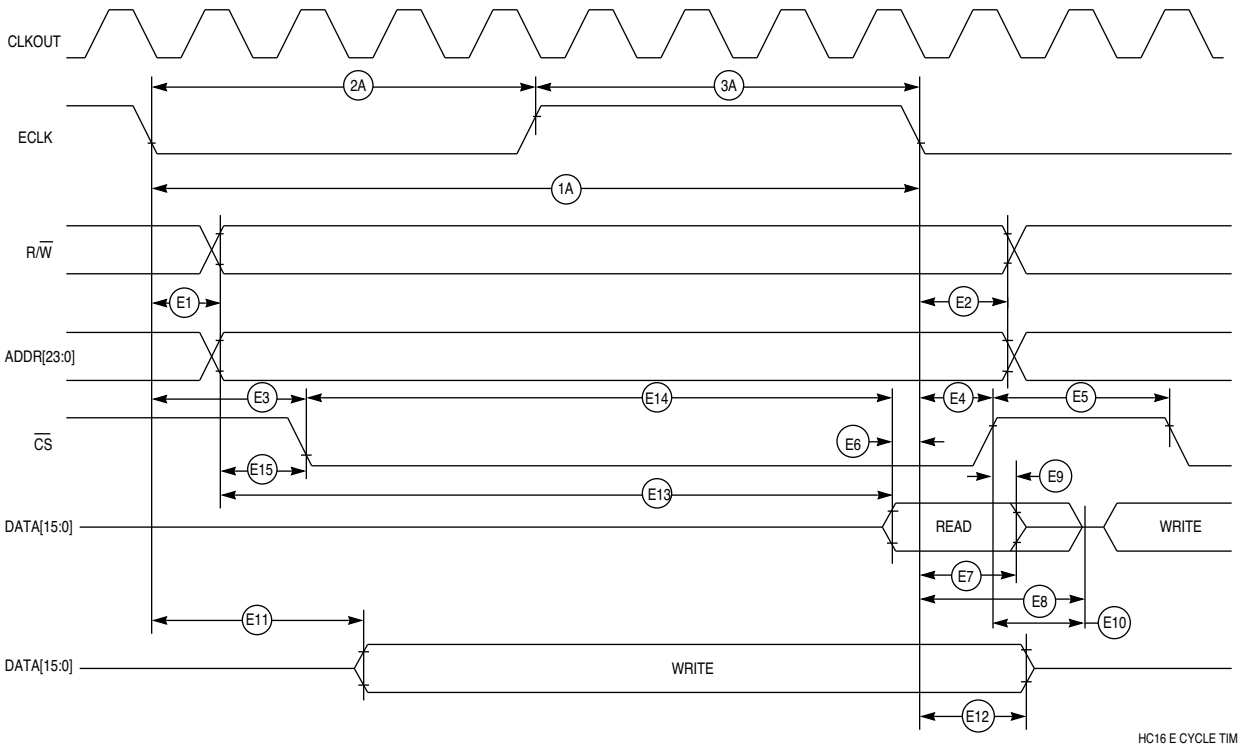


Figure A–15 ECLK Timing Diagram

Table A–9 QSPI Timing

(V_{DD} and V_{DDSYN} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, T_A = T_L to T_H , 200 pF load on all QSPI pins)[1]

Num	Function	Symbol	Min	Max	Unit
1	Operating Frequency Master Slave	f_{op}	DC DC	1/4 1/4	System Clock Frequency System Clock Frequency
2	Cycle Time Master Slave	t_{qcyc}	4 4	510 —	t_{cyc} t_{cyc}
3	Enable Lead Time Master Slave	t_{lead}	2 2	128 —	t_{cyc} t_{cyc}
4	Enable Lag Time Master Slave	t_{lag}	— 2	1/2 —	SCK t_{cyc}
5	Clock (SCK) High or Low Time Master Slave[2]	t_{sw}	2 t_{cyc} – 30 2 t_{cyc} – n	255 t_{cyc} —	ns ns
6	Sequential Transfer Delay Master Slave (Does Not Require Deselect)	t_{td}	17 13	8192 —	t_{cyc} t_{cyc}
7	Data Setup Time (Inputs) Master Slave	t_{su}	20 20	— —	ns ns
8	Data Hold Time (Inputs) Master Slave	t_{hi}	0 20	— —	ns ns
9	Slave Access Time	t_a	—	1	t_{cyc}
10	Slave MISO Disable Time	t_{dis}	—	2	t_{cyc}
11	Data Valid (after SCK Edge) Master Slave	t_v	— —	50 50	ns ns
12	Data Hold Time (Outputs) Master Slave	t_{ho}	0 0	— —	ns ns
13	Rise Time Input Output	t_{ri} t_{ro}	— —	2 30	µs ns
14	Fall Time Input Output	t_{fi} t_{fo}	— —	2 30	µs ns

NOTES:
1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.
2. For high time, n = External SCK rise time; for low time, n = External SCK fall time.

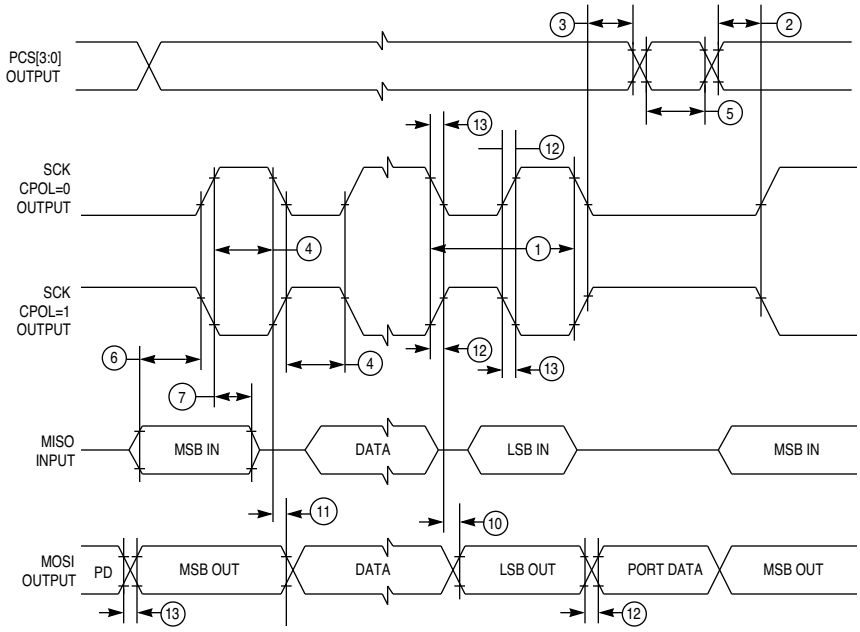


Figure A–16 QSPI Timing — Master, CPHA = 0

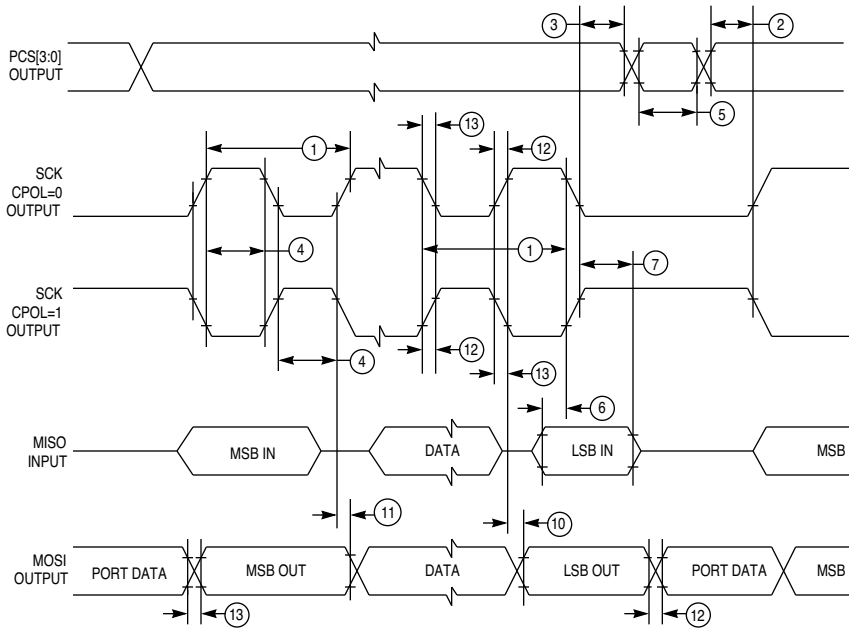
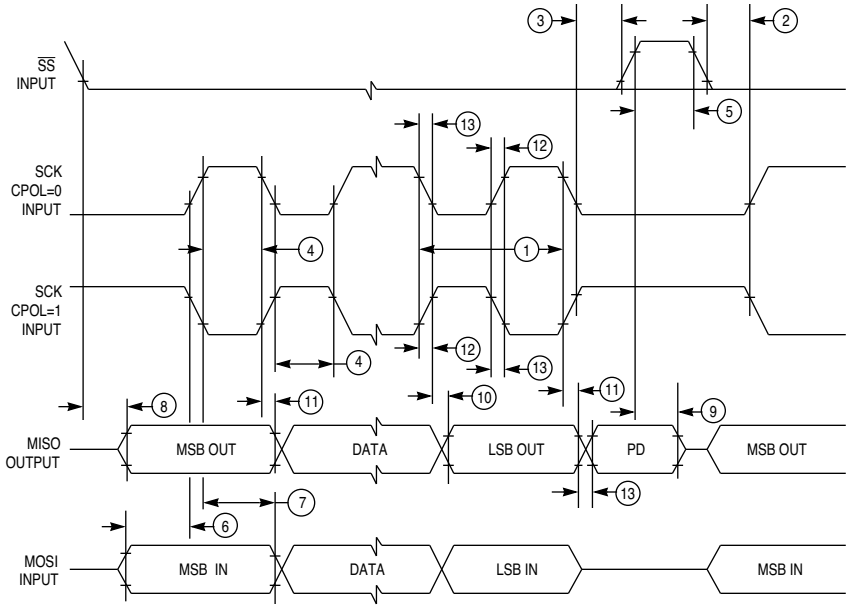
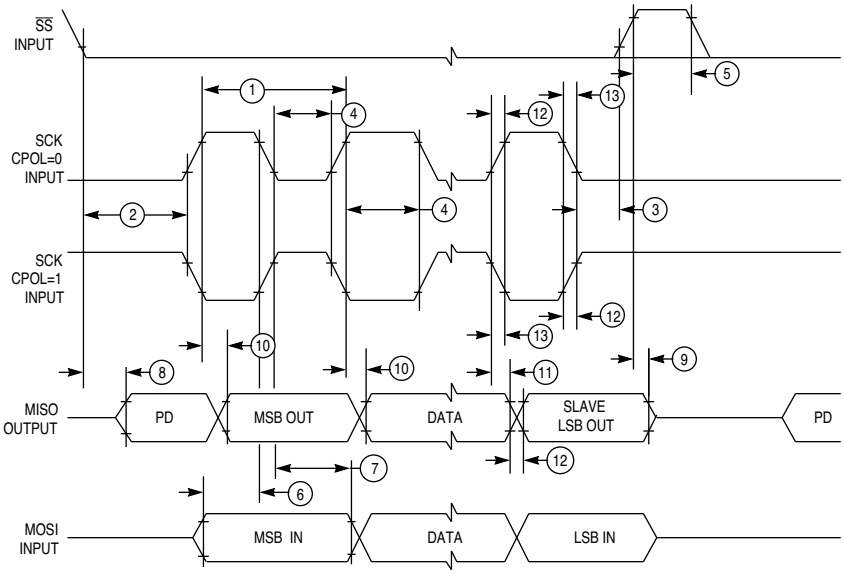


Figure A–17 QSPI Timing — Master, CPHA = 1



16 QSPI SLV CPHA0

Figure A–18 QSPI Timing — Slave, CPHA = 0



16 QSPI SLV CPHA1

Figure A–19 QSPI Timing — Slave, CPHA = 1

Table A–10 ADC Maximum Ratings

Num	Parameter	Symbol	Min	Max	Unit
1	Analog Supply	V_{DDA}	–0.3	6.5	V
2	Internal Digital Supply, with reference to V_{SSI}	V_{DDI}	–0.3	6.5	V
3	Reference Supply, with reference to V_{SSI}	V_{RH}, V_{RL}	–0.3	6.5	V
4	V_{SS} Differential Voltage	$V_{SSI} - V_{SSA}$	–0.1	0.1	V
5	V_{DD} Differential Voltage	$V_{DDI} - V_{DDA}$	–6.5	6.5	V
6	V_{REF} Differential Voltage	$V_{RH} - V_{RL}$	–6.5	6.5	V
7	V_{RH} to V_{DDA} Differential Voltage	$V_{RH} - V_{DDA}$	–6.5	6.5	V
8	V_{RL} to V_{SSA} Differential Voltage	$V_{RL} - V_{SSA}$	–6.5	6.5	V
9	Disruptive Input Current[1,2,3, 4, 5,6,7] $V_{NEGCLAMP} \cong -0.3$ V $V_{POSCLAMP} \cong 8$ V	I_{NA}	–500	500	µA
10	Positive Overvoltage Current Coupling Ratio[1, 5, 6, 8]	K_P	2000	—	—
11	Negative Overvoltage Current Coupling Ratio[1, 5, 6, 8]	K_N	500	—	—
12	Maximum Input Current [3, 4, 6] $V_{NEGCLAMP} \cong -0.3$ V $V_{POSCLAMP} \cong 8$ V	I_{MA}	–25	25	mA

NOTES:

1. Below disruptive current conditions, a stressed channel will store the maximum conversion value for analog inputs greater than V_{RH} and the minimum conversion value for inputs less than V_{RL}. This assumes that $V_{RH} \leq V_{DDA}$ and $V_{RL} \geq V_{SSA}$ due to the presence of the sample amplifier. Other channels are not affected by non-disruptive conditions
2. Input signals with large slew rates or high frequency noise components cannot be converted accurately. These signals also interfere with conversion of other channels.
3. Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.
4. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using positive and negative clamp values, then use the larger of the calculated values.
5. This parameter is periodically sampled rather than 100% tested.
6. Applies to single pin only.
7. The values of external system components can change the maximum input current value, and affect operation. A voltage drop may occur across the external source impedances of the adjacent pins, impacting conversions on these adjacent pins. The actual maximum may need to be determined by testing the complete design.
8. Current coupling is the ratio of the current induced from overvoltage (positive or negative, through an external series coupling resistor), divided by the current induced on adjacent pins. A voltage drop may occur across the external source impedances of the adjacent pins, impacting conversions on these adjacent pins

Table A–11 ADC DC Electrical Characteristics (Operating)

(V_{SS} = 0 Vdc, ADCLK = 2.1 MHz, $T_A = T_L$ to T_H)

Num	Parameter	Symbol	Min	Max	Unit
1	Analog Supply[1]	V_{DDA}	4.5	5.5	V
2	Internal Digital Supply[1]	V_{DDI}	4.5	5.5	V
3	V_{SS} Differential Voltage	$V_{SSI} - V_{SSA}$	– 1.0	1.0	mV
4	V_{DD} Differential Voltage	$V_{DDI} - V_{DDA}$	– 1.0	1.0	V
5	Reference Voltage Low[2, 3]	V_{RL}	V_{SSA}	V_{DDA} / 2	V
6	Reference Voltage High[2, 3]	V_{RH}	V_{DDA} / 2	V_{DDA}	V
7	V_{REF} Differential Voltage[3]	$V_{RH} - V_{RL}$	4.5	5.5	V
8	Input Voltage[2]	V_{INDC}	V_{SSA}	V_{DDA}	V
9	Input High, Port ADA	V_{IH}	0.7 (V_{DDA})	V_{DDA} + 0.3	V
10	Input Low, Port ADA	V_{IL}	V_{SSA} – 0.3	0.2 (V_{DDA})	V
11	Analog Supply Current Normal Operation[4] Low-power stop	I_{DDA}	 — —	 1.0 200	 mA µA
12	Reference Supply Current	I_{REF}	—	250	µA
13	Input Current, Off Channel[5]	I_{OFF}	—	150	nA
14	Total Input Capacitance, Not Sampling	C_{INN}	—	10	pF
15	Total Input Capacitance, Sampling	C_{INS}	—	15	pF

NOTES:
1. Refers to operation over full temperature and frequency range.
2. To obtain full-scale, full-range results, $V_{SSA} \le V_{RL} \le V_{INDC} \le V_{RH} \le V_{DDA}$.
3. Accuracy tested and guaranteed at $V_{RH} - V_{RL}$ = 5.0 V ± 5%.
4. Current measured at maximum system clock frequency with ADC active.
5. Maximum leakage occurs at maximum operating temperature. Current decreases by approximately one-half for each 10°C decrease from maximum temperature.

Table A–12 ADC AC Characteristics (Operating)

(V_{DD} and V_{DDA} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, T_A within operating temperature range)

Num	Parameter	Symbol	Min	Max	Unit
1	ADC Clock Frequency	f_{adclk}	0.5	2.1	MHz
2	8-bit Conversion Time[1] F_{ADCLK} = 1.0 MHz F_{ADCLK} = 2.1 MHz	t_{conv}	 15.2 7.6	—	µs
3	10-bit Conversion Time[1] F_{ADCLK} = 1.0 MHz F_{ADCLK} = 2.1 MHz	t_{conv}	 17.1 8.6	—	µs
4	Stop Recovery Time	t_{sr}	—	10	µs

NOTES:
1. Conversion accuracy varies with f_{adclK} rate. Reduced conversion accuracy occurs at maximum.

Table A–13 ADC Conversion Characteristics (Operating)

(V_{DD} and V_{DDA} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, T_A = T_L to T_H,
0.5 MHz ≤ f_{adclk} ≤ 1.0 MHz, 2 clock input sample time)

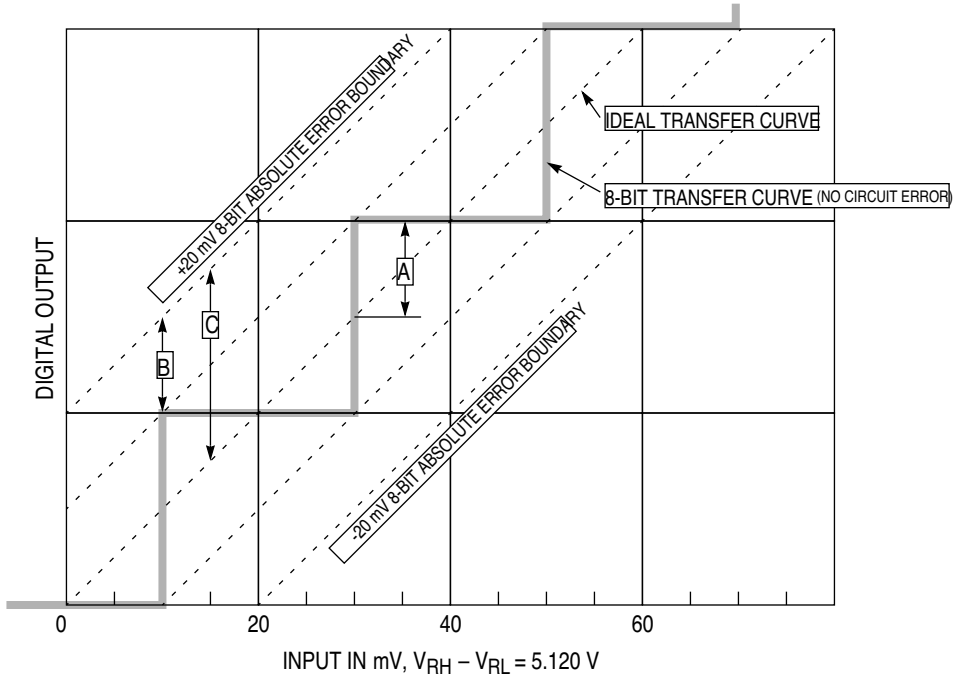
Num	Parameter	Symbol	Min	Typ	Max	Unit
1	8-bit Resolution[1]	1 Count	—	20	—	mV
2	8-bit Differential Nonlinearity	DNL	–0.5	—	0.5	Counts
3	8-bit Integral Nonlinearity	INL	–1	—	1	Counts
4	8-bit Absolute Error[2]	AE	–1	—	1	Counts
5	10-bit Resolution[1]	1 Count	—	5	—	mV
6	10-bit Differential Nonlinearity[3]	DNL	–0.5	—	0.5	Counts
7	10-bit Integral Nonlinearity[3]	INL	–2.0	—	2.0	Counts
8	10-bit Absolute Error[3, 4]	AE	–2.5	—	2.5	Counts
9	Source Impedance at Input[5]	R_S	—	20	—	kΩ

NOTES:

1. At V_{RH} –V_{RL}= 5.12 V, one 10-bit count = 5 mV and one 8-bit count = 20 mV.
2. 8-bit absolute error of 1 count (20 mV) includes 1/2 count (10 mV) inherent quantization error and 1/2 count (10 mV) circuit (differential, integral, and offset) error.
3. Conversion accuracy varies with f_{adclk} rate. Reduced conversion accuracy occurs at maximum F_{AD-CLK}. Assumes that minimum sample time (2 ADC Clocks) is selected.
4. 10-bit absolute error of 2.5 counts (12.5 mV) includes 1/2 count (2.5 mV) inherent quantization error and 2 counts (10 mV) circuit (differential, integral, and offset) error.
5. Maximum source impedance is application-dependent. Error resulting from pin leakage depends on junction leakage into the pin and on leakage due to charge-sharing with internal capacitance.
   Error from junction leakage is a function of external source impedance and input leakage current. In the following expression, expected error in result value due to junction leakage (V_{errj}) is expressed:

$$V_{errj} = R_S \times I_{OFF}$$

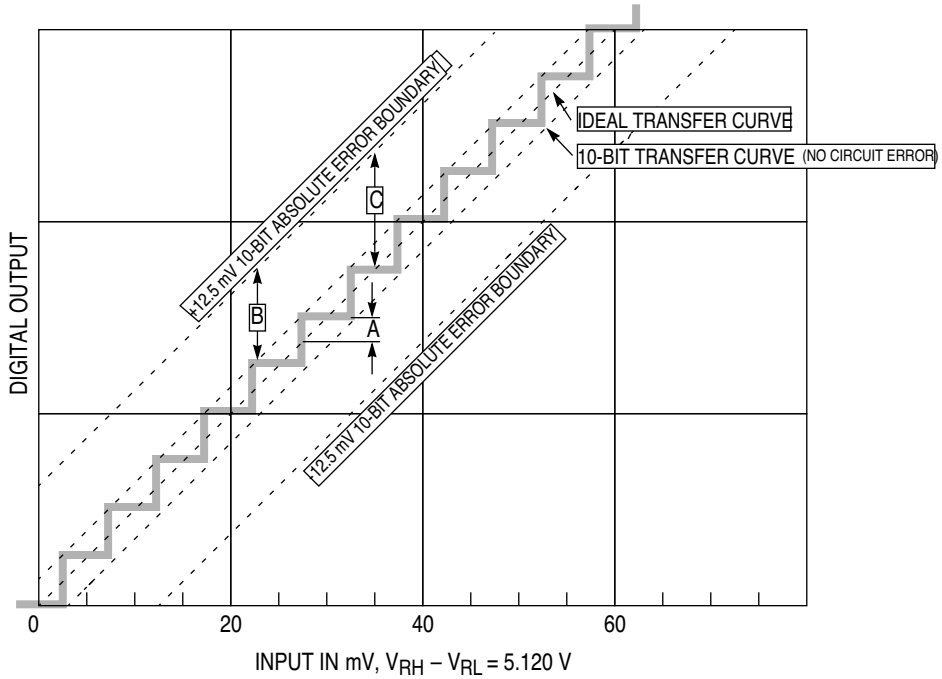
   where I_{OFF} is a function of operating temperature, as shown in table A-11.
   Charge-sharing leakage is a function of input source impedance, conversion rate, change in voltage between successive conversions, and the size of the decoupling capacitor used. Error levels are best determined empirically. In general, continuous conversion of the same channel may not be compatible with high source impedance.



A – +1/2 COUNT (10 mV) INHERENT QUANTIZATION ERROR
B – CIRCUIT-CONTRIBUTED +10 mV ERROR
C – + 20 mV ABSOLUTE ERROR (ONE 8-BIT COUNT)

ADC 8-BIT ACCURACY

Figure A–20 8-Bit ADC Conversion Accuracy



A – +.5 COUNT (2.5 mV) INHERENT QUANTIZATION ERROR
B – CIRCUIT-CONTRIBUTED +10 mV ERROR
C – +12.5 mV ABSOLUTE ERROR (2.5 10-BIT COUNTS)

ADC 10-BIT ACCURACY

Figure A–21 10-Bit ADC Conversion Accuracy