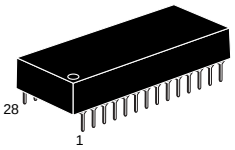
M48Z08
M48Z18

5V, 64 Kbit (8Kb x 8) ZEROPOWER® SRAM

FEATURES SUMMARY

- INTEGRATED, ULTRA LOW POWER SRAM AND POWER-FAIL CONTROL CIRCUIT
- UNLIMITED WRITE CYCLES
- READ CYCLE TIME EQUALS WRITE CYCLE TIME
- AUTOMATIC POWER-FAIL CHIP DESELECT AND WRITE PROTECTION
- WRITE PROTECT VOLTAGES
  (V_{PFD} = Power-fail Deselect Voltage):
  - M48Z08: V_{CC} = 4.75 to 5.5V
    $4.5V \le V_{PFD} \le 4.75V$
  - M48Z18: V_{CC} = 4.5 to 5.5V
    $4.2V \le V_{PFD} \le 4.5V$
- SELF-CONTAINED BATTERY IN THE CAPHAT™ DIP PACKAGE
- PIN AND FUNCTION COMPATIBLE WITH JEDEC STANDARD 8K x 8 SRAMs
- RoHS COMPLIANCE
  Lead-free components are compliant with the RoHS Directive.

Figure 1. 28-pin CAPHAT, DIP Package



PCDIP28 (PC)
Battery CAPHAT™

SUMMARY DESCRIPTION

The M48Z08/18 ZEROPOWER® RAM is a 8K x 8 non-volatile static RAM which is pin and functional compatible with the DS1225.

The monolithic chip is available in two special packages to provide a highly integrated battery backed-up memory solution.

The M48Z08/18 is a non-volatile pin and function equivalent to any JEDEC standard 8K x 8 SRAM.

It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The 28-pin, 600mil DIP CAPHAT™ houses the M48Z08/18 silicon with a long life lithium button cell in a single package.

Figure 2. Logic Diagram

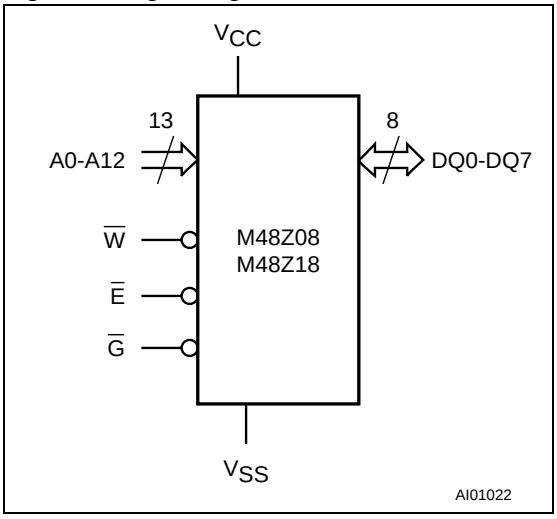


Figure 3. DIP Connections

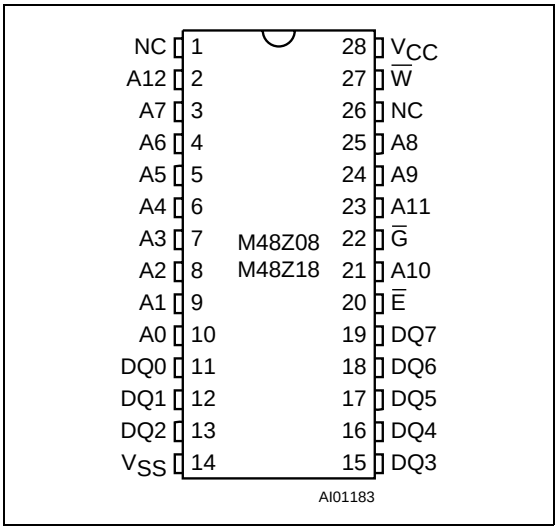


Table 1. Signal Names

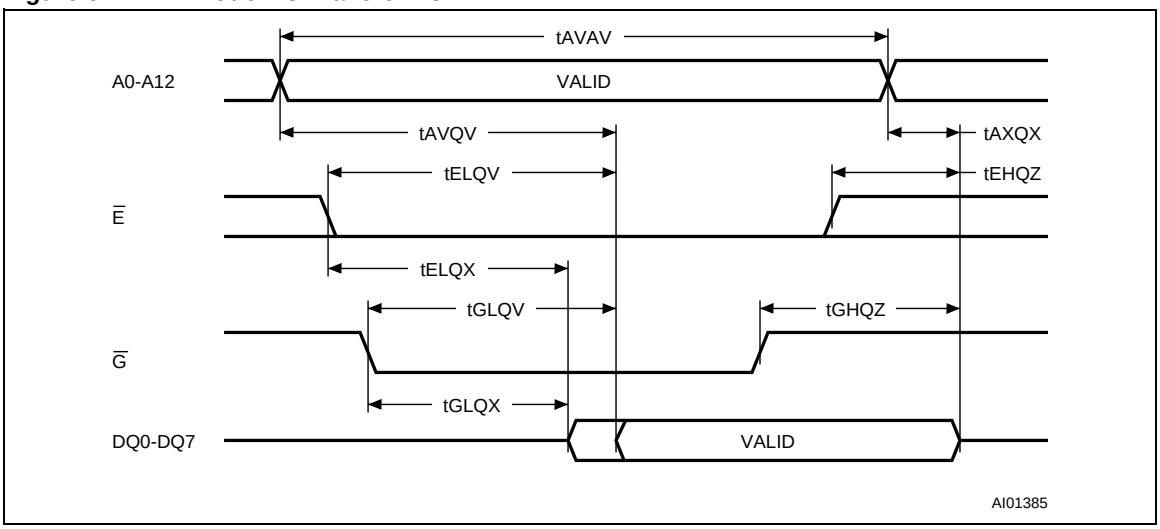
A0-A12	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	WRITE Enable
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally

READ Mode

The M48Z08/18 is in the READ Mode whenever $\overline{W}$ (WRITE Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 65,536 locations in the static storage array. Thus, the unique address specified by the 13 address inputs defines which one of the 8,192 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within address access time (t_{AVQV}) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access time (t_{ELQV}) or Output Enable Access time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the address inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for Output Data Hold time (t_{AXQX}) but will go indeterminate until the next address access.

Figure 5. READ Mode AC Waveforms



Note: WRITE Enable ($\overline{W}$) = High.

Table 3. READ Mode AC Characteristics

Symbol	Parameter[1]	M48Z08/M48Z18		Unit
		Min	Max	
t_{AVAV}	READ Cycle Time	100		ns
t_{AVQV}	Address Valid to Output Valid		100	ns
t_{ELQV}	Chip Enable Low to Output Valid		100	ns
t_{GLQV}	Output Enable Low to Output Valid		50	ns
t_{ELQX}[2]	Chip Enable Low to Output Transition	10		ns
t_{GLQX}[2]	Output Enable Low to Output Transition	5		ns
t_{EHQZ}[2]	Chip Enable High to Output Hi-Z		50	ns
t_{GHQZ}[2]	Output Enable High to Output Hi-Z		40	ns
t_{AXQX}	Address Transition to Output Transition	5		ns

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{CC} = 4.75 to 5.5V or 4.5 to 5.5V (except where noted).
2. C_L = 30pF.

Table 4. WRITE Mode AC Characteristics

Symbol	Parameter[1]	M48Z08/M48Z18		Unit
		Min	Max	
t_{AVAV}	WRITE Cycle Time	100		ns
t_{AVWL}	Address Valid to WRITE Enable Low	0		ns
t_{AVEL}	Address Valid to Chip Enable 1 Low	0		ns
t_{WLWH}	WRITE Enable Pulse Width	80		ns
t_{ELEH}	Chip Enable Low to Chip Enable 1 High	80		ns
t_{WHAX}	WRITE Enable High to Address Transition	10		ns
t_{EHAX}	Chip Enable High to Address Transition	10		ns
t_{DVWH}	Input Valid to WRITE Enable High	50		ns
t_{DVEH}	Input Valid to Chip Enable 1 High	30		ns
t_{WHDX}	WRITE Enable High to Input Transition	5		ns
t_{EHDX}	Chip Enable High to Input Transition	5		ns
t_{WLQZ}[2,3]	WRITE Enable Low to Output Hi-Z		50	ns
t_{AVWH}	Address Valid to WRITE Enable High	80		ns
t_{AVEH}	Address Valid to Chip Enable High	80		ns
t_{WHQX}[2,3]	WRITE Enable High to Output Transition	10		ns

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{CC} = 4.75 to 5.5V or 4.5 to 5.5V (except where noted).
2. C_L = 30pF.
3. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

MAXIMUM RATING

Stressing the device above the rating listed in the "Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 5. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off, Oscillator Off)	–40 to 85	°C
T_{SLD}(1)	Lead Solder Temperature for 10 seconds	260	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
I_O	Output Current	20	mA
P_D	Power Dissipation	1	W

Note: 1. For DIP package: Soldering temperature not to exceed 260°C for 10 seconds (total thermal budget not to exceed 150°C for longer than 30 seconds).

CAUTION: *Negative undershoots below –0.3V are not allowed on any pin while in the Battery Back-up mode.*

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 6. Operating and AC Measurement Conditions

Parameter	M48Z08	M48Z18	Unit
Supply Voltage (V_{CC})	4.75 to 5.5	4.5 to 5.5	V
Ambient Operating Temperature (T_A)	0 to 70	0 to 70	°C
Load Capacitance (C_L)	100	100	pF
Input Rise and Fall Times	≤ 5	≤ 5	ns
Input Pulse Voltages	0 to 3	0 to 3	V
Input and Output Timing Ref. Voltages	1.5	1.5	V

Note: Output Hi-Z is defined as the point where data is no longer driven.

Figure 9. AC Testing Load Circuit

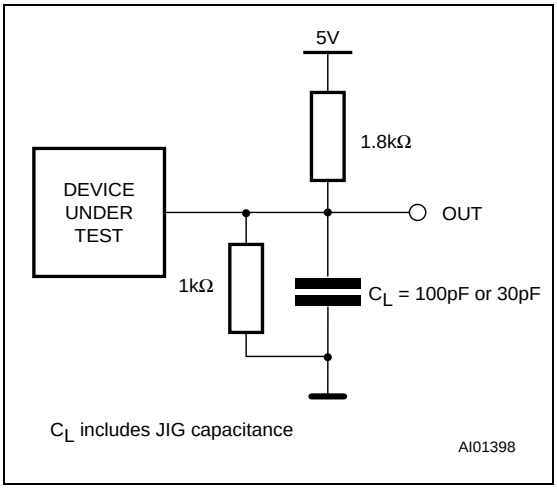


Table 7. Capacitance

Symbol	Parameter[1,2]	Min	Max	Unit
C_{IN}	Input Capacitance		10	pF
C_{IO}[3]	Input / Output Capacitance		10	pF

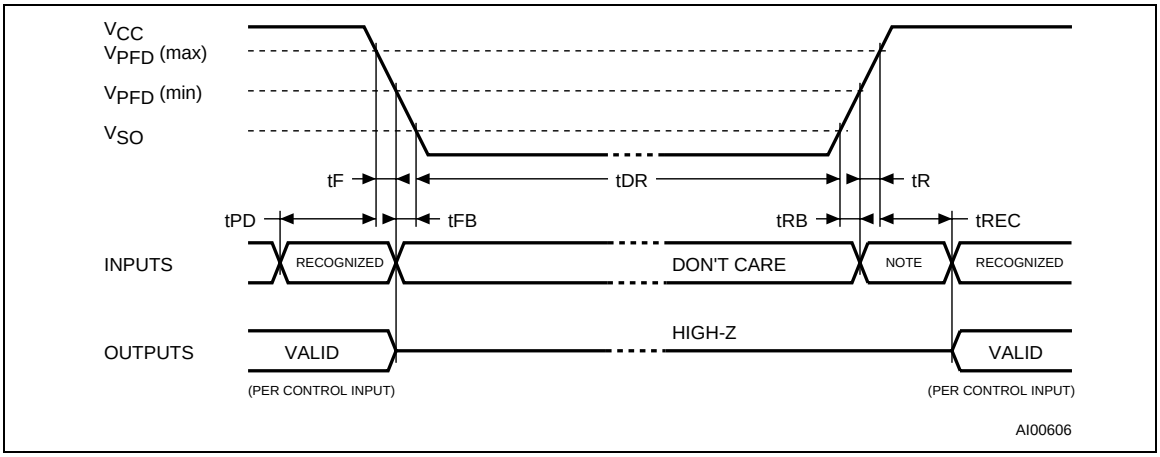
Note: 1. Effective capacitance measured with power supply at 5V; sampled only, not 100% tested.
2. At 25°C, f = 1MHz.
3. Outputs deselected.

Table 8. DC Characteristics

Symbol	Parameter	Test Condition(1)	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}(2)	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±1	µA
I_{CC}	Supply Current	Outputs open		80	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		3	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} - 0.2V$		3	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{CC} = 4.75 to 5.5V or 4.5 to 5.5V (except where noted).
2. Outputs deselected.

Figure 10. Power Down/Up Mode AC Waveforms



Note: Inputs may or may not be recognized at this time. Caution should be taken to keep $\overline{E}$ high as V_{CC} rises past V_{PFD} (min). Some systems may perform inadvertent WRITE cycles after V_{CC} rises above V_{PFD} (min) but before normal system operations begin. Even though a power on reset is being applied to the processor, a reset condition may not occur until after the system is running.

Table 9. Power Down/Up AC Characteristics

Symbol	Parameter(1)	Min	Max	Unit
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		µs
t_F(2)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB}(3)	V_{PFD} (min) to V_{SS} V_{CC} Fall Time	10		µs
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} Rise Time	0		µs
t_{RB}	V_{SS} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{rec}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Up	2		ms

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{CC} = 4.75 to 5.5V or 4.5 to 5.5V (except where noted).
2. V_{PFD} (max) to V_{PFD} (min) fall time of less than tF may result in deselection/write protection not occurring until 200µs after V_{CC} passes V_{PFD} (min).
3. V_{PFD} (min) to V_{SS} fall time of less than t_{FB} may cause corruption of RAM data.

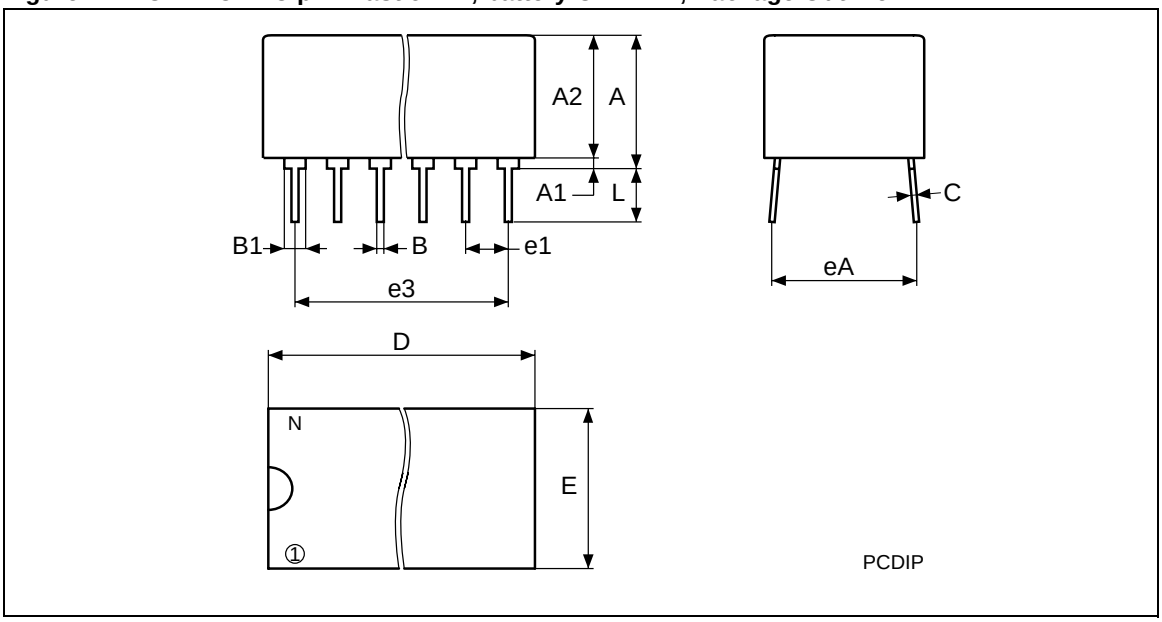
Table 10. Power Down/Up Trip Points DC Characteristics

Symbol	Parameter(1,2)		Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage	M48Z08	4.5	4.6	4.75	V
		M48Z18	4.2	4.3	4.5	V
V_{SO}	Battery Back-up Switchover Voltage			3.0		V
t_{DR}(3)	Expected Data Retention Time		11			YEARS

Note: 1. All voltages referenced to V_{SS}.
2. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{CC} = 4.75 to 5.5V or 4.5 to 5.5V (except where noted).
3. At 25°C, V_{CC} = 0V.

PACKAGE MECHANICAL INFORMATION

Figure 11. PCDIP28 – 28-pin Plastic DIP, battery CAPHAT, Package Outline



Note: Drawing is not to scale.

Table 11. PCDIP28 – 28-pin Plastic DIP, battery CAPHAT, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.38	8.89		0.330	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		39.37	39.88		1.550	1.570
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3		29.72	36.32		1.170	1.430
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N	28			28		

PART NUMBERING

Table 12. Ordering Information Scheme

Example: M48Z 08 –100 PC 1 TR

Device Type

M48Z

Supply Voltage and Write Protect Voltage

08(1) = V_{CC} = 4.75 to 5.5V; V_{PFD} = 4.5 to 4.75V

18 = V_{CC} = 4.5 to 5.5V; V_{PFD} = 4.2 to 4.5V

Speed

–100 = 100ns

Package

PC = PCDIP28

Temperature Range

1 = 0 to 70°C

Shipping Method

blank = ECOPACK Package, Tubes

TR = ECOPACK Package, Tape & Reel

Note: 1. The M48Z08/18 part is offered with the PCDIP28 (e.g., CAPHAT™) package only.

For other options, or for more information on any aspect of this device, please contact the ST Sales Office nearest you.