1. Features

- **Low-voltage and Standard-voltage Operation**
  - **1.8 (V_{CC} = 1.8V to 5.5V)**
- **Internal Organization**
  - **64 x 16**
- **Three-wire Serial Interface**
- **2 MHz Clock Rate (5V) Compatibility**
- **Self-timed Write Cycle (5 ms max)**
- **High Reliability**
  - **Endurance: 1 Million Write Cycles**
  - **Data Retention: 100 Years**
- **8-lead PDIP, 8-lead JEDEC SOIC, and 8-lead TSSOP Packages**
- **Lead-free/Halogen-free Devices**

2. Description

The AT93C46E provides 1024 bits of serial electrically-erasable programmable read-only memory (EEPROM) organized as 64 words of 16 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The AT93C46E is available in space-saving 8-lead PDIP, 8-lead JEDEC SOIC, and 8-lead TSSOP packages.

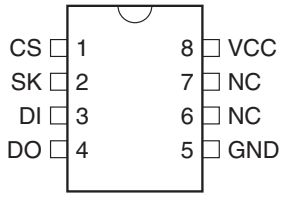
The AT93C46E is enabled through the Chip Select pin (CS) and accessed via a three-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a Read instruction at DI, the address is decoded and the data is clocked out serially on the data output DO pin. The write cycle is completely self-timed and no separate erase cycle is required before write. The write cycle is only enabled when the part is in the erase/write enable state. When CS is brought high following the initiation of a write cycle, the DO pin outputs the ready/busy status of the part.

The AT93C46E is available in 1.8V (1.8V to 5.5V) version.

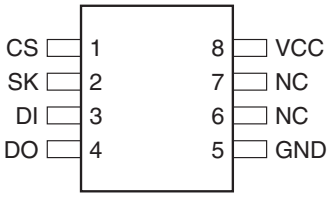
Table 2-1. Pin Configuration

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
VCC	Power Supply
NC	No Connect

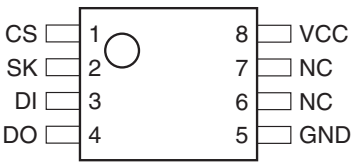
8-lead PDIP



8-lead SOIC



8-lead TSSOP



Three-wire Serial EEPROM

1K (64 x 16)

AT93C46E

Absolute Maximum Ratings*

Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 2-1. Block Diagram

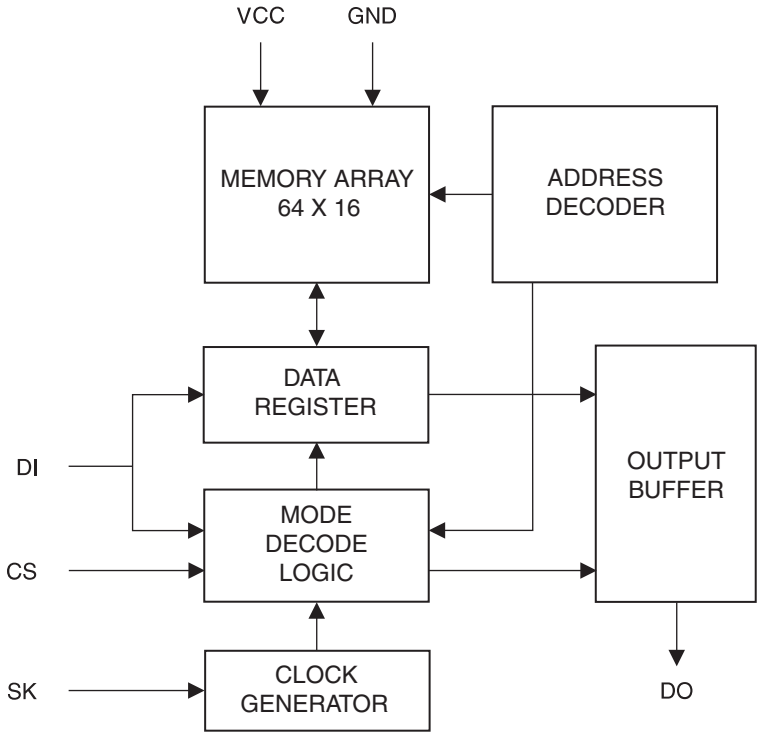


Table 2-2. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0V (unless otherwise noted)

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance (CS, SK, DI)	5	pF	V_{IN} = 0V

Note: This parameter is characterized and is not 100% tested.

Table 2-3. DC Characteristics

Applicable over recommended operating range from: T_{AI} = –40°C to +85°C, V_{CC} = +1.8V to +5.5V, (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.8		5.5	V
V_{CC2}	Supply Voltage			2.7		5.5	V
V_{CC3}	Supply Voltage			4.5		5.5	V
I_{CC}	Supply Current	V_{CC} = 5.0V	Read at 1.0 MHz		0.5	2.0	mA
			Write at 1.0 MHz		0.5	2.0	mA
I_{SB1}	Standby Current	V_{CC} = 1.8V	CS = 0V		0.4	1.0	µA
I_{SB2}	Standby Current	V_{CC} = 2.7V	CS = 0V		6.0	10.0	µA
I_{SB3}	Standby Current	V_{CC} = 5.0V	CS = 0V		10.0	15.0	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}			0.1	1.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}			0.1	1.0	µA
V_{IL1}(1) V_{IH1}(1)	Input Low Voltage Input High Voltage	2.7V ≤ V_{CC} ≤ 5.5V		–0.6 2.0		0.8 V_{CC} + 1	V
V_{IL2}(1) V_{IH2}(1)	Input Low Voltage Input High Voltage	1.8V ≤ V_{CC} ≤ 2.7V		–0.6 V_{CC} x 0.7		V_{CC} x 0.3 V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	2.7V ≤ V_{CC} ≤ 5.5V	I_{OL} = 2.1 mA			0.4	V
			I_{OH} = –0.4 mA	2.4			V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	1.8V ≤ V_{CC} ≤ 2.7V	I_{OL} = 0.15 mA			0.2	V
			I_{OH} = –100 µA	V_{CC} – 0.2			V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

Table 2-4. AC Characteristics

Applicable over recommended operating range from T_A = –40°C to + 85°C, V_{CC} = +2.7V to + 5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
f_{SK}	SK Clock Frequency	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		0 0 0		2 1 0.25	MHz
t_{SKH}	SK High Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		250 250 1000			ns
t_{SKL}	SK Low Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		250 250 1000			ns
t_{CS}	Minimum CS Low Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		250 250 1000			ns
t_{CSS}	CS Setup Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	50 50 200			ns
t_{DIS}	DI Setup Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	100 100 400			ns
t_{CSH}	CS Hold Time	Relative to SK		0			ns
t_{DIH}	DI Hold Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	100 100 400			ns
t_{PD1}	Output Delay to “1”	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			250 250 1000	ns
t_{PD0}	Output Delay to “0”	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			250 250 1000	ns
t_{SV}	CS to Status Valid	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			250 250 1000	ns
t_{DF}	CS to DO in High Impedance	AC Test CS = V_{IL}	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			100 150 400	ns
t_{WP}	Write Cycle Time			0.1	3	5	ms
Endurance(1)	5.0V, 25°C			1M			Write Cycle

Note: 1. This parameter is ensured by characterization.

3. Functional Description

The AT93C46E is accessed via a simple and versatile three-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. ***A valid instruction starts with a rising edge of CS*** and consists of a start bit (logic “1”) followed by the appropriate op code and the desired memory address location.

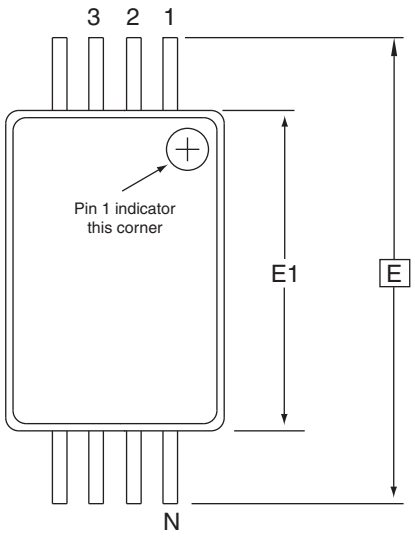
AT93C46E Ordering Information

Ordering Code	Package	Operation Range
AT93C46E-PU (Bulk Form only)	8P3	Lead-free/Halogen-free/ Industrial Temperature (–40°C to 85°C)
AT93C46EN-SH-B[1] (NiPdAu Lead Finish)	8S1	
AT93C46EN-SH-T[2] (NiPdAu Lead Finish)	8S1	
AT93C46E-TH-B[1] (NiPdAu Lead Finish)	8A2	
AT93C46E-TH-T[2] (NiPdAu Lead Finish)	8A2	

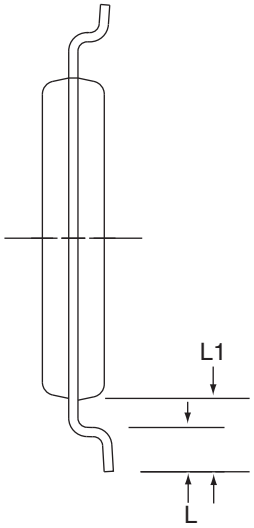
Notes: 1. “B” denotes bulk.
2. “-T” denotes tape and reel. SOIC = 4K per reel. TSSOP = 5K per reel.

Package Type	
8P3	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8A2	8-lead, 0.170" Wide, Thin Small Outline Package (TSSOP)
Options	
–1.8	Low Voltage (1.8V to 5.5V)

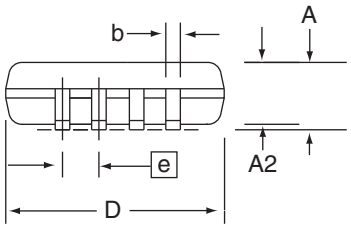
8A2 - TSSOP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
A	–	–	1.20	
A2	0.80	1.00	1.05	
b	0.19	–	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 RE3		

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
5. Dimension D and E1 to be determined at Datum Plane H.

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**8A2,** 8-lead, 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	TNR	8A2	C