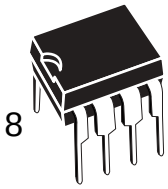
M93S66, M93S56
M93S46

4Kbit, 2Kbit and 1Kbit (16-bit wide)
MICROWIRE Serial Access EEPROM with Block Protection

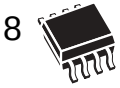
FEATURES SUMMARY

- Industry Standard MICROWIRE Bus
- Single Supply Voltage:
  - 4.5 to 5.5V for M93Sx6
  - 2.5 to 5.5V for M93Sx6-W
  - 1.8 to 5.5V for M93Sx6-R
- Single Organization: by Word (x16)
- Programming Instructions that work on: Word or Entire Memory
- Self-timed Programming Cycle with Auto-Erase
- User Defined Write Protected Area
- Page Write Mode (4 words)
- Ready/$\overline{\text{Busy}}$ Signal During Programming
- Speed:
  - 1MHz Clock Rate, 10ms Write Time (Current product, identified by process identification letter F or M)
  - 2MHz Clock Rate, 5ms Write Time (New Product, identified by process identification letter W or G)
- Sequential Read Operation
- Enhanced ESD/Latch-Up Behavior
- More than 1 Million Erase/Write Cycles
- More than 40 Year Data Retention

Figure 1. Packages



PDIP8 (BN)



SO8 (MN)
150 mil width

TSSOP8 (DS)
3x3mm body size

TSSOP8 (DW)
169 mil width

SUMMARY DESCRIPTION

This specification covers a range of 4K, 2K, 1K bit serial Electrically Erasable Programmable Memory (EEPROM) products (respectively for M93S66, M93S56, M93S46). In this text, these products are collectively referred to as M93Sx6.

Figure 2. Logic Diagram

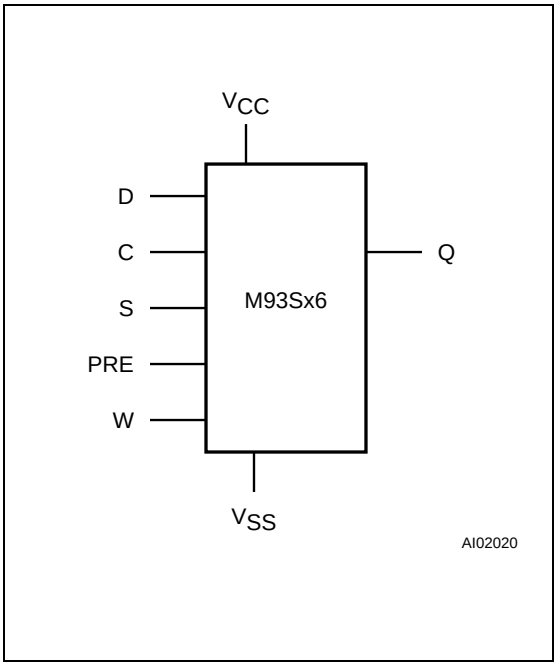


Table 1. Signal Names

S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
PRE	Protection Register Enable
W	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

The M93Sx6 is accessed through a serial input (D) and output (Q) using the MICROWIRE bus protocol. The memory is divided into 256, 128, 64 x16 bit words (respectively for M93S66, M93S56, M93S46).

The M93Sx6 is accessed by a set of instructions which includes Read, Write, Page Write, Write All and instructions used to set the memory protection. These are summarized in Table 2. and Table 3.).

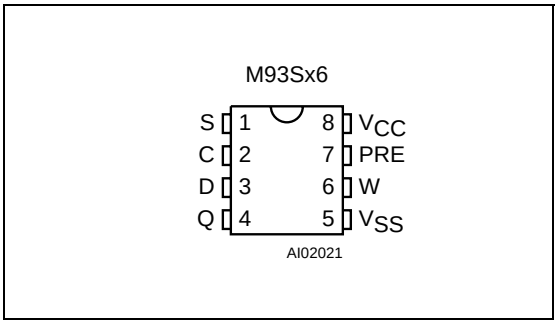
A Read Data from Memory (READ) instruction loads the address of the first word to be read into an internal address pointer. The data contained at this address is then clocked out serially. The address pointer is automatically incremented after the data is output and, if the Chip Select Input (S) is held High, the M93Sx6 can output a sequential stream of data words. In this way, the memory can be read as a data stream from 16 to 4096 bits (for the M93S66), or continuously as the address counter automatically rolls over to 00h when the highest address is reached.

Within the time required by a programming cycle (t_W), up to 4 words may be written with help of the Page Write instruction. the whole memory may also be erased, or set to a predetermined pattern, by using the Write All instruction.

Within the memory, a user defined area may be protected against further Write instructions. The size of this area is defined by the content of a Protection Register, located outside of the memory array. As a final protection step, data may be permanently protected by programming a One Time Programming bit (OTP bit) which locks the Protection Register content.

Programming is internally self-timed (the external clock signal on Serial Clock (C) may be stopped or left running after the start of a Write cycle) and does not require an erase cycle prior to the Write instruction. The Write instruction writes 16 bits at a time into one of the word locations of the M93Sx6, the Page Write instruction writes up to 4 words of 16 bits to sequential locations, assuming in both cases that all addresses are outside the Write Protected area. After the start of the programming cycle, a Busy/Ready signal is available on Serial Data Output (Q) when Chip Select Input (S) is driven High.

Figure 3. DIP, SO and TSSOP Connections



Note: See PACKAGE MECHANICAL section for package dimensions, and how to identify pin-1.

An internal Power-on Data Protection mechanism in the M93Sx6 inhibits the device when the supply is too low.

POWER-ON DATA PROTECTION

To prevent data corruption and inadvertent write operations during power-up, a Power-On Reset (POR) circuit resets all internal programming circuitry, and sets the device in the Write Disable mode.

– At Power-up and Power-down, the device must *not* be selected (that is, Chip Select Input (S) must be driven Low) until the supply voltage reaches the operating value V_{CC} specified in Table 5. to Table 6..

– When V_{CC} reaches its valid level, the device is properly reset (in the Write Disable mode) and is ready to decode and execute incoming instructions.

For the M93Sx6 devices (5V range) the POR threshold voltage is around 3V. For the M93Sx6-W (3V range) and M93Sx6-R (2V range) the POR threshold voltage is around 1.5V.

INSTRUCTIONS

The instruction set of the M93Sx6 devices contains seven instructions, as summarized in Table 2. to Table 3.. Each instruction consists of the following parts, as shown in Figure 4.:

- Each instruction is preceded by a rising edge on Chip Select Input (S) with Serial Clock (C) being held Low.
- A start bit, which is the first '1' read on Serial Data Input (D) during the rising edge of Serial Clock (C).
- Two op-code bits, read on Serial Data Input (D) during the rising edge of Serial Clock (C). (Some instructions also use the first two bits of the address to define the op-code).
- The address bits of the byte or word that is to be accessed. For the M93S46, the address is made up of 6 bits (see Table 2.). For the M93S56 and M93S66, the address is made up of 8 bits (see Table 3.).

The M93Sx6 devices are fabricated in CMOS technology and are therefore able to run as slow as 0 Hz (static input signals) or as fast as the maximum ratings specified in Table 16. to Table 19..

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage Temperature	–65	150	°C
T_{LEAD}	Lead Temperature during Soldering	See note [1]		°C
V_{OUT}	Output range (Q = V_{OH} or Hi-Z)	–0.50	V_{CC}+0.5	V
V_{IN}	Input range	–0.50	V_{CC}+1	V
V_{CC}	Supply Voltage	–0.50	6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [2]	–4000	4000	V

Note: 1. Compliant with JEDEC Std J-STD-020B (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU
2. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω)

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 5. Operating Conditions (M93Sx6)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
T_A	Ambient Operating Temperature (Device Grade 6)	–40	85	°C
	Ambient Operating Temperature (Device Grade 3)	–40	125	°C

Table 6. Operating Conditions (M93Sx6-W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	2.5	5.5	V
T_A	Ambient Operating Temperature (Device Grade 6)	–40	85	°C

Table 7. Operating Conditions (M93Sx6-R)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	1.8	5.5	V
T_A	Ambient Operating Temperature (Device Grade 6)	–40	85	°C

Table 8. AC Measurement Conditions (M93Sx6)

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance	100		pF
	Input Rise and Fall Times		50	ns
	Input Pulse Voltages	0.4 V to 2.4 V		V
	Input Timing Reference Voltages	1.0 V and 2.0 V		V
	Output Timing Reference Voltages	0.8 V and 2.0 V		V

Note: Output Hi-Z is defined as the point where data out is no longer driven.

Table 9. AC Measurement Conditions (M93Sx6-W and M93Sx6-R)

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance	100		pF
	Input Rise and Fall Times		50	ns
	Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V
	Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V

Note: Output Hi-Z is defined as the point where data out is no longer driven.

Figure 9. AC Testing Input Output Waveforms

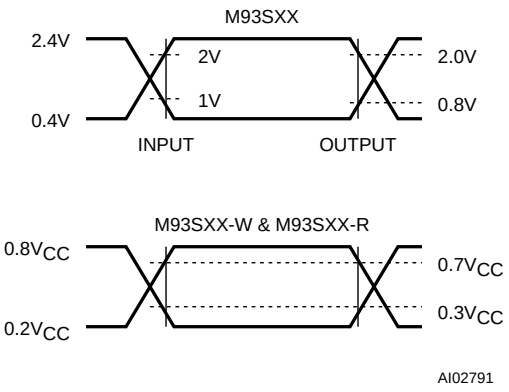


Table 10. Capacitance

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF

Note: Sampled only, not 100% tested, at T_A=25°C and a frequency of 1 MHz.

Table 13. DC Characteristics (M93Sx6-W, Device Grade 6)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2.5	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply Current (CMOS Inputs)	V_{CC} = 5V, S = V_{IH}, f = 1 MHz, Current Product [1]		1.5	mA
		V_{CC} = 2.5V, S = V_{IH}, f = 1 MHz, Current Product [1]		1	mA
		V_{CC} = 5V, S = V_{IH}, f = 2 MHz, New Product [2]		2	mA
		V_{CC} = 2.5V, S = V_{IH}, f = 2 MHz, New Product [2]		1	mA
I_{CC1}	Supply Current (Stand-by)	V_{CC} = 2.5V, S = V_{SS}, C = V_{SS}, Current Product [1]		10	µA
		V_{CC} = 2.5V, S = V_{SS}, C = V_{SS}, New Product [2]		5	µA
V_{IL}	Input Low Voltage (D, C, S)		–0.45	0.2 V_{CC}	V
V_{IH}	Input High Voltage (D, C, S)		0.7 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage (Q)	V_{CC} = 5V, I_{OL} = 2.1mA		0.4	V
		V_{CC} = 2.5V, I_{OL} = 100µA		0.2	V
V_{OH}	Output High Voltage (Q)	V_{CC} = 5V, I_{OH} = –400µA	2.4		V
		V_{CC} = 2.5V, I_{OH} = –100µA	V_{CC}–0.2		V

Note: 1. Current product: identified by Process Identification letter F or M.
2. New product: identified by Process Identification letter W or G.

Table 14. DC Characteristics (M93Sx6-W, Device Grade 3)

Symbol	Parameter	Test Condition	Min [1].	Max. [1]	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2.5	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply Current (CMOS Inputs)	V_{CC} = 5V, S = V_{IH}, f = 2 MHz		2	mA
		V_{CC} = 2.5V, S = V_{IH}, f = 2 MHz		1	mA
I_{CC1}	Supply Current (Stand-by)	V_{CC} = 2.5V, S = V_{SS}, C = V_{SS}		5	µA
V_{IL}	Input Low Voltage (D, C, S)		–0.45	0.2 V_{CC}	V
V_{IH}	Input High Voltage (D, C, S)		0.7 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage (Q)	V_{CC} = 5V, I_{OL} = 2.1mA		0.4	V
		V_{CC} = 2.5V, I_{OL} = 100µA		0.2	V
V_{OH}	Output High Voltage (Q)	V_{CC} = 5V, I_{OH} = –400µA	2.4		V
		V_{CC} = 2.5V, I_{OH} = –100µA	V_{CC}–0.2		V

Note: 1. New product: identified by Process Identification letter W or G.

Table 15. DC Characteristics (M93Sx6-R)

Symbol	Parameter	Test Condition	Min. [1]	Max. [1]	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2.5	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply Current (CMOS Inputs)	V_{CC} = 5V, S = V_{IH}, f = 2 MHz		2	mA
		V_{CC} = 1.8V, S = V_{IH}, f = 1 MHz		1	mA
I_{CC1}	Supply Current (Stand-by)	V_{CC} = 1.8V, S = V_{SS}, C = V_{SS}		2	µA
V_{IL}	Input Low Voltage (D, C, S)		–0.45	0.2 V_{CC}	V
V_{IH}	Input High Voltage (D, C, S)		0.8 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage (Q)	V_{CC} = 1.8V, I_{OL} = 100µA		0.2	V
V_{OH}	Output High Voltage (Q)	V_{CC} = 1.8V, I_{OH} = –100µA	V_{CC}–0.2		V

Note: 1. Preliminary Data: this product is under development. For more infomation, please contact your nearest ST sales office.

Table 17. AC Characteristics (M93Sx6-W, Device Grade 6)

Test conditions specified in Table 9. and Table 6.							
Symbol	**Alt.**	**Parameter**	**Min.[3]**	**Max.[3]**	**Min.[4]**	**Max.[4]**	**Unit**
f_C	f_{SK}	Clock Frequency	D.C.	1	D.C.	2	MHz
t_{PRVCH}	t_{PRES}	Protect Enable Valid to Clock High	50		50		ns
t_{WVCH}	t_{PES}	Write Enable Valid to Clock High	50		50		ns
t_{CLPRX}	t_{PREH}	Clock Low to Protect Enable Transition	0		0		ns
t_{SLWX}	t_{PEH}	Chip Select Low to Write Enable Transition	250		250		ns
t_{SLCH}		Chip Select Low to Clock High	250		50		ns
t_{SHCH}	t_{CSS}	Chip Select Set-up Time	100		50		ns
t_{SLSH}[2]	t_{CS}	Chip Select Low to Chip Select High	1000		200		ns
t_{CHCL}[1]	t_{SKH}	Clock High Time	350		200		ns
t_{CLCH}[1]	t_{SKL}	Clock Low Time	250		200		ns
t_{DVCH}	t_{DIS}	Data In Set-up Time	100		50		ns
t_{CHDX}	t_{DIH}	Data In Hold Time	100		50		ns
t_{CLSH}	t_{SKS}	Clock Set-up Time (relative to S)	100		50		ns
t_{CLSL}	t_{CSH}	Chip Select Hold Time	0		0		ns
t_{SHQV}	t_{SV}	Chip Select to Ready/Busy Status		400		200	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z		200		100	ns
t_{CHQL}	t_{PD0}	Delay to Output Low		400		200	ns
t_{CHQV}	t_{PD1}	Delay to Output Valid		400		200	ns
t_W	t_{WP}	Erase/Write Cycle time		10		5	ms

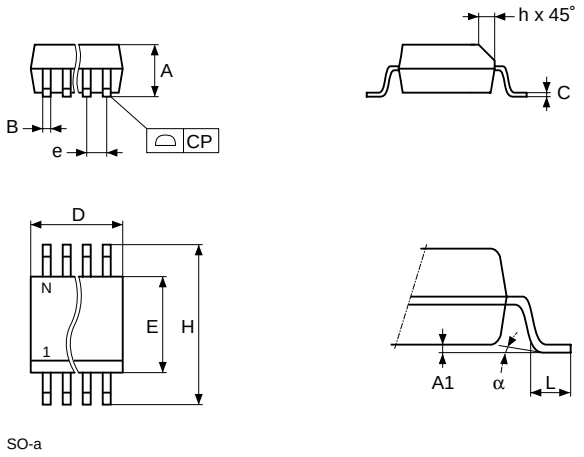
Note: 1. $t_{CHCL} + t_{CLCH} \geq 1 / f_C$.
2. Chip Select Input (S) must be brought Low for a minimum of tSLSH between consecutive instruction cycles.
3. Current product: identified by Process Identification letter F or M.
4. New product: identified by Process Identification letter W or G.

Table 18. AC Characteristics (M93Sx6-W, Device Grade 3)

Test conditions specified in Table 9. and Table 6.					
Symbol	**Alt.**	**Parameter**	**Min.[3]**	**Max.[3]**	**Unit**
f_C	f_{SK}	Clock Frequency	D.C.	2	MHz
t_{PRVCH}	t_{PRES}	Protect Enable Valid to Clock High	50		ns
t_{WVCH}	t_{PES}	Write Enable Valid to Clock High	50		ns
t_{CLPRX}	t_{PREH}	Clock Low to Protect Enable Transition	0		ns
t_{SLWX}	t_{PEH}	Chip Select Low to Write Enable Transition	250		ns
t_{SLCH}		Chip Select Low to Clock High	50		ns
t_{SHCH}	t_{CSS}	Chip Select Set-up Time	50		ns
t_{SLSH}[2]	t_{CS}	Chip Select Low to Chip Select High	200		ns
t_{CHCL}[1]	t_{SKH}	Clock High Time	200		ns
t_{CLCH}[1]	t_{SKL}	Clock Low Time	200		ns
t_{DVCH}	t_{DIS}	Data In Set-up Time	50		ns
t_{CHDX}	t_{DIH}	Data In Hold Time	50		ns
t_{CLSH}	t_{SKS}	Clock Set-up Time (relative to S)	50		ns
t_{CLSL}	t_{CSH}	Chip Select Hold Time	0		ns
t_{SHQV}	t_{SV}	Chip Select to Ready/Busy Status		200	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z		100	ns
t_{CHQL}	t_{PD0}	Delay to Output Low		200	ns
t_{CHQV}	t_{PD1}	Delay to Output Valid		200	ns
t_W	t_{WP}	Erase/Write Cycle time		5	ms

Note: 1. $t_{CHCL} + t_{CLCH} \geq 1 / f_C$.
2. Chip Select Input (S) must be brought Low for a minimum of tSLSH between consecutive instruction cycles.
3. New product: identified by Process Identification letter W or G.

Figure 14. SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width, Package Outline



Note: Drawing is not to scale.

Table 21. SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width, Package Mechanical Data

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

PART NUMBERING

Table 24. Ordering Information Scheme

Example: M93S66 – W MN 6 T P

Device Type

M93 = MICROWIRE serial access EEPROM (x16) with Block Protection

Device Function

66 = 4 Kbit (256 x 16)
56 = 2 Kbit (128 x 16)
46 = 1 Kbit (64 x 16)

Operating Voltage

blank = V_{CC} = 4.5 to 5.5V
W = V_{CC} = 2.5 to 5.5V
R = V_{CC} = 1.8 to 5.5V

Package

BN = PDIP8
MN = SO8 (150 mil width)
DW = TSSOP8 (169 mil width)
DS[2] = TSSOP8 (3x3mm body size)

Device Grade

6 = Industrial: device tested with standard test flow over –40 to 85 °C
3 = Automotive: device tested with High Reliability Certified Flow[1] over –40 to 125 °C

Option

blank = Standard Packing
T = Tape & Reel Packing

Plating Technology

blank = Standard SnPb plating
P = Lead-Free and RoHS compliant
G = Lead-Free, RoHS compliant, Sb_2O_3-free and TBBA-free

Note: 1. ST strongly recommends the use of the Automotive Grade devices for use in an automotive environment. The High Reliability Certified Flow (HRCF) is described in the quality note QNEE9801. Please ask your nearest ST sales office for a copy.
2. Available only on new products: identified by the Process Identification letter W or G.

Devices are shipped from the factory with the memory content set at all 1s (FFh).

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

Table 25. How to Identify Current and New Products by the Process Identification Letter

Markings on Current Products[1]	Markings on New Products[1]
M93S46W6 AYWW**F** (or AYWW**M**)	M93S46W6 AYWW**W** (or AYWW**G**)

Note: 1. This example comes from the S08 package. Other packages have similar information. For further information, please ask your ST Sales Office for Process Change Notice PCN MPG/EE/0059 (PCEE0059).