Features

- **Low-voltage and Standard-voltage Operation**
  - **1.8 (V_{CC} = 1.8V to 5.5V)**
- **User-selectable Internal Organization**
  - **1K: 128 x 8 or 64 x 16**
- **Three-wire Serial Interface**
- **2 MHz Clock Rate (5V)**
- **Self-timed Write Cycle (5 ms max)**
- **High Reliability**
  - **Endurance: 1 Million Write Cycles**
  - **Data Retention: 100 Years**
- **8-lead JEDEC PDIP, 8-lead JEDEC SOIC, 8-lead Ultra Thin mini-MAP (MLP 2x3), 8-lead TSSOP and 8-ball dBGA2 Packages**
- **Die Sales: Wafer Form, Tape and Reel, and Bumped Wafers**

Description

The AT93C46D provides 1024 bits of serial electrically erasable programmable read-only memory (EEPROM), organized as 64 words of 16 bits each (when the ORG pin is connected to VCC), and 128 words of 8 bits each (when the ORG pin is tied to ground). The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential. The AT93C46D is available in space-saving 8-lead PDIP, 8-lead JEDEC SOIC, 8-lead Ultra Thin mini-MAP (MLP 2x3), 8-lead TSSOP, and 8-lead dBGA2 packages.

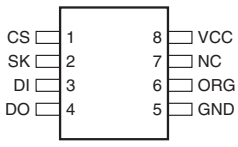
The AT93C46D is enabled through the Chip Select pin (CS) and accessed via a three-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a Read instruction at DI, the address is decoded and the data is clocked out serially on the DO pin. The Write cycle is completely self-timed, and no separate Erase cycle is required before Write. The Write cycle is only enabled when the part is in the Erase/Write Enable state. When CS is brought high following the initiation of a Write cycle, the DO pin outputs the Ready/Busy status of the part.

The AT93C46D is available in 1.8 (1.8V to 5.5V) version.

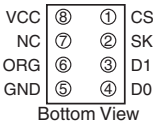
Table 0-1. Pin Configurations

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
VCC	Power Supply
ORG	Internal Organization
NC	No Connect

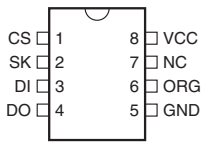
8-lead SOIC



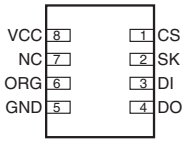
8-lead dBGA2



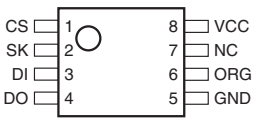
8-lead PDIP



8-lead Ultra Thin mini-MAP (MLP 2x3)



8-lead TSSOP



Three-wire Serial EEPROM

1K (128 x 8 or 64 x 16)

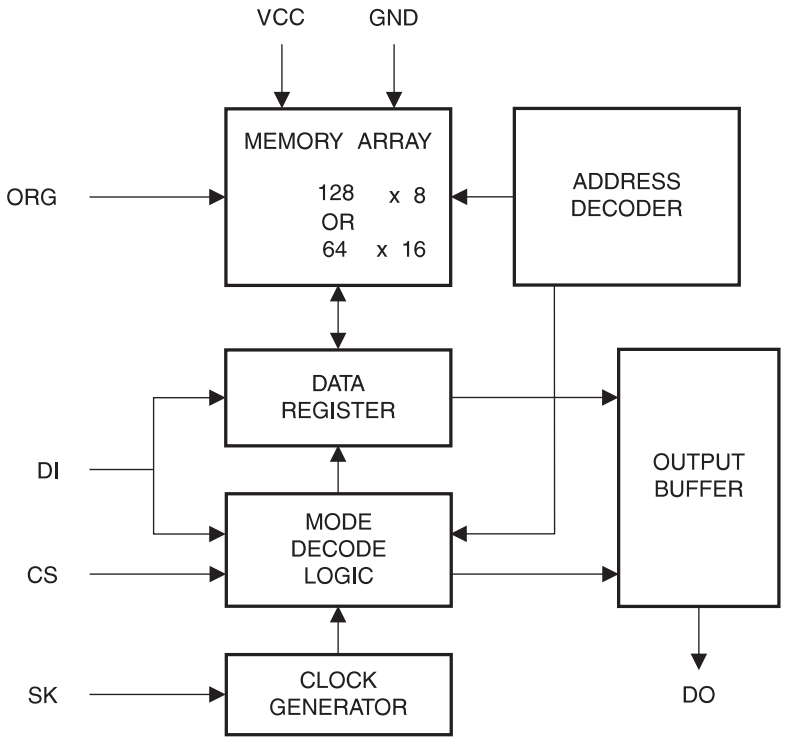
AT93C46D

1. Absolute Maximum Ratings*

Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Figure 1-1. Block Diagram



Notes:
1. When the ORG pin is connected to VCC, the "x 16" organization is selected. When it is connected to ground, the "x 8" organization is selected. If the ORG pin is left unconnected and the application does not load the input beyond the capability of the internal 1 Meg ohm pullup, then the "x 16" organization is selected.
2. For the AT93C46D, if the "x 16" organization is the mode of choice and pin 6 (ORG) is left unconnected, Atmel® recommends using AT93C46E device. For more details, see the AT93C46E datasheet.

Table 1-1. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.8V (unless otherwise noted)

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance (CS, SK, DI)	5	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

Table 1-2. DC Characteristics

Applicable over recommended operating range from: T_{AI} = –40°C to +85°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
V_{CC1}	Supply Voltage			1.8		5.5	V
V_{CC2}	Supply Voltage			2.7		5.5	V
V_{CC3}	Supply Voltage			4.5		5.5	V
I_{CC}	Supply Current	V_{CC} = 5.0V	READ at 1.0 MHz		0.5	2.0	mA
			WRITE at 1.0 MHz		0.5	2.0	mA
I_{SB1}	Standby Current	V_{CC} = 1.8V	CS = 0V		0.4	1.0	µA
I_{SB2}	Standby Current	V_{CC} = 2.7V	CS = 0V		6.0	10.0	µA
I_{SB3}	Standby Current	V_{CC} = 5.0V	CS = 0V		10.0	15.0	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}			0.1	1.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}			0.1	1.0	µA
V_{IL1}[1]	Input Low Voltage	2.7V ≤ V_{CC} ≤ 5.5V		–0.6		0.8	V
V_{IH1}[1]	Input High Voltage			2.0		V_{CC} + 1	
V_{IL2}[1]	Input Low Voltage	1.8V ≤ V_{CC} ≤ 2.7V		–0.6		V_{CC} x 0.3	V
V_{IH2}[1]	Input High Voltage			V_{CC} x 0.7		V_{CC} + 1	
V_{OL1}	Output Low Voltage	2.7V ≤ V_{CC} ≤ 5.5V	I_{OL} = 2.1 mA			0.4	V
V_{OH1}	Output High Voltage		I_{OH} = –0.4 mA	2.4			V
V_{OL2}	Output Low Voltage	1.8V ≤ V_{CC} ≤ 2.7V	I_{OL} = 0.15 mA			0.2	V
V_{OH2}	Output High Voltage		I_{OH} = –100 µA	V_{CC} – 0.2			V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

Table 1-3. AC Characteristics

Applicable over recommended operating range from T_{AI} = –40°C to + 85°C, V_{CC} = +2.7V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
f_{SK}	SK Clock Frequency	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		0 0 0		2 1 0.25	MHz
t_{SKH}	SK High Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		250 250 1000			ns
t_{SKL}	SK Low Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		250 250 1000			ns
t_{CS}	Minimum CS Low Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		250 250 1000			ns
t_{CSS}	CS Setup Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	50 50 200			ns
t_{DIS}	DI Setup Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	100 100 400			ns
t_{CSH}	CS Hold Time	Relative to SK		0			ns
t_{DIH}	DI Hold Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	100 100 400			ns
t_{PD1}	Output Delay to “1”	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			250 250 1000	ns
t_{PD0}	Output Delay to “0”	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			250 250 1000	ns
t_{SV}	CS to Status Valid	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			250 250 1000	ns
t_{DF}	CS to DO in High Impedance	AC Test CS = V_{IL}	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			100 150 400	ns
t_{WP}	Write Cycle Time		$1.8V \le V_{CC} \le 5.5V$	0.1	3	5	ms
Endurance[1]	5.0V, 25°C			1M			Write Cycles

Note: 1. This parameter is ensured by characterization.

4. AT93C46D Ordering Information

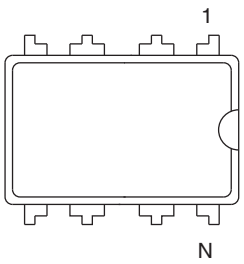
Ordering Code	Voltage	Package	Operation Range
AT93C46D-PU (Bulk form only)	1.8	8P3	Lead-free/Halogen-free/ Industrial Temperature (–40°C to 85°C)
AT93C46DN-SH-B(1) (NiPdAu Lead finish)	1.8	8S1	
AT93C46DN-SH-T(2) (NiPdAu Lead finish)	1.8	8S1	
AT93C46D-TH-B(1) (NiPdAu Lead finish)	1.8	8A2	
AT93C46D-TH-T(2) (NiPdAu Lead finish)	1.8	8A2	
AT93C46DY6-YH-T(2) (NiPdAu Lead finish)	1.8	8Y6	
AT93C46DU3-UU-T(2)	1.8	8U3-1	
AT93C46D-W-11(3)	1.8	Die Sale	Industrial (–40°C to 85°C)

Notes:
1. "-B" denotes bulk
2. "-T" denotes tape and reel. SOIC = 4K per reel. TSSOP, Ultra Thin Mini MAP, and dBGA2 = 5K per reel.
3. Available in tape and reel, and wafer form; order as SL788 for inkless wafer form. Bumped die available upon request. Please contact Serial Interface Marketing.

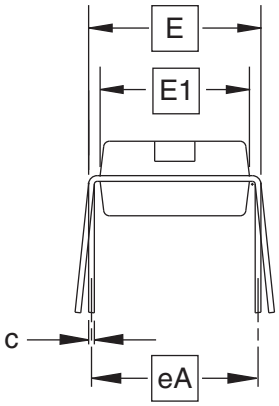
Package Type	
8P3	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8A2	8-lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
8U3-1	8-ball, Die Ball Grid Array Package (dBGA2)
8Y6	8-lead, 2.00 mm x 3.00 mm Body, 0.50mm Pitch, Ultra-Thin Mini-MAO, Dual No Lead Package. (DFN), (MLP 2x3mm)
Options	
–1.8	Low Voltage (1.8V to 5.5V)

6. Package Information

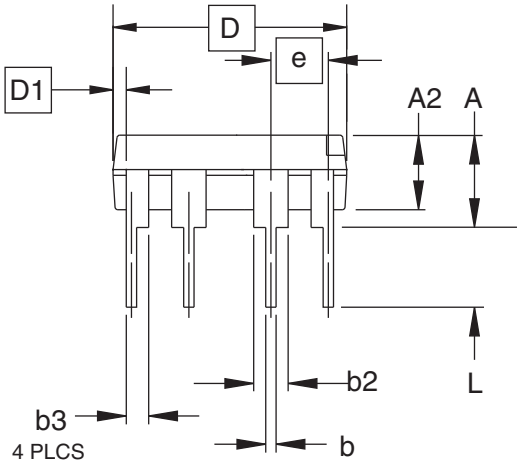
8P3 - PDIP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = inches)

SYMBOL	MIN	NOM	MAX	NOTE
A			0.210	2
A2	0.115	0.130	0.195	
b	0.014	0.018	0.022	5
b2	0.045	0.060	0.070	6
b3	0.030	0.039	0.045	6
c	0.008	0.010	0.014	
D	0.355	0.365	0.400	3
D1	0.005			3
E	0.300	0.310	0.325	4
E1	0.240	0.250	0.280	3
e	0.100 BSC			
eA	0.300 BSC			4
L	0.115	0.130	0.150	2

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
4. E and eA measured with the leads constrained to be perpendicular to datum.
5. Pointed or rounded lead tips are preferred to ease insertion.
6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8P3**, 8-lead, 0.300" Wide Body, Plastic Dual In-line Package (PDIP)	8P3	B