MC74HC4538A

Dual Precision Monostable Multivibrator (Retriggerable, Resettable)

ON Semiconductor®

The MC74HC4538A is identical in pinout to the MC14538B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

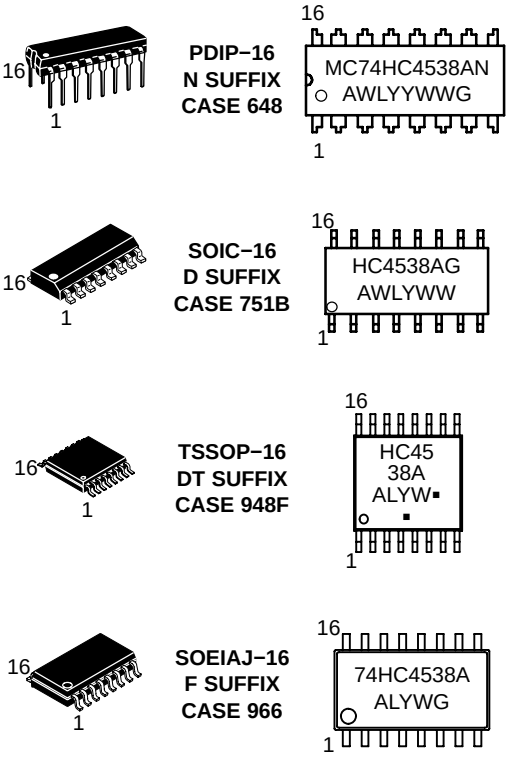
This dual monostable multivibrator may be triggered by either the positive or the negative edge of an input pulse, and produces a precision output pulse over a wide range of pulse widths. Because the device has conditioned trigger inputs, there are no trigger−input rise and fall time restrictions. The output pulse width is determined by the external timing components, R_x and C_x. The device has a reset function which forces the Q output low and the $\overline{Q}$ output high, regardless of the state of the output pulse circuitry.

Features

- Unlimited Rise and Fall Times Allowed on the Trigger Inputs
- Output Pulse is Independent of the Trigger Pulse Width
- ± 10% Guaranteed Pulse Width Variation from Part to Part (Using the Same Test Jig)
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 3.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 145 FETs or 36 Equivalent Gates
- Pb−Free Packages are Available*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MARKING DIAGRAMS



A	=	Assembly Location
L, WL	=	Wafer Lot
Y, YY	=	Year
W, WW	=	Work Week
G	=	Pb−Free Package
▪	=	Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

Publication Order Number:
MC74HC4538A/D

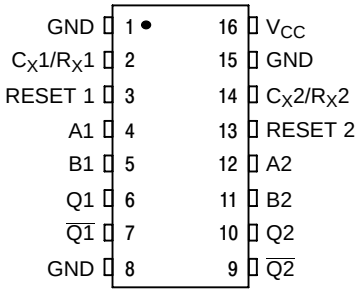


Figure 1. Pin Assignment

FUNCTION TABLE

Inputs			Outputs	
Reset	A	B	Q	$\overline{Q}$
H H	↑ L	H ↓	⊓ ⊓	⊔ ⊔
H H	X H	L X	Not Triggered Not Triggered	
H H	L,H,↓ L	H L,H,↑	Not Triggered Not Triggered	
L ↓ ↑	X X	X X	L Not Triggered	H

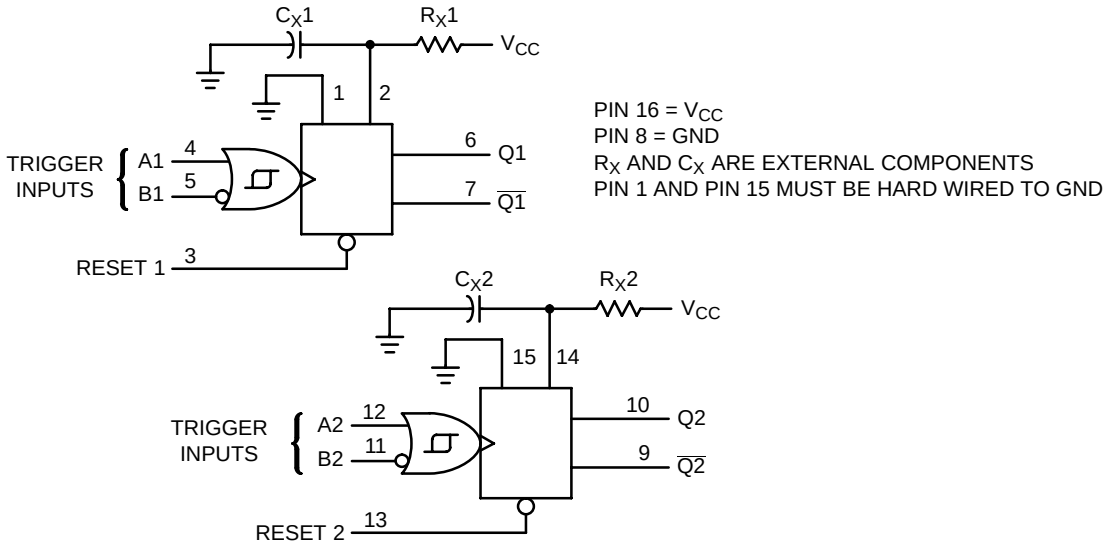


Figure 2. Logic Diagram

ORDERING INFORMATION

Device	Package	Shipping†
MC74HC4538AN	PDIP−16	500 Units / Box
MC74HC4538ANG	PDIP−16 (Pb−Free)	500 Units / Box
MC74HC4538AD	SOIC−16	48 Units / Rail
MC74HC4538ADG	SOIC−16 (Pb−Free)	48 Units / Rail
MC74HC4538ADR2	SOIC−16	2500 Units / Reel
MC74HC4538ADR2G	SOIC−16 (Pb−Free)	2500 Units / Reel
MC74HC4538ADTR2	TSSOP−16*	2500 Units / Reel
MC74HC4538ADTR2G	TSSOP−16*	2500 Units / Reel
MC74HC4538AF	SOEIAJ−16	50 Units / Rail
MC74HC4538AFG	SOEIAJ−16 (Pb−Free)	50 Units / Rail
MC74HC4538AFEL	SOEIAJ−16	2000 Units / Reel
MC74HC4538AFELG	SOEIAJ−16 (Pb−Free)	2000 Units / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +7.0	V
V_I	DC Input Voltage		$-0.5 \le V_I \le V_{CC} + 0.5$	V
V_O	DC Output Voltage	(Note 1)	$-0.5 \le V_O \le V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	A, B, Reset C_X, R_X	±20 ±30	mA
I_{OK}	DC Output Diode Current		±25	mA
I_O	DC Output Sink Current		±25	mA
I_{CC}	DC Supply Current per Supply Pin		±100	mA
I_{GND}	DC Ground Current per Ground Pin		±100	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction temperature under Bias		+150	°C
θ_{JA}	Thermal resistance	PDIP SOIC TSSOP	78 112 148	°C/W
P_D	Power Dissipation in Still Air at 85°C	PDIP SOIC TSSOP	750 500 450	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 30% − 35%	UL−94−VO (0.125 in)	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	>2000 >100 >500	V
$I_{Latchup}$	Latchup Performance	Above V_{CC} and Below GND at 85°C (Note 5)	±300	mA

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. Tested to EIA/JESD22−A114−A.
3. Tested to EIA/JESD22−A115−A.
4. Tested to JESD22−C101−A.
5. Tested to EIA/JESD78.
6. For high frequency or heavy load considerations, see the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		3.0*	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		–55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 7) A or B (Figure 5)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0 –	1000 500 400 No Limit	ns
R_x	External Timing Resistor	V_{CC} < 4.5 V $V_{CC} \ge$ 4.5 V	1.0 2.0	† †	kΩ
C_x	External Timing Capacitor		0	†	μF

*The HC4538A will function at 2.0 V but for optimum pulse−width stability, V_{CC} should be above 3.0 V.

†The maximum allowable values of R_x and C_x are a function of the leakage of capacitor C_x, the leakage of the HC4538A, and leakage due to board layout and surface resistance. For most applications, C_x/R_x should be limited to a maximum value of 10 μF/1.0 MΩ. Values of C_x > 1.0 μF may cause a problem during power down (see Power Down Considerations). Susceptibility to externally induced noise signals may occur for R_x > 1.0 MΩ.

7. Unused inputs may not be left open. All inputs must be tied to a high−logic voltage level or a low−logic input voltage level.
8. Information on typical parametric values can be found in the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limits						Unit
				–55 to 25°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
V_{IH}	Minimum High−Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	1.5 3.15 4.2		1.5 3.15 4.2		1.5 3.15 4.2		V
V_{IL}	Maximum Low−Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0		0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V
V_{OH}	Minimum High−Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		1.9 4.4 5.9		V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \leq -4.0$ mA $\|I_{out}\| \leq -5.2$ mA	 4.5 6.0	 3.98 5.48		 3.84 5.34		 3.7 5.2		
V_{OL}	Maximum Low−Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0		0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \leq 4.0$ mA $\|I_{out}\| \leq 5.2$ mA	 4.5 6.0		 0.26 0.26		 0.33 0.33		 0.4 0.4	
I_{in}	Maximum Input Leakage Current (A, B, Reset)	V_{in} = V_{CC} or GND	6.0		± 0.1		± 1.0		± 1.0	μA
I_{in}	Maximum Input Leakage Current (R_x, C_x)	V_{in} = V_{CC} or GND	6.0		± 50		± 500		± 500	nA
I_{CC}	Maximum Quiescent Supply Current (per package) Standby State	V_{in} = V_{CC} or GND Q1 and Q2 = Low I_{out} = 0 μA	6.0		130		220		350	μA
I_{CC}	Maximum Supply Current (per package) Active State	V_{in} = V_{CC} or GND Q1 and Q2 = High I_{out} = 0 μA Pins 2 and 14 = 0.5 V_{CC}	 6.0	25°C 	 400	–45°C to 85°C 	 600	–55°C to 125°C 	 800	μA

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limits						Unit
			–55 to 25°C		≤ 85°C		≤ 125°C		
			Min	Max	Min	Max	Min	Max	
t_{PLH}	Maximum Propagation Delay Input A or B to Q (Figures 6 and 8)	2.0 4.5 6.0		175 35 30		220 44 37		265 53 45	ns
t_{PHL}	Maximum Propagation Delay Input A or B to NQ (Figures 6 and 8)	2.0 4.5 6.0		195 39 33		245 49 42		295 59 50	ns
t_{PHL}	Maximum Propagation Delay Reset to Q (Figures 7 and 8)	2.0 4.5 6.0		175 35 30		220 44 37		265 53 45	ns
t_{PLH}	Maximum Propagation Delay Reset to NQ (Figures 7 and 8)	2.0 4.5 6.0		175 35 30		220 44 37		265 53 45	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 7 and 8)	2.0 4.5 6.0		75 15 13		95 19 16		110 22 19	ns
C_{in}	Maximum Input Capacitance (A. B, Reset) (C_x, R_x)	–		10 25		10 25		10 25	pF

9. For propagation delays with loads other than 50 pF, and information on typical parametric values, see the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (per Multivibrator)*	150	pF

*Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

TIMING CHARACTERISTICS (Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limits						Unit
			–55 to 25°C		≤ 85°C		≤ 125°C		
			Min	Max	Min	Max	Min	Max	
t_{rec}	Minimum Recovery Time, Inactive to A or B (Figure 7)	2.0 4.5 6.0	0 0 0		0 0 0		0 0 0		ns
t_w	Minimum Pulse Width, Input A or B (Figure 6)	2.0 4.5 6.0	60 12 10		75 15 13		90 18 15		ns
t_w	Minimum Pulse Width, Reset (Figure 7)	2.0 4.5 6.0	60 12 10		75 15 13		90 18 15		ns
t_r, t_f	Maximum Input Rise and Fall Times, Reset (Figure 7)	2.0 4.5 6.0		1000 500 400		1000 500 400		1000 500 400	ns
	A or B (Figure 7)	2.0 4.5 6.0	No Limit						

OUTPUT PULSE WIDTH CHARACTERISTICS (C_L = 50 pF)t

Symbol	Parameter	Conditions		Guaranteed Limits						Unit
				–55 to 25°C		≤ 85°C		≤ 125°C		
		Timing Components	V_{CC} V	Min	Max	Min	Max	Min	Max	
τ	Output Pulse Width* (Figures 6 and 8)	R_x = 10 kΩ, C_x = 0.1 μF	5.0	0.63	0.77	0.6	0.8	0.59	0.81	ms
–	Pulse Width Match Between Circuits in the same Package	–	–	± 5.0						%
–	Pulse Width Match Variation (Part to Part)	–	–	± 10						%

*For output pulse widths greater than 100 μs, typically τ = kR_xC_x, where the value of k may be found in Figure 3.

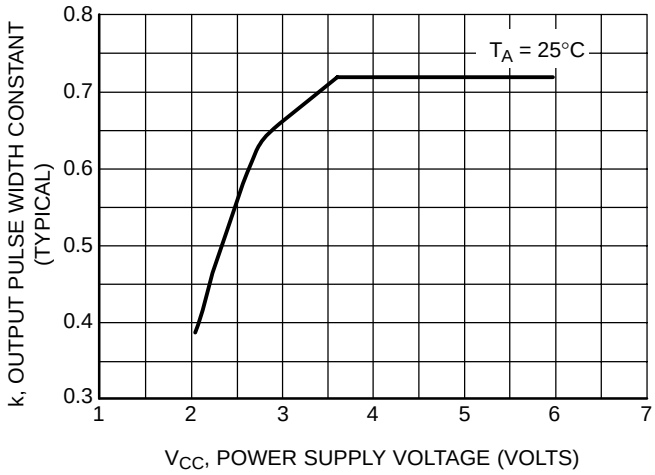


Figure 3. Typical Output Pulse Width Constant, k, versus Supply Voltage (For output pulse widths > 100 μs: τ = kR_xC_x)

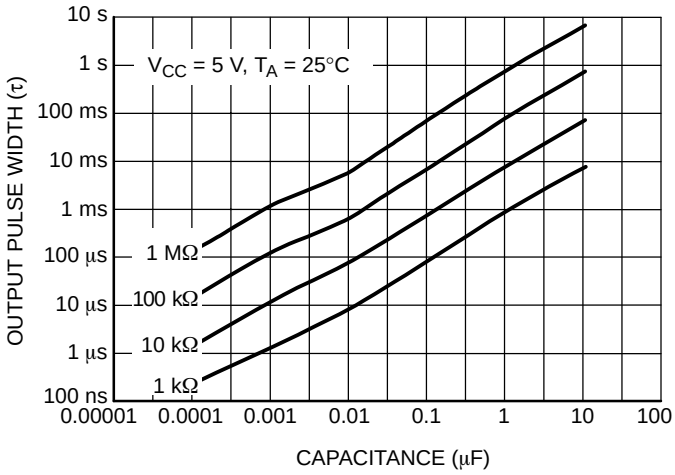


Figure 4. Output Pulse Width versus Timing Capacitance

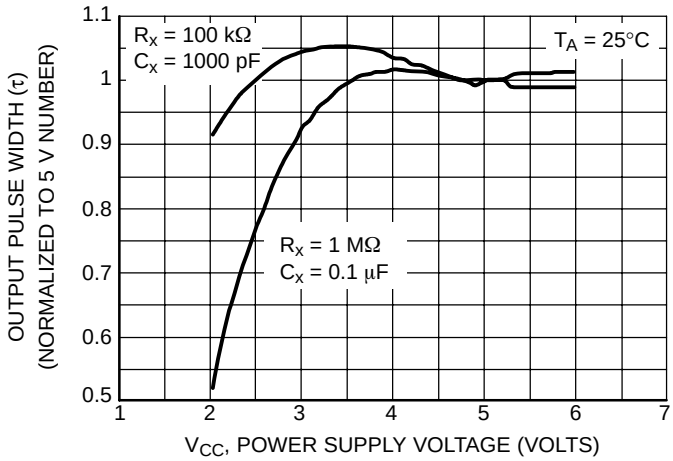
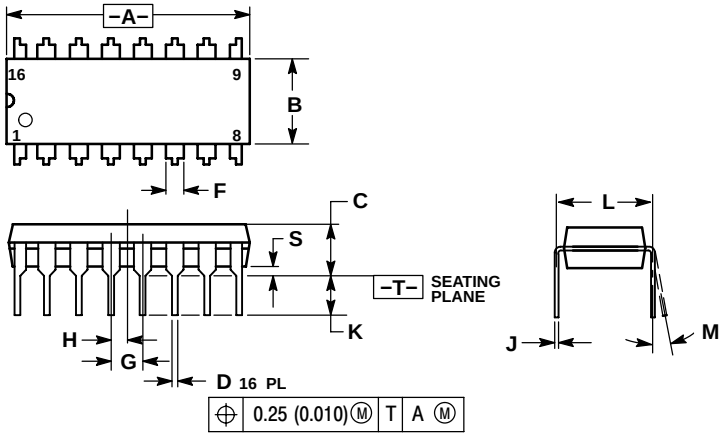


Figure 5. Normalized Output Pulse Width versus Power Supply Voltage

PACKAGE DIMENSIONS

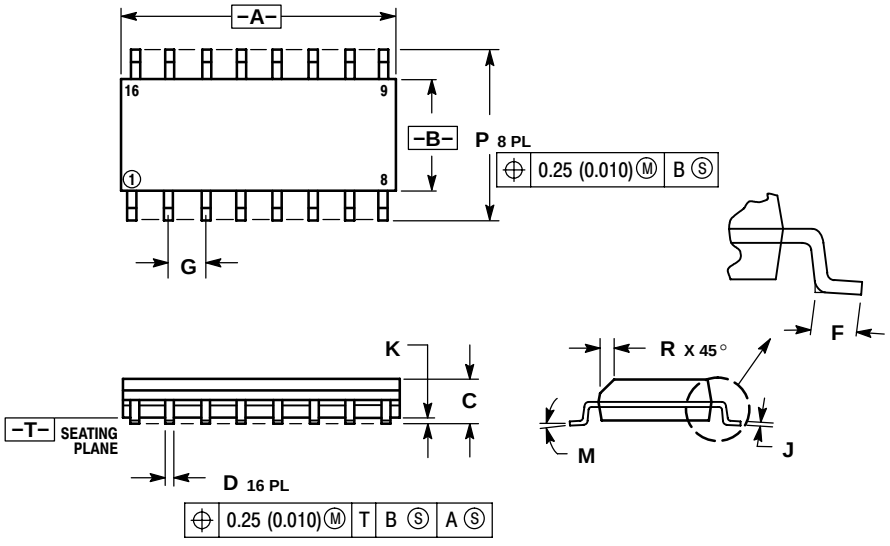
PDIP−16
N SUFFIX
CASE 648−08
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

SOIC−16
D SUFFIX
CASE 751B−05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019