

MC14538B

Dual Precision Retriggerable/Resetable Monostable Multivibrator

The MC14538B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and produces an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, C_X and R_X . Output Pulse Width $T = R_X \cdot C_X$ (secs)

$$R_X = \Omega$$

$$C_X = \text{Farads}$$

Features

- Unlimited Rise and Fall Time Allowed on the A Trigger Input
- Pulse Width Range = 10 μ s to 10 s
- Latched Trigger Inputs
- Separate Latched Reset Inputs
- 3.0 Vdc to 18 Vdc Operational Limits
- Triggerable from Positive (A Input) or Negative-Going Edge (B-Input)
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-pin Compatible with MC14528B and CD4528B (CD4098)
- Use the MC54/74HC4538A for Pulse Widths Less Than 10 μ s with Supplies Up to 6 V
- Pb-Free Packages are Available*

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	± 10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Operating Temperature Range	-55 to +125	$^{\circ}$ C
T_{stg}	Storage Temperature Range	-65 to +150	$^{\circ}$ C
T_L	Lead Temperature (8-Second Soldering)	260	$^{\circ}$ C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}$ C From 65 $^{\circ}$ C To 125 $^{\circ}$ C

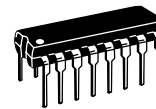
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

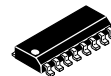


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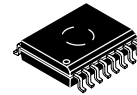
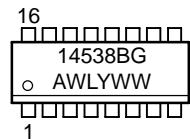
MARKING DIAGRAMS



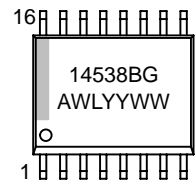
PDIP-16
P SUFFIX
CASE 648



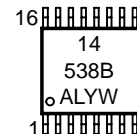
SOIC-16
D SUFFIX
CASE 751B



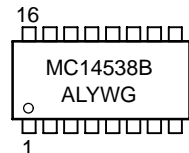
SOIC-16
DW SUFFIX
CASE 751G



TSSOP-16
DT SUFFIX
CASE 948F



SOEIAJ-16
F SUFFIX
CASE 966



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Indicator

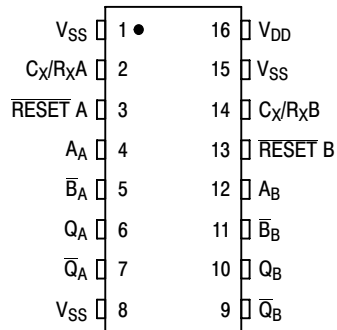
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

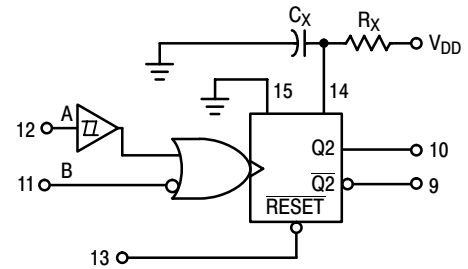
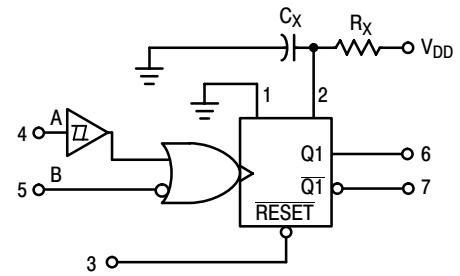
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PIN ASSIGNMENT

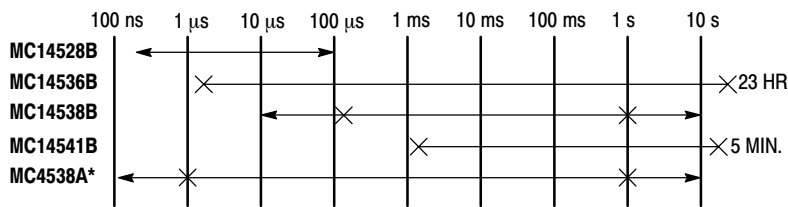


BLOCK DIAGRAM



R_X AND C_X ARE EXTERNAL COMPONENTS.
V_{DD} = PIN 16
V_{SS} = PIN 8, PIN 1, PIN 15

ONE-SHOT SELECTION GUIDE



*LIMITED OPERATING VOLTAGE (2 - 6 V)

TOTAL OUTPUT PULSE WIDTH RANGE ←————→
RECOMMENDED PULSE WIDTH RANGE ×————×

ORDERING INFORMATION

Device	Package	Shipping†
MC14538BCP	PDIP-16	500 Units / Rail
MC14538BCPG	PDIP-16 (Pb-Free)	500 Units / Rail
MC14538BD	SOIC-16	48 Units / Rail
MC14538BDG	SOIC-16 (Pb-Free)	48 Units / Rail
MC14538BDR2	SOIC-16	2500 Units / Tape & Reel
MC14538BDR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
MC14538BDW	SOIC-16 WB	47 Units / Rail
MC14538BDWR2	SOIC-16 WB	1000 Units / Tape & Reel
MC14538BDWR2G	SOIC-16 WB (Pb-Free)	1000 Units / Tape & Reel
MC14538BDTR2	TSSOP-16*	2500 Units / Tape & Reel
MC14538BF	SOEIAJ-16	50 Units / Rail
MC14538BFG	SOEIAJ-16 (Pb-Free)	50 Units / Rail
MC14538BFEL	SOEIAJ-16	2000 Units / Tape & Reel
MC14538BFELG	SOEIAJ-16 (Pb-Free)	2000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (Note 2)	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	"0" Level V _{OL}	5.0	-	0.05	-	0	0.05	-	0.05	Vdc	
		10	-	0.05	-	0	0.05	-	0.05		
		15	-	0.05	-	0	0.05	-	0.05		
	V _{in} = 0 or V _{DD}	"1" Level V _{OH}	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
			10	9.95	-	9.95	10	-	9.95	-	
			15	14.95	-	14.95	15	-	14.95	-	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	"0" Level V _{IL}	5.0	-	1.5	-	2.25	1.5	-	1.5	Vdc	
		10	-	3.0	-	4.50	3.0	-	3.0		
		15	-	4.0	-	6.75	4.0	-	4.0		
	V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	"1" Level V _{IH}	5.0	3.5	-	3.5	2.75	-	3.5	-	Vdc
			10	7.0	-	7.0	5.50	-	7.0	-	
			15	11	-	11	8.25	-	11	-	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	- 3.0	-	- 2.4	- 4.2	-	- 1.7	-	mAdc	
		5.0	- 0.64	-	- 0.51	- 0.88	-	- 0.36	-		
		10	- 1.6	-	- 1.3	- 2.25	-	- 0.9	-		
	V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Sink I _{OL}	5.0	0.64	-	0.51	0.88	-	0.36	-	mAdc
			10	1.6	-	1.3	2.25	-	0.9	-	
			15	4.2	-	3.4	8.8	-	2.4	-	
Input Current, Pin 2 or 14	I _{in}	15	-	±0.05	-	±0.00001	±0.05	-	±0.5	µAdc	
Input Current, Other Inputs	I _{in}	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	µAdc	
Input Capacitance, Pin 2 or 14	C _{in}	-	-	-	-	25	-	-	-	pF	
Input Capacitance, Other Inputs (V _{in} = 0)	C _{in}	-	-	-	-	5.0	7.5	-	-	pF	
Quiescent Current (Per Package) Q = Low, \bar{Q} = High	I _{DD}	5.0	-	5.0	-	0.005	5.0	-	150	µAdc	
		10	-	10	-	0.010	10	-	300		
		15	-	20	-	0.015	20	-	600		
Quiescent Current, Active State (Both) (Per Package) Q = High, \bar{Q} = Low	I _{DD}	5.0	-	2.0	-	0.04	0.20	-	2.0	mAdc	
		10	-	2.0	-	0.08	0.45	-	2.0		
		15	-	2.0	-	0.13	0.70	-	2.0		
Total Supply Current at an external load capacitance (C _L) and at external timing network (R _X , C _X) (Note 3)	I _T	5.0 10	$I_T = (3.5 \times 10^{-2}) R_X C_X f + 4 C_X f + 1 \times 10^{-5} C_L f$ $I_T = (8.0 \times 10^{-2}) R_X C_X f + 9 C_X f + 2 \times 10^{-5} C_L f$ $I_T = (1.25 \times 10^{-1}) R_X C_X f + 12 C_X f + 3 \times 10^{-5} C_L f$ where: I _T in µA (one monostable switching only), C _X in µF, C _L in pF, R _X in k ohms, and f in Hz is the input frequency.							µAdc	

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at 25°C.

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SWITCHING CHARACTERISTICS (Note 4) ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD} V_{dc}	All Types			Unit
			Min	Typ (Note 5)	Max	
Output Rise Time $t_{TLH} = (1.35 \text{ ns/pF}) C_L + 33 \text{ ns}$ $t_{TLH} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	t_{TLH}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Output Fall Time $t_{THL} = (1.35 \text{ ns/pF}) C_L + 33 \text{ ns}$ $t_{THL} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{THL} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	t_{THL}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay Time A or B to Q or \bar{Q} $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 255 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 132 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 87 \text{ ns}$ Reset to Q or \bar{Q} $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 205 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 107 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 82 \text{ ns}$	$t_{PLH},$ t_{PHL}	5.0 10 15 5.0 10 15	– – – – – –	300 150 100 250 125 95	600 300 220 500 250 190	ns ns
Input Rise and Fall Times Reset B Input A Input	t_r, t_f	5 10 15 5 10 15 5 10 15	– – – – – – – – –	– – – 300 1.2 0.4 No Limit	15 5 4 1.0 0.1 0.05 –	μs ms –
Input Pulse Width A, B, or Reset	$t_{WH},$ t_{WL}	5.0 10 15	170 90 80	85 45 40	– – –	ns
Retrigger Time	t_{rr}	5.0 10 15	0 0 0	– – –	– – –	ns
Output Pulse Width — Q or \bar{Q} Refer to Figures 8 and 9 $C_X = 0.002 \mu\text{F}, R_X = 100 \text{ k}\Omega$ $C_X = 0.1 \mu\text{F}, R_X = 100 \text{ k}\Omega$ $C_X = 10 \mu\text{F}, R_X = 100 \text{ k}\Omega$	T	5.0 10 15 5.0 10 15 5.0 10 15	198 200 202 9.3 9.4 9.5 0.91 0.92 0.93	210 212 214 9.86 10 10.14 0.965 0.98 0.99	230 232 234 10.5 10.6 10.7 1.03 1.04 1.06	μs ms s
Pulse Width Match between circuits in the same package. $C_X = 0.1 \mu\text{F}, R_X = 100 \text{ k}\Omega$	100 [($T_1 - T_2$)/ T_1]	5.0 10 15	– – –	± 1.0 ± 1.0 ± 1.0	± 5.0 ± 5.0 ± 5.0	%

4. The formulas given are for the typical characteristics only at 25°C .

5. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

OPERATING CONDITIONS

External Timing Resistance	R_X	–	5.0	–	(Note 6)	$\text{k}\Omega$
External Timing Capacitance	C_X	–	0	–	No Limit (Note 7)	μF

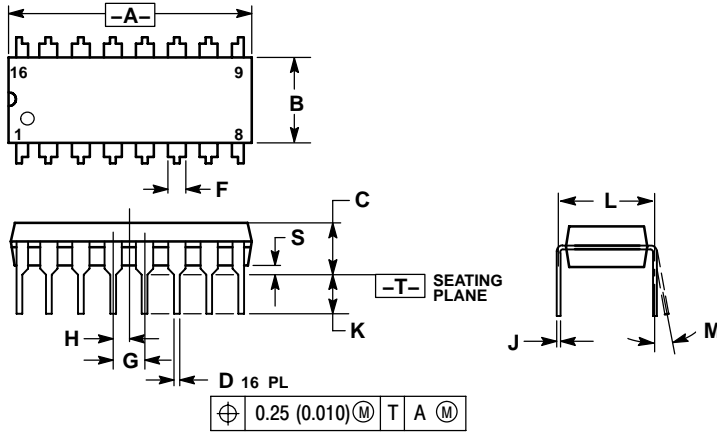
6. The maximum usable resistance R_X is a function of the leakage of the capacitor C_X , leakage of the MC14538B, and leakage due to board layout and surface resistance. Susceptibility to externally induced noise signals may occur for $R_X > 1 \text{ M}\Omega$.

7. If $C_X > 15 \mu\text{F}$, use discharge protection diode per Fig. 11.

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PACKAGE DIMENSIONS

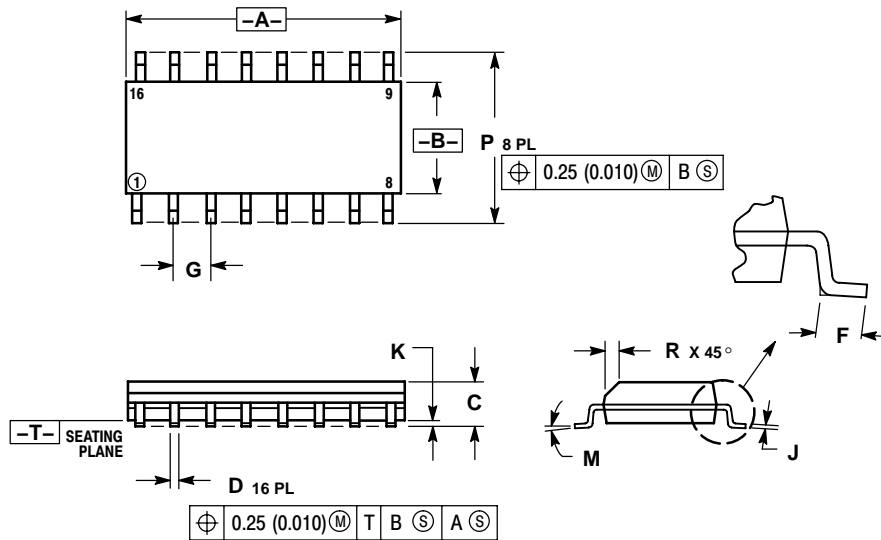
PDIP-16
P SUFFIX
PLASTIC DIP PACKAGE
CASE 648-08
ISSUE T



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0° 10°		0° 10°	
S	0.020	0.040	0.51	1.01

SOIC-16
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B-05
ISSUE J



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0° 7°		0° 7°	
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019