

# NDF08N50Z, NDP08N50Z

## N-Channel Power MOSFET 500 V, 0.69 Ω

### Features

- Low ON Resistance
- Low Gate Charge
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

### ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25°C unless otherwise noted)

Rating	Symbol	NDF08N50Z	NDP08N50Z	Unit
Drain-to-Source Voltage	V <sub>DSS</sub>	500		V
Continuous Drain Current R <sub>θJC</sub>	I <sub>D</sub>	7.5 (Note 1)	7.5	A
Continuous Drain Current R <sub>θJC</sub> T <sub>A</sub> = 100°C	I <sub>D</sub>	4.7 (Note 1)	4.7	A
Pulsed Drain Current, V <sub>GS</sub> @ 10 V	I <sub>DM</sub>	30 (Note 1)	30	A
Power Dissipation	P <sub>D</sub>	31	125	W
Gate-to-Source Voltage	V <sub>GS</sub>	30		V
Single Pulse Avalanche Energy, I <sub>D</sub> = 7.5 A	E <sub>AS</sub>	190		mJ
ESD (HBM) (JESD 22-A114)	V <sub>esd</sub>	3500		V
RMS Isolation Voltage (t = 0.3 sec., R.H. ≤ 30%, T <sub>A</sub> = 25°C) (Figure 14)	V <sub>ISO</sub>	4500		V
Peak Diode Recovery	dv/dt	4.5		V/ns
Continuous Source Current (Body Diode)	I <sub>S</sub>	7.5		A
Maximum Temperature for Soldering Leads	T <sub>L</sub>	260		°C
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

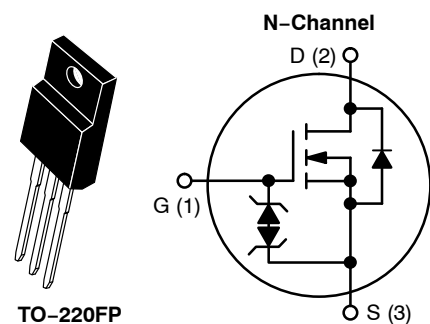
1. Limited by maximum junction temperature
2. I<sub>SD</sub> = 7.5 A, di/dt ≤ 100 A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, T<sub>J</sub> = +150°C



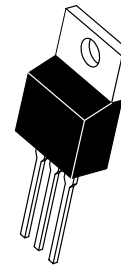
ON Semiconductor®

<http://onsemi.com>

V <sub>DSS</sub>	R <sub>DS(ON)</sub> (TYP) @ 3.6 A
500 V	0.69 Ω

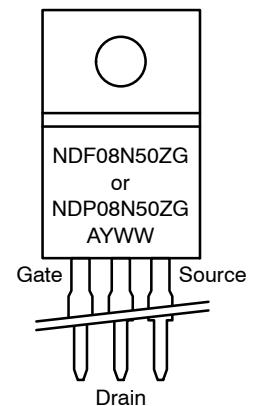


TO-220FP  
CASE 221D  
STYLE 1



TO-220AB  
CASE 221A  
STYLE 5

### MARKING DIAGRAM



- A = Location Code
- Y = Year
- WW = Work Week
- G = Pb-Free Package

### ORDERING INFORMATION

Device	Package	Shipping
NDF08N50ZG	TO-220FP	50 Units/Rail
NDP08N50ZG	TO-220AB	In Development

# NDF08N50Z, NDP08N50Z

## THERMAL RESISTANCE

Parameter	Symbol	NDF08N50Z	NDP08N50Z	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	4.0	1.0	°C/W
Junction-to-Ambient Steady State (Note 3)	$R_{\theta JA}$	50	50	

3. Insertion mounted

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	$BV_{DSS}$	500			V
Breakdown Voltage Temperature Coefficient	Reference to $25^\circ\text{C}$ , $I_D = 1\text{ mA}$	$\Delta BV_{DSS} / \Delta T_J$		0.6		V/°C
Drain-to-Source Leakage Current	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	$I_{DSS}$			1	$\mu\text{A}$
					50	
Gate-to-Source Forward Leakage	$V_{GS} = \pm 20\text{ V}$	$I_{GSS}$			$\pm 10$	$\mu\text{A}$

### ON CHARACTERISTICS (Note 4)

Static Drain-to-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 3.6\text{ A}$	$R_{DS(on)}$		0.69	0.85	$\Omega$
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 100\ \mu\text{A}$	$V_{GS(th)}$	3.0		4.5	V
Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 3.75\text{ A}$	$g_{FS}$		6.0		S

### DYNAMIC CHARACTERISTICS

Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	$C_{iss}$		912		$\text{pF}$
Output Capacitance		$C_{oss}$		120		
Reverse Transfer Capacitance		$C_{rss}$		27		
Total Gate Charge	$V_{DD} = 250\text{ V}, I_D = 7.5\text{ A},$ $V_{GS} = 10\text{ V}$	$Q_g$		31		$\text{nC}$
Gate-to-Source Charge		$Q_{gs}$		6.2		
Gate-to-Drain ("Miller") Charge		$Q_{gd}$		17		
Plateau Voltage		$V_{GP}$		6.3		V
Gate Resistance		$R_g$		3.0		$\Omega$

### RESISTIVE SWITCHING CHARACTERISTICS

Turn-On Delay Time	$V_{DD} = 250\text{ V}, I_D = 7.5\text{ A},$ $V_{GS} = 10\text{ V}, R_G = 5\ \Omega$	$t_{d(on)}$		13		$\text{ns}$
Rise Time		$t_r$		23		
Turn-Off Delay Time		$t_{d(off)}$		31		
Fall Time		$t_f$		29		

### SOURCE-DRAIN DIODE CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Diode Forward Voltage	$I_S = 7.5\text{ A}, V_{GS} = 0\text{ V}$	$V_{SD}$			1.6	V
Reverse Recovery Time	$V_{GS} = 0\text{ V}, V_{DD} = 30\text{ V}$ $I_S = 7.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	$t_{rr}$		295		ns
Reverse Recovery Charge		$Q_{rr}$		1.85		$\mu\text{C}$

4. Pulse Width  $\leq 380\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

# NDF08N50Z, NDP08N50Z

## TYPICAL CHARACTERISTICS

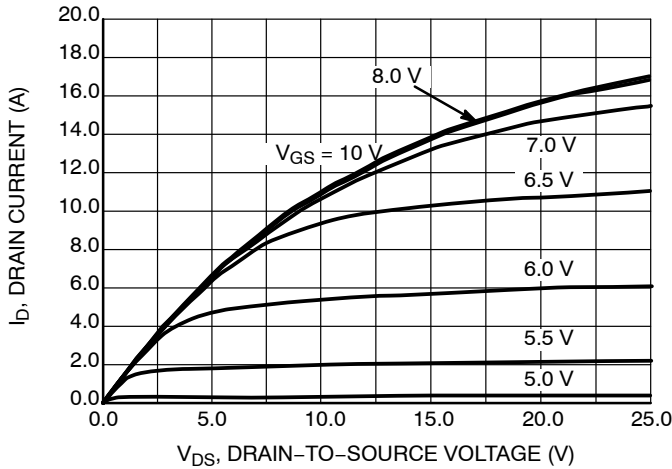


Figure 1. On-Region Characteristics

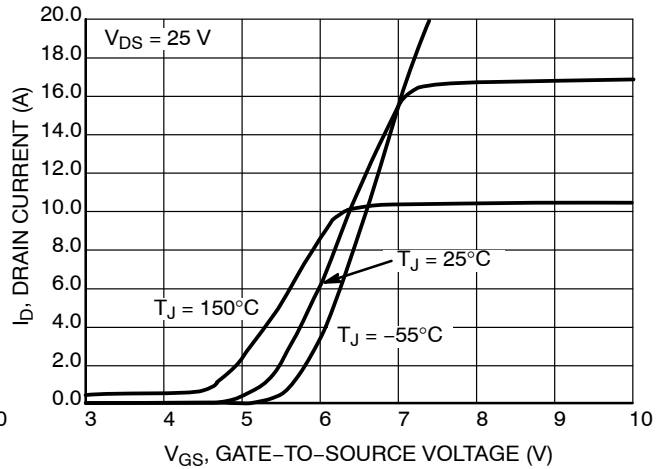


Figure 2. Transfer Characteristics

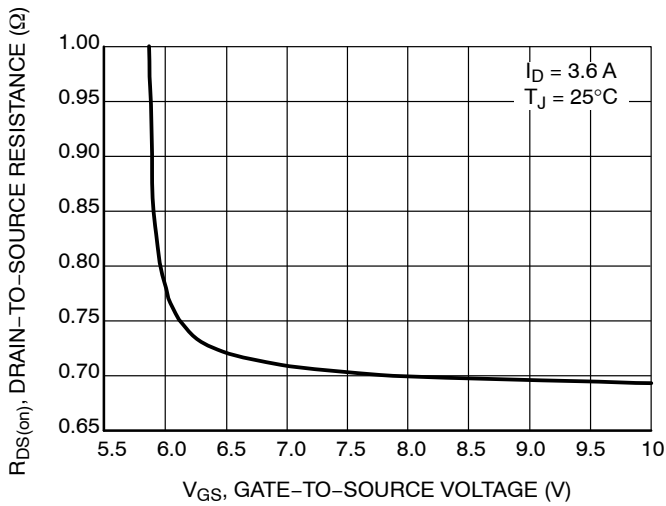


Figure 3. On-Region versus Gate-to-Source Voltage

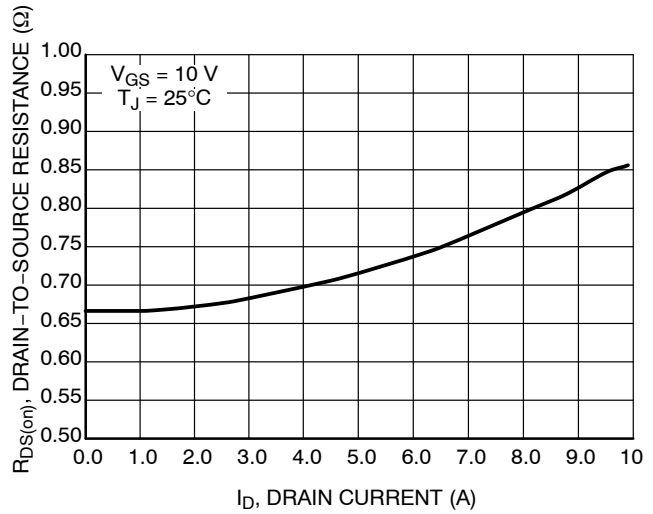


Figure 4. On-Resistance versus Drain Current and Gate Voltage

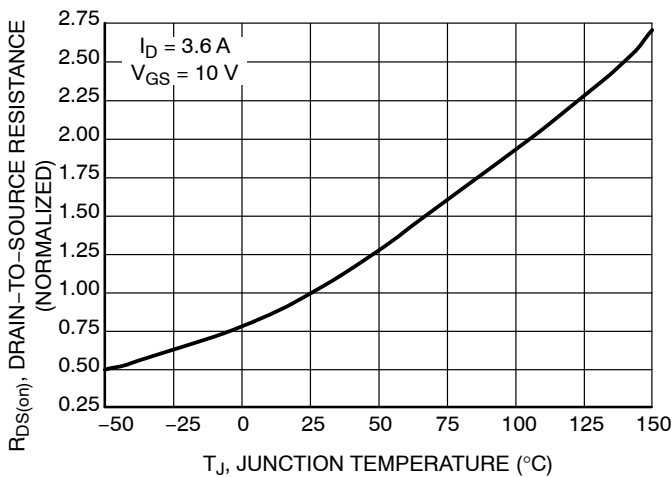


Figure 5. On-Resistance Variation with Temperature

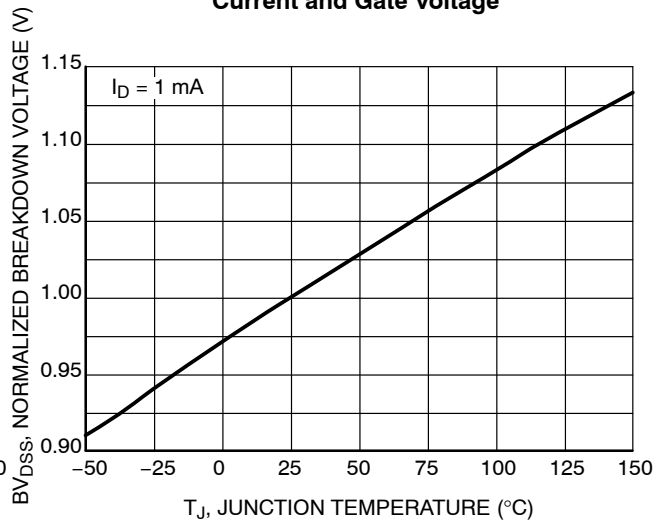
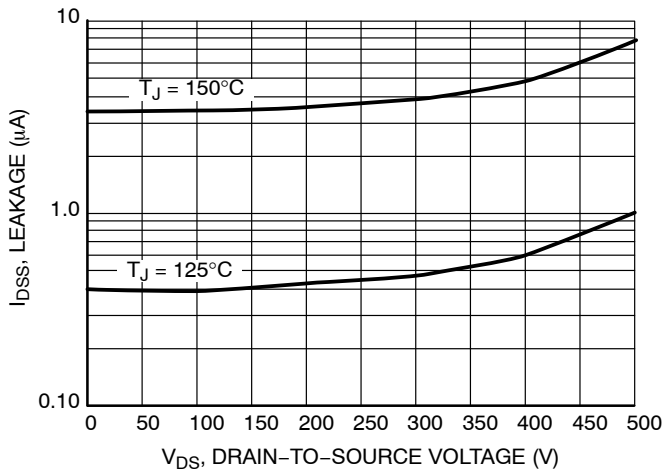


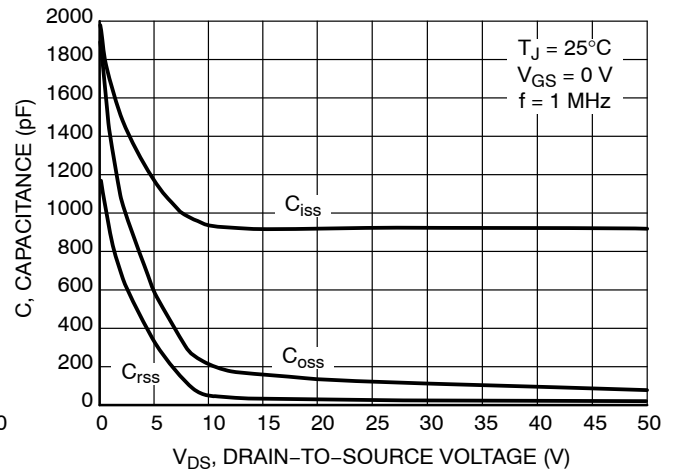
Figure 6.  $BV_{DSS}$  Variation with Temperature

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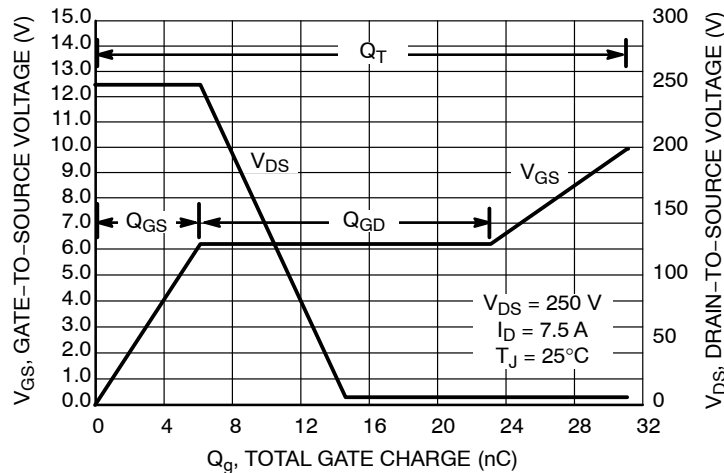
## TYPICAL CHARACTERISTICS



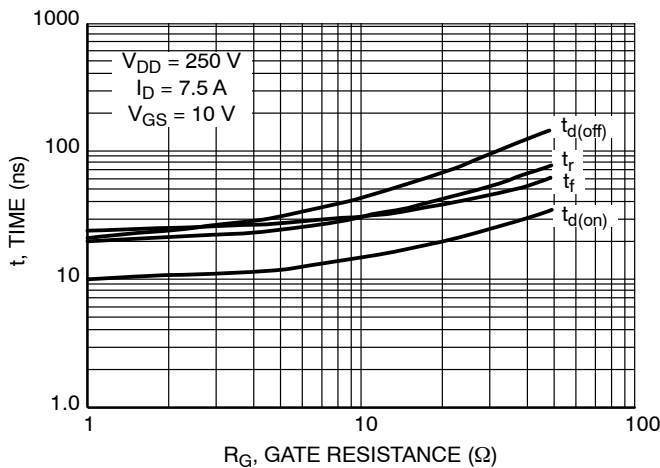
**Figure 7. Drain-to-Source Leakage Current versus Voltage**



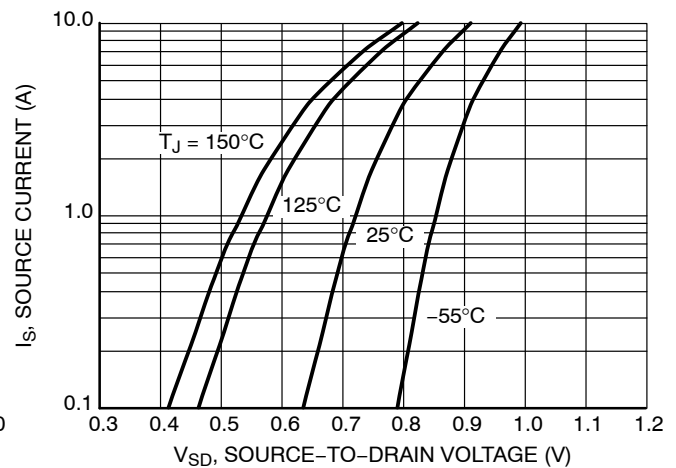
**Figure 8. Capacitance Variation**



**Figure 9. Gate-to-Source Voltage and Drain-to-Source Voltage versus Total Charge**



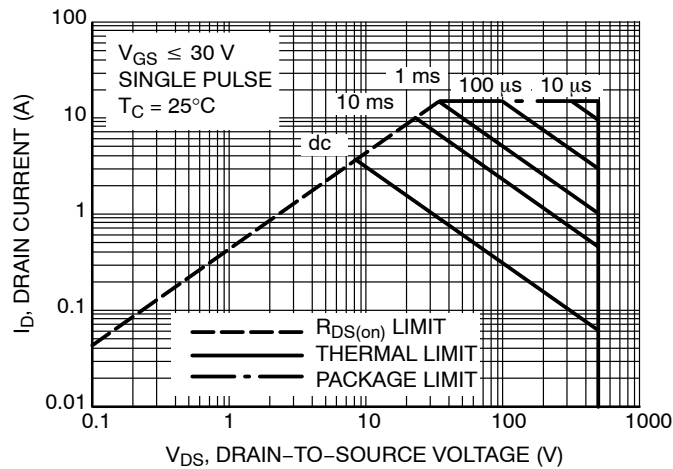
**Figure 10. Resistive Switching Time Variation versus Gate Resistance**



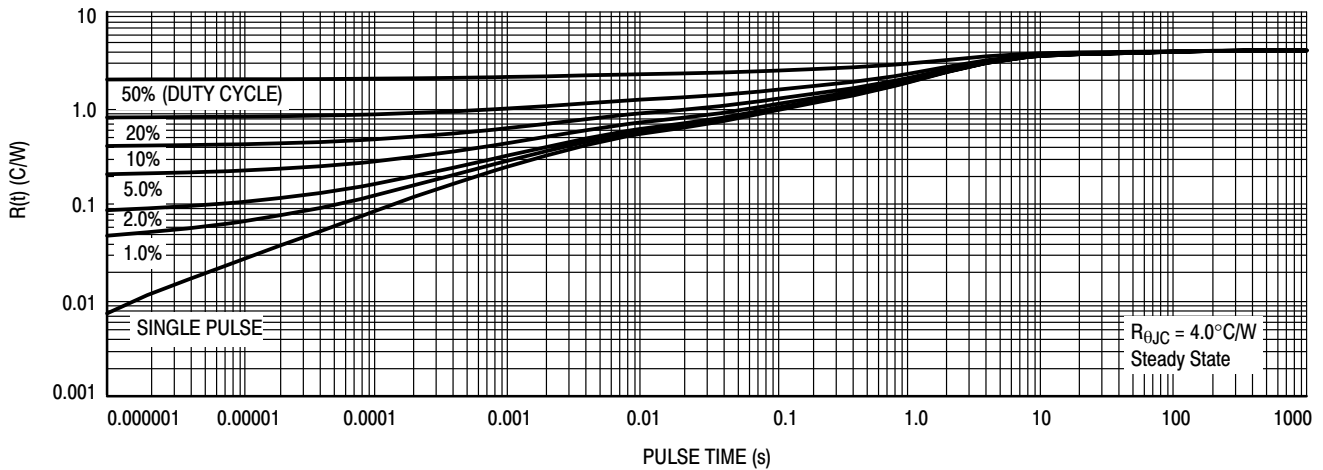
**Figure 11. Diode Forward Voltage versus Current**

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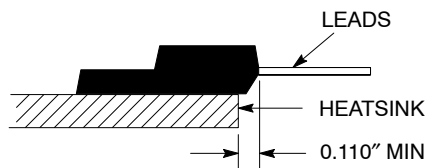
## TYPICAL CHARACTERISTICS



**Figure 12. Maximum Rated Forward Biased Safe Operating Area NDF08N50Z**



**Figure 13. Thermal Impedance (Junction-to-Case) for NDF08N50Z**



**Figure 14. Isolation Test Diagram**

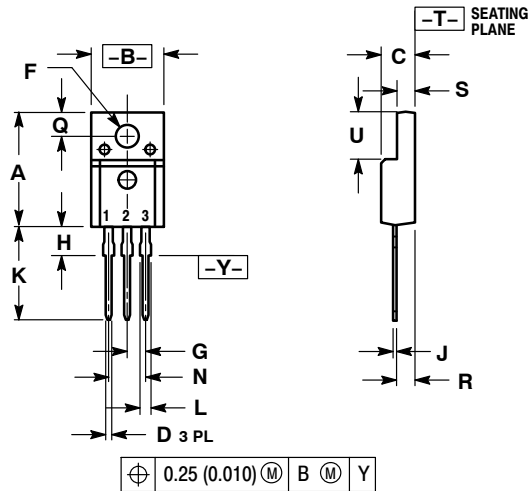
Measurement made between leads and heatsink with all leads shorted together.

\*For additional mounting information, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NDF08N50Z, NDP08N50Z

## PACKAGE DIMENSIONS

### TO-220 FULLPAK CASE 221D-03 ISSUE K

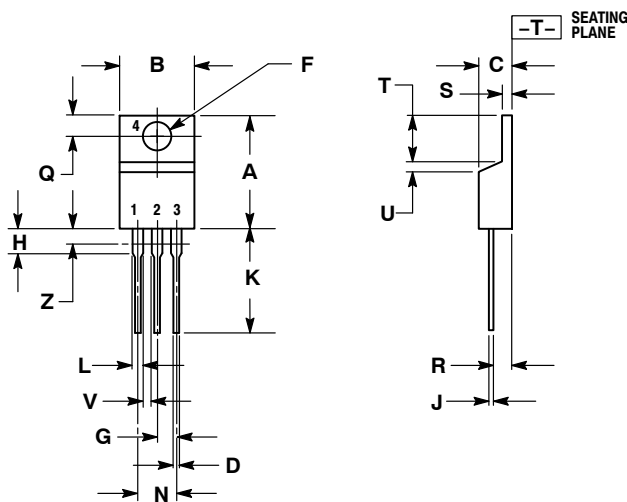


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH
  3. 221D-01 THRU 221D-02 OBSOLETE, NEW STANDARD 221D-03.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.617	0.635	15.67	16.12
B	0.392	0.419	9.96	10.63
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100 BSC		2.54 BSC	
H	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200 BSC		5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88

- STYLE 1:
1. GATE
  2. DRAIN
  3. SOURCE

### TO-220 CASE 221A-09 ISSUE AF



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

- STYLE 5:
1. GATE
  2. DRAIN
  3. SOURCE
  4. DRAIN

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