



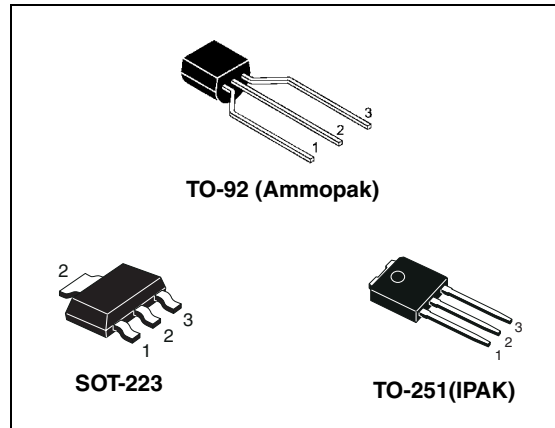
STD1LNK60Z-1 STQ1NK60ZR-AP - STN1NK60Z

N-channel 600V - 13Ω - 0.8A - TO-92 - TO-251 - SOT-223
Zener-Protected SuperMESH™ Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)}	I _D	P _w
STD1LNK60Z-1	600V	<15Ω	0.8A	25W
STQ1NK60ZR-AP	600V	<15Ω	0.3A	3W
STN1NK60Z	600V	<15Ω	0.3A	3.3W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- ESD improved capability
- New high voltage benchmark



Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

Application

- Switching applications

Figure 1. Internal schematic diagram

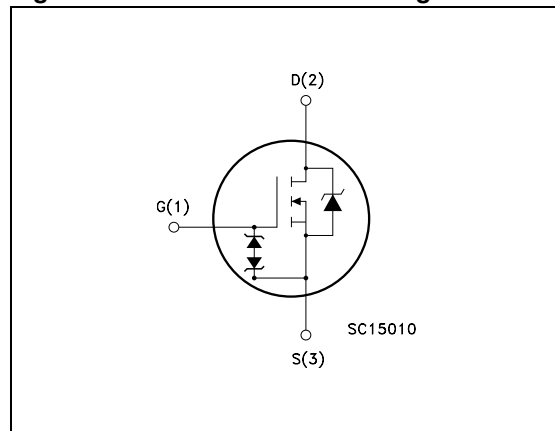


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD1LNK60Z-1	D1LNK60Z	TO-251 (IPAK)	Tube
STQ1NK60ZR-AP	1NK60ZR	TO-92	Ammopak
STN1NK60Z	1NK60Z	SOT-223	Tape & reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		I _{PAK}	TO-92	SOT-223	
V _{DS}	Drain-source voltage (V _{GS} = 0)	600			V
V _{GS}	Gate-source voltage	± 30			V
I _D	Drain current (continuous) at T _C = 25°C	0.8	0.3	0.3	A
I _D	Drain current (continuous) at T _C =100°C	0.5	0.189		A
I _{DM} ⁽¹⁾	Drain current (pulsed)	3.2	1.2		A
P _{TOT}	Total dissipation at T _C = 25°C	25	3	3.3	W
	Derating factor	0.24	0.25	0.26	W/°C
V _{ESD(G-D)}	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	800			V
dv/dt ⁽²⁾	Peak diode recovery voltage slope	4.5			V/ns
T _J T _{stg}	Operating junction temperature Storage temperature	-55 to 150			°C

1. Pulse width limited by safe operating area
2. I_{SD} ≤ 0.3A, di/dt ≤ 200A/μs, V_{DD} = 80%V_{(BR)DSS}

Table 3. Thermal resistance

Symbol	Parameter	Value			Unit
		I _{PAK}	TO-92	SOT-223	
R _{thj-case}	Thermal resistance junction-case Max	5	--	--	°C/W
R _{thj-a}	Thermal resistance junction-ambient Max	100	120	37.87 ⁽¹⁾	°C/W
R _{thj-lead}	Thermal resistance junction-lead Max	--	40	--	°C/W
T _I	Maximum lead temperature for soldering purpose	275	260		°C

1. When mounted on 1 inch² FR-4 board, 2 Oz Cu

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T _J Max)	0.8	A
E _{AS}	Single pulse avalanche energy (starting T _J =25°C, I _d =I _{ar} , V _{dd} =50V)	60	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1mA, V_{GS} = 0$	600			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating} @ 125^{\circ}C$			1 50	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20V$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 50\mu A$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 0.4A$		13	15	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15V, I_D = 0.4A$		0.5		S
C_{iss}	Input capacitance	$V_{DS} = 25V, f = 1\text{ MHz}, V_{GS} = 0$		94		pF
C_{oss}	Output capacitance			17.6		pF
C_{rss}	Reverse transfer capacitance			2.8		pF
$C_{oss\ eq}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0V \text{ to } 480V$		11		pF
Q_g	Total gate charge	$V_{DD} = 480V, I_D = 0.8A$		4.9	6.9	nC
Q_{gs}	Gate-source charge	$V_{GS} = 10V$		1		nC
Q_{gd}	Gate-drain charge	(see Figure 21)		2.7		nC

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2. $C_{oss\ eq}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=300\text{ V}$, $I_D=0.4\text{ A}$, $R_G=4.7\Omega$, $V_{GS}=10\text{ V}$ <i>(see Figure 20)</i>		5.5		ns
t_r	Rise time			5		ns
$t_{d(off)}$	Turn-off delay time			13		ns
t_f	Fall time			28		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				0.8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				2.4	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=0.8\text{ A}$, $V_{GS}=0$			1.6	V
t_{rr}	Reverse recovery time	$I_{SD}=0.8\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=20\text{ V}$, $T_j=25^\circ\text{C}$		135		ns
Q_{rr}	Reverse recovery charge			216		nC
I_{RRM}	Reverse recovery current			3.2		A
t_{rr}	Reverse recovery time	$I_{SD}=0.8\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=20\text{ V}$, $T_j=150^\circ\text{C}$		140		ns
Q_{rr}	Reverse recovery charge			224		nC
I_{RRM}	Reverse recovery current			3.2		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300μs, duty cycle 1.5%

Table 9. Gate-source zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}^{(1)}$	Gate-source breakdown voltage	$I_{GS}=\pm 1\text{ mA}$ (open drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for IPAK

Figure 3. Thermal impedance for IPAK

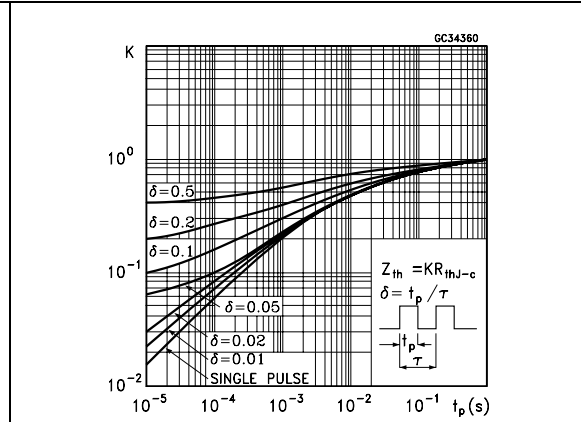
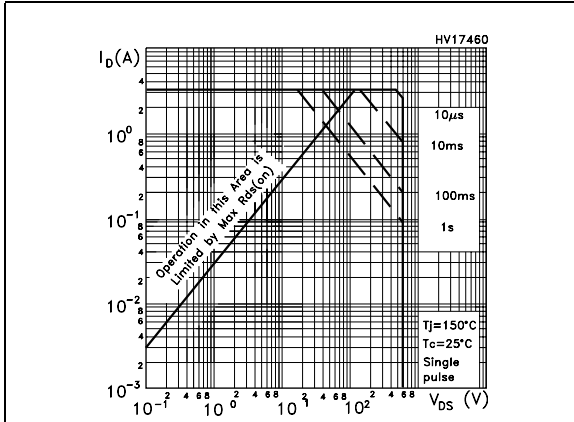


Figure 4. Safe operating area for TO-92

Figure 5. Thermal impedance for TO-92

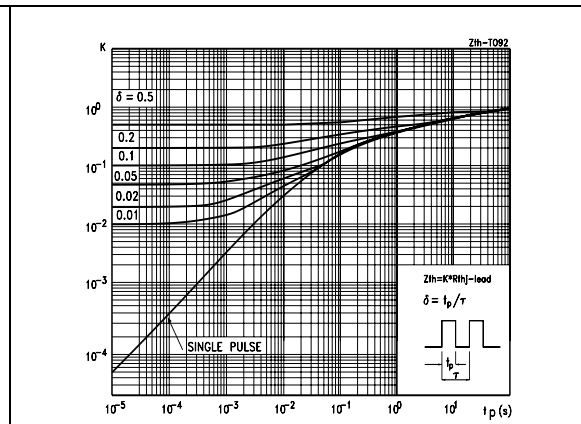
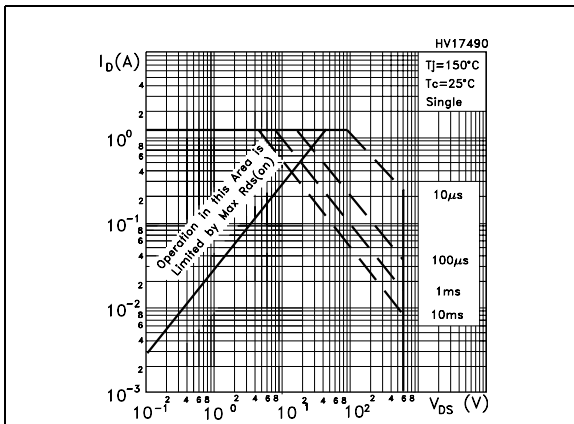


Figure 6. Safe operating area for SOT-223

Figure 7. Thermal impedance for SOT-223

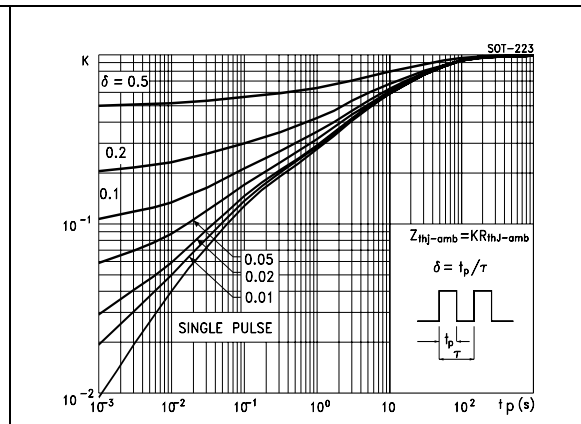
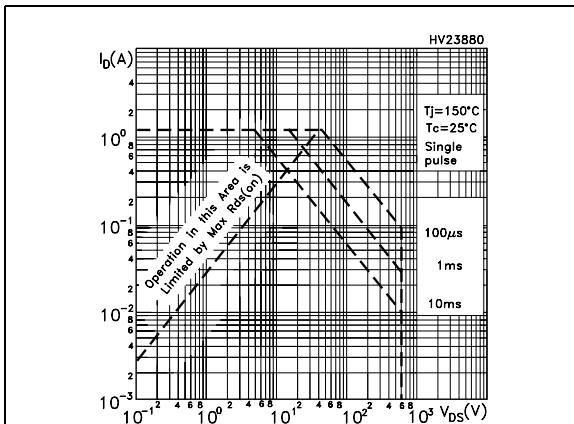


Figure 8. Output characteristics

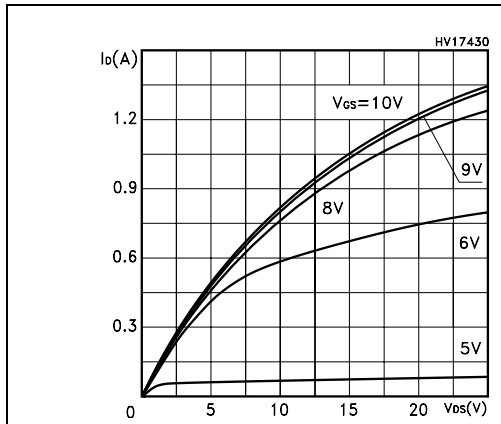


Figure 9. Transfer characteristics

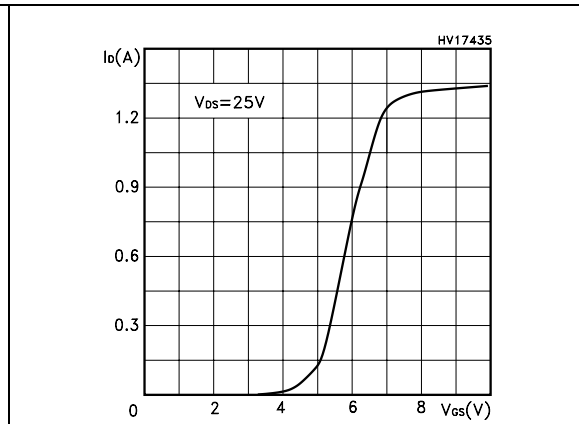


Figure 10. Transconductance

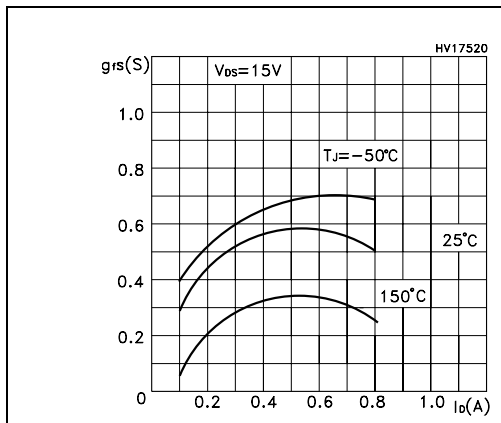


Figure 11. Static drain-source on resistance

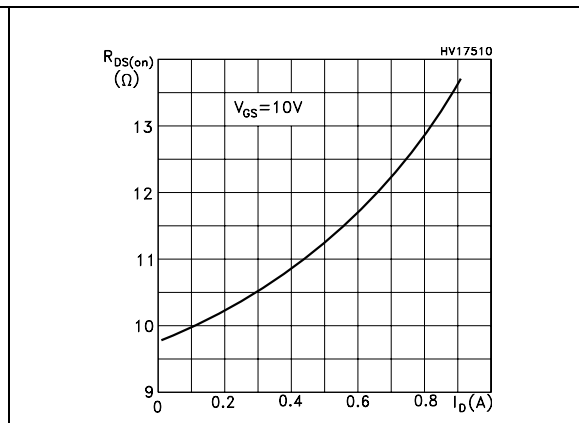


Figure 12. Gate charge vs gate-source voltage

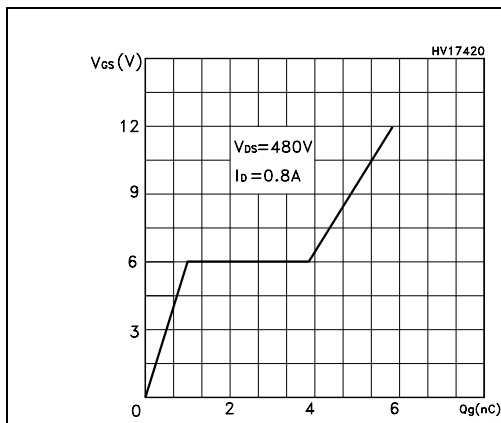


Figure 13. Capacitance variations

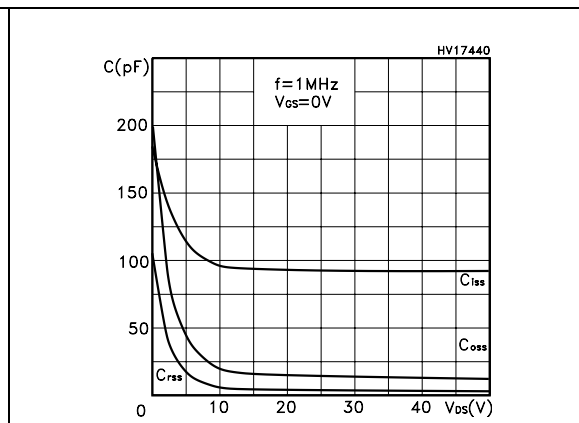


Figure 14. Normalized gate threshold voltage vs temperature

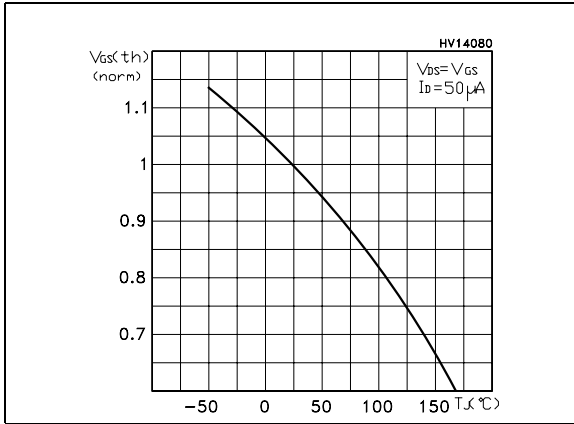


Figure 15. Normalized on resistance vs temperature

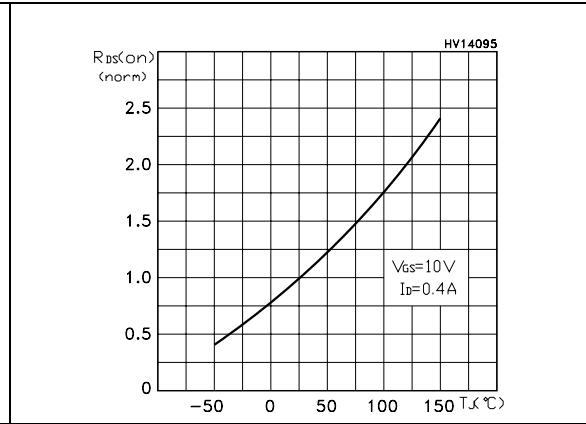


Figure 16. Source-drain diode forward characteristics

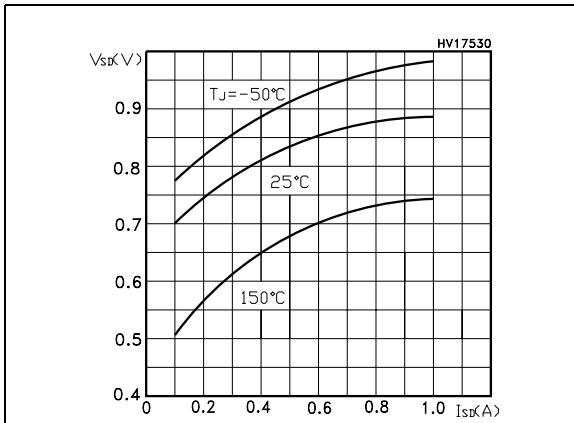


Figure 17. Normalized BV_{DSS} vs temperature

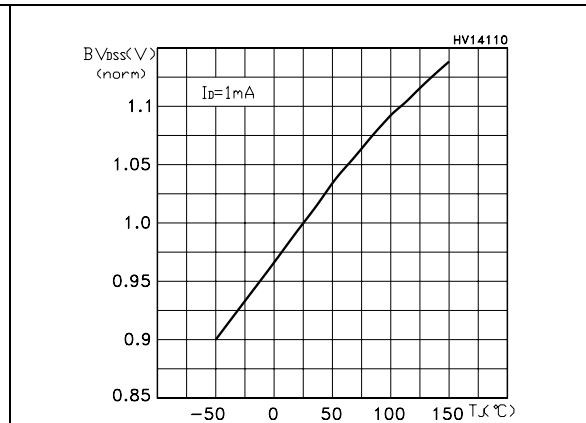


Figure 18. Maximum avalanche energy vs temperature

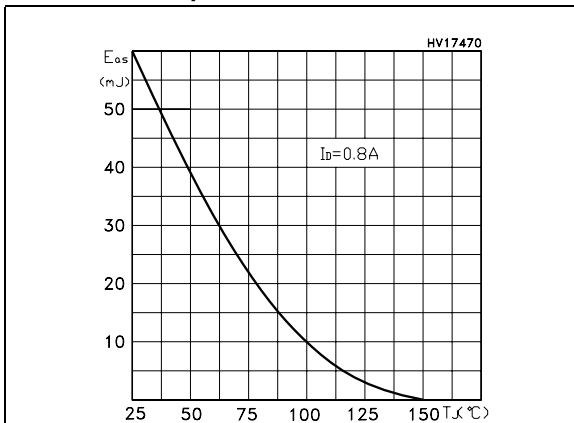
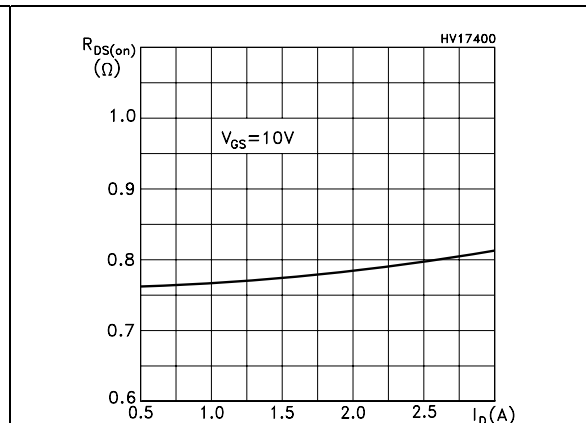


Figure 19. Max Id Current vs Tc



3 Test circuit

Figure 20. Switching times test circuit for resistive load

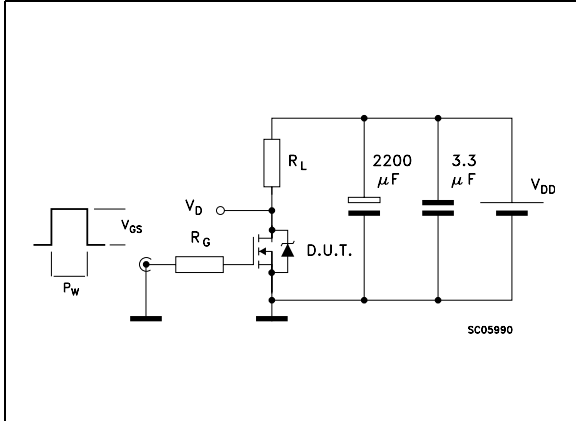


Figure 21. Gate charge test circuit

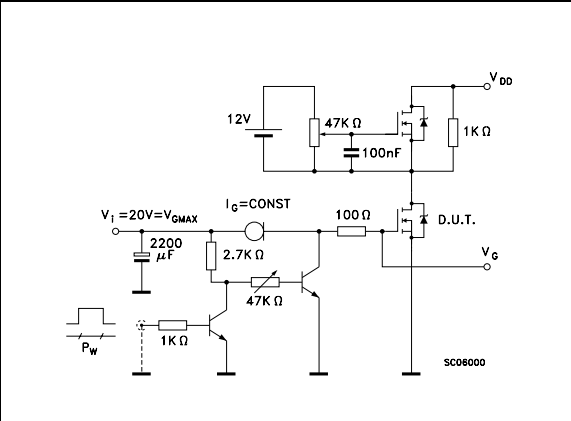


Figure 22. Test circuit for inductive load switching and diode recovery times

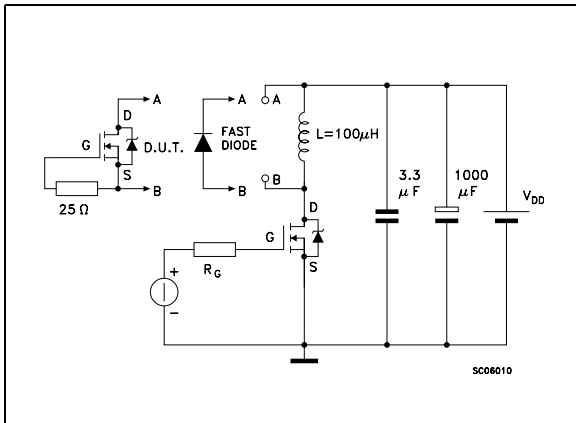


Figure 23. Unclamped inductive load test circuit

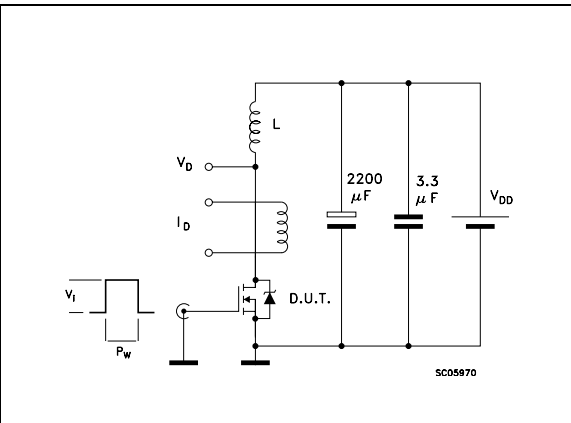


Figure 24. Unclamped inductive waveform

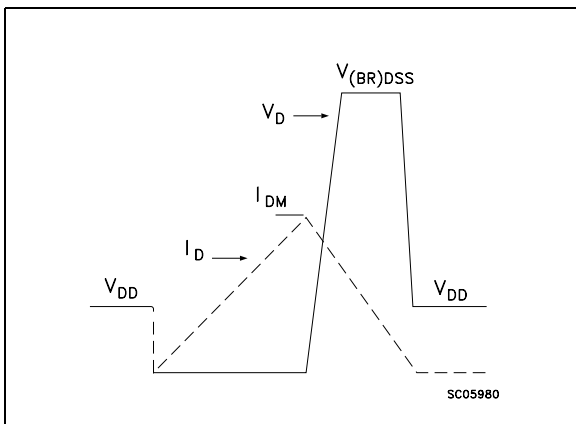
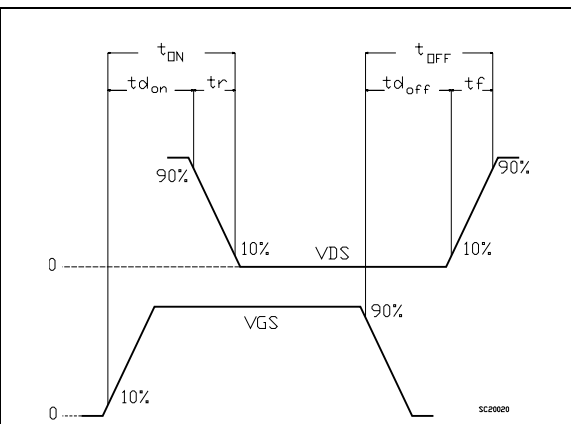


Figure 25. Switching time waveform

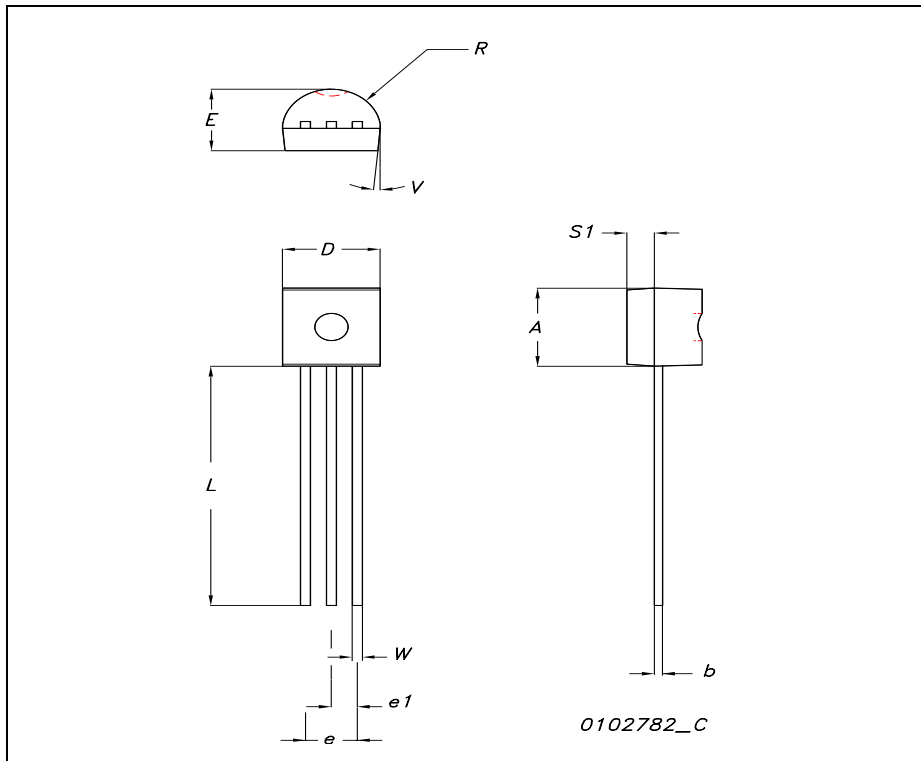


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

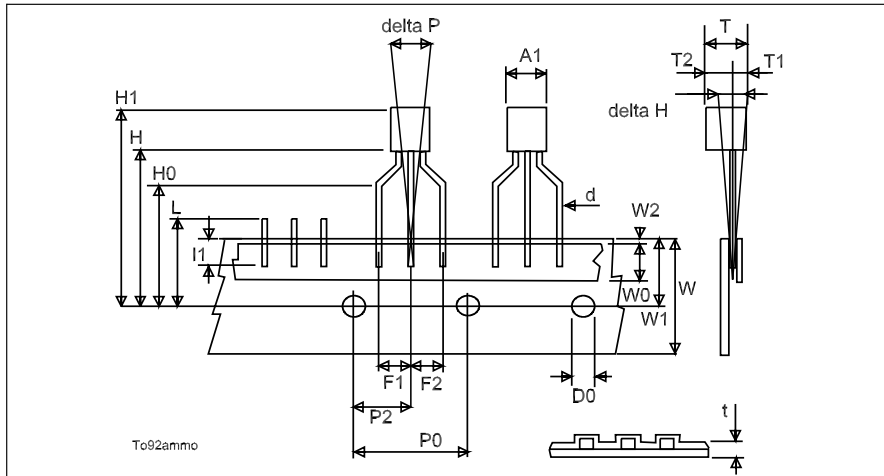
TO-92 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.32		4.95	0.170		0.194
b	0.36		0.51	0.014		0.020
D	4.45		4.95	0.175		0.194
E	3.30		3.94	0.130		0.155
e	2.41		2.67	0.094		0.105
e1	1.14		1.40	0.044		0.055
L	12.70		15.49	0.50		0.610
R	2.16		2.41	0.085		0.094
S1	0.92		1.52	0.036		0.060
W	0.41		0.56	0.016		0.022
V		5°			5°	



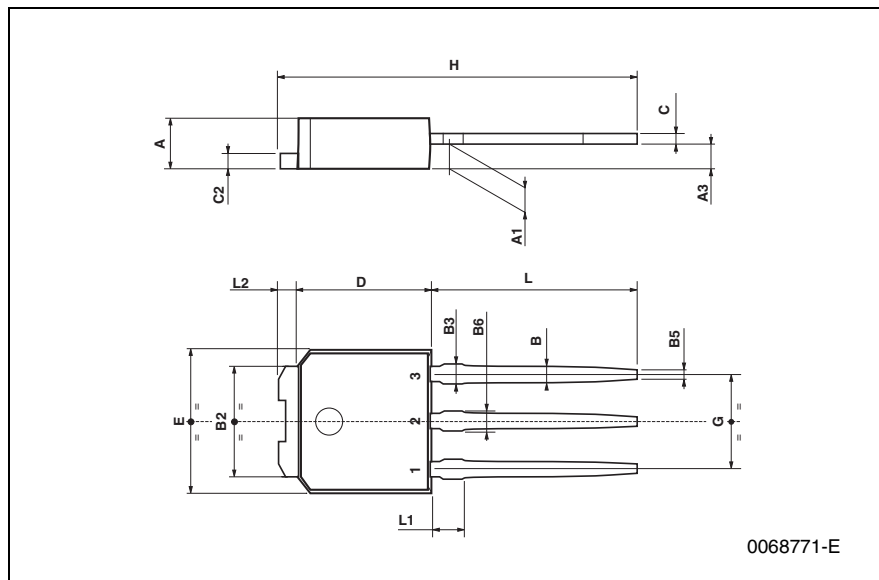
TO-92 AMMOPACK

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A1	4.45		4.95	0.170		0.194
T	3.30		3.94	0.130		0.155
T1			1.6			0.06
T2			2.3			0.09
d	0.41		0.56	0.016		0.022
P0	12.5	12.7	12.9	0.49	0.5	0.51
P2	5.65	6.35	7.05	0.22	0.25	0.27
F1, F2	2.44	2.54	2.94	0.09	0.1	0.11
delta H	-2		2	-0.08		0.08
W	17.5	18	19	0.69	0.71	0.74
W0	5.7	6	6.3	0.22	0.23	0.24
W1	8.5	9	9.25	0.33	0.35	0.36
W2			0.5			0.02
H	18.5		20.5	0.72		0.80
H0	15.5	16	16.5	0.61	0.63	0.65
H1			25			0.98
D0	3.8	4	4.2	0.15	0.157	0.16
t			0.9			0.035
L			11			0.43
I1	3			0.11		
delta P	-1		1	-0.04		0.04



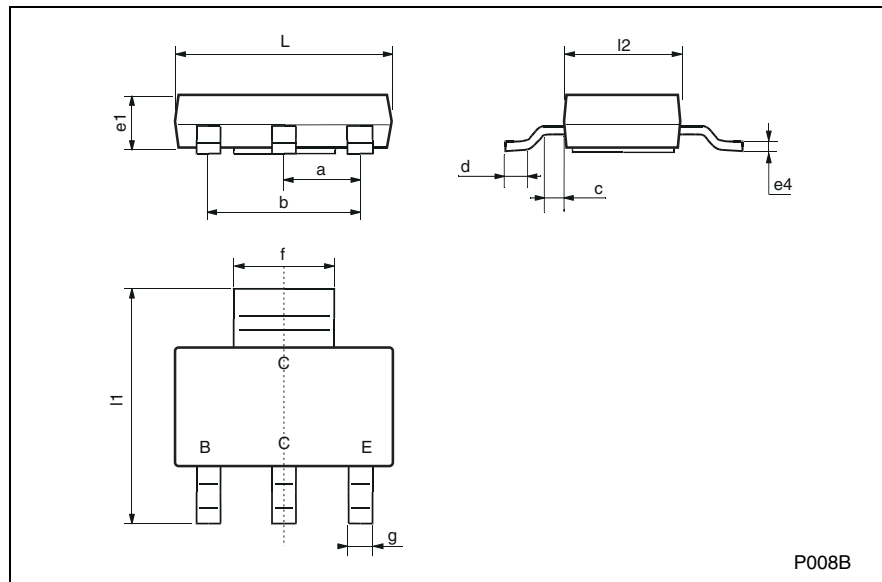
TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



SOT-223 MECHANICAL DATA

DIM.	mm			mils		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a	2.27	2.3	2.33	89.4	90.6	91.7
b	4.57	4.6	4.63	179.9	181.1	182.3
c	0.2	0.4	0.6	7.9	15.7	23.6
d	0.63	0.65	0.67	24.8	25.6	26.4
e1	1.5	1.6	1.7	59.1	63	66.9
e4			0.32			12.6
f	2.9	3	3.1	114.2	118.1	122.1
g	0.67	0.7	0.73	26.4	27.6	28.7
l1	6.7	7	7.3	263.8	275.6	287.4
l2	3.5	3.5	3.7	137.8	137.8	145.7
L	6.3	6.5	6.7	248	255.9	263.8



5 Revision history

Table 10. Revision history

Date	Revision	Changes
19-Mar-2003	3	First electronic version
15-May-2003	4	Removed DPAK
09-Jun-2003	5	Final datasheet
17-Nov-2004	6	Inserted SOT-223
15-Feb-2005	7	Modified Figure 4 .
07-Sep-2005	8	Inserted ecopack indication
22-Feb-2006	9	The document has been reformatted
01-Jun-2007	10	Order code table on first page has been updated
19-Jul-2007	11	Table 1.: Device summary has been updated

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