



# STP4N150 STW4N150

N-channel 1500V - 5Ω - 4A - TO-220/TO-247  
Very high PowerMESH™ Power MOSFET

## General features

Type	V <sub>DSS</sub> (@T <sub>jmax</sub> )	R <sub>DS(on)</sub>	I <sub>D</sub>
STP4N150	1500 V	< 7 Ω	4A
STW4N150	1500 V	< 7 Ω	4A

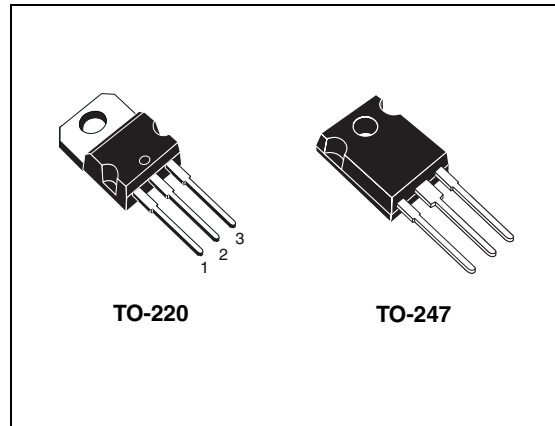
- Avalanche ruggedness
- Gate charge minimized
- Very low intrinsic capacitances
- High speed switching

## Description

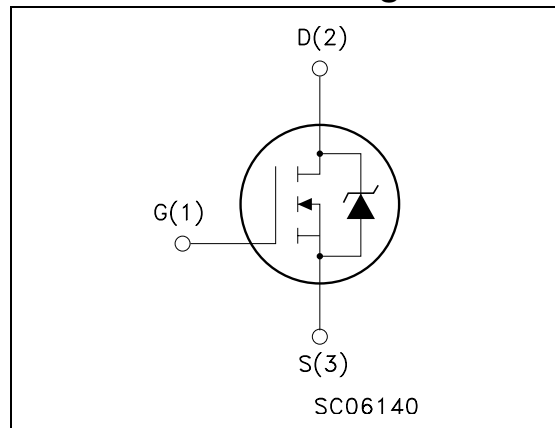
Using the well consolidated high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of Power MOSFETs with outstanding performances. The strengthened layout coupled with the Company's proprietary edge termination structure, gives the lowest RDS(on) per area, unrivalled gate charge and switching characteristics.

## Applications

- Switching application



## Internal schematic diagram



## Order codes

Part number	Marking	Package	Packaging
STP4N150	P4N150	TO-220	Tube
STW4N150	W4N150	TO-247	Tube

## Contents

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	1500	V
$V_{DGR}$	Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	1500	V
$V_{GS}$	Gate- source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	4	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	2.5	A
$I_{DM}^{(1)}$	Drain current (pulsed)	12	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	160	W
	Derating factor	1	W/ $^\circ\text{C}$
$T_j$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area

**Table 2. Thermal data**

Symbol	Parameter	Value		Unit
		TO-220	TO-247	
Rthj-case	Thermal resistance junction-case max	0.78		$^\circ\text{C}/\text{W}$
Rthj-amb	Thermal resistance junction-ambient max	62.5	50	$^\circ\text{C}/\text{W}$

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j \text{ max}$ )	4	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50 \text{ V}$ )	350	mJ

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	1500			V
$I_{DSS}$	Zero gate voltage Drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}, T_C = 125^{\circ}C$			10 500	$\mu A$ $\mu A$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 30 \text{ V}$			$\pm 100$	$\mu A$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}, I_D = 2 \text{ A}$		5	7	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 30 \text{ V}, I_D = 2 \text{ A}$		3.5		S
$C_{iss}$	Input capacitance	$V_{DS} = 25 \text{ V}, f = 1 \text{ MHz},$ $V_{GS} = 0$		1300		pF
$C_{oss}$	Output capacitance			120		pF
$C_{rss}$	Reverse transfer capacitance			12		pF
$T_{d(on)}$	Turn-on delay time	$V_{DD} = 750 \text{ V}, I_D = 2 \text{ A},$ $R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$ (see Figure 18)		35		ns
$T_r$	Rise time			30		ns
$t_{d(off)}$	Turn-off delay time			45		ns
$t_f$	Fall time			45		ns
$Q_g$	Total gate charge	$V_{DD} = 600 \text{ V}, I_D = 4 \text{ A},$ $V_{GS} = 10 \text{ V}$ (see Figure 19)		30	50	nC
$Q_{gs}$	Gate-source charge			10		nC
$Q_{gd}$	Gate-drain charge			9		nC

1. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current				4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				12	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 4 \text{ A}, V_{GS} = 0$			2	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 4 \text{ A}, di/dt = 100$ $\text{A}/\mu\text{s}$		510		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 45\text{V}$		3		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 18)		12		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 4 \text{ A}, di/dt = 100$ $\text{A}/\mu\text{s}$		615		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 45\text{V}, T_j = 150^\circ\text{C}$		4		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 18)		12.6		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220

Figure 2. Thermal impedance for TO-220

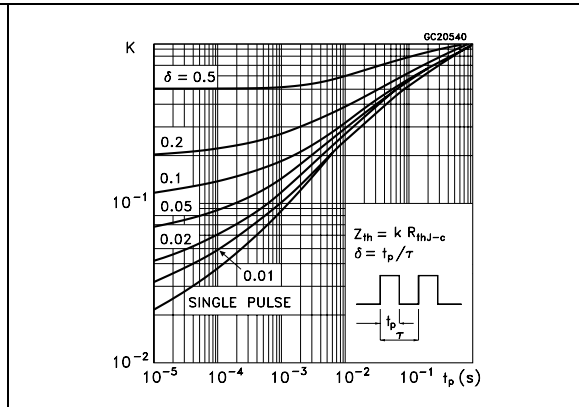
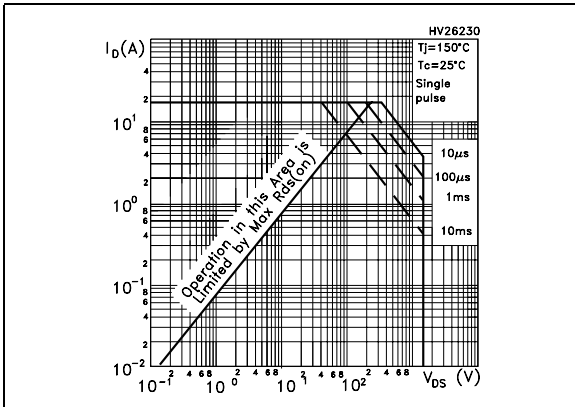


Figure 3. Safe operating area for TO-247

Figure 4. Thermal impedance for TO-247

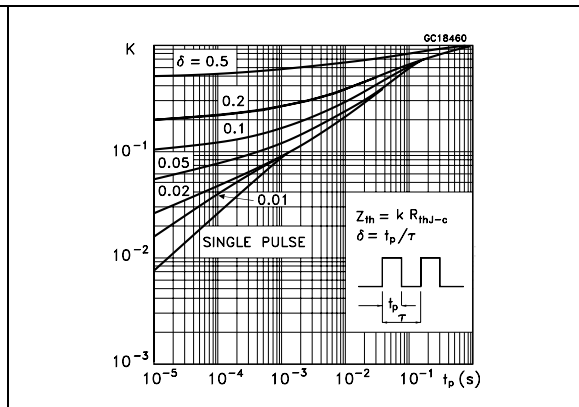
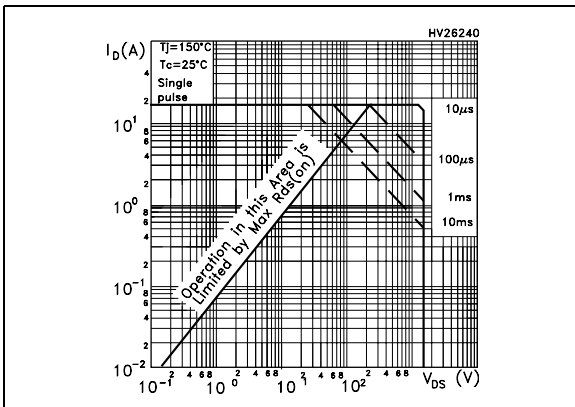


Figure 5. Output characteristics

Figure 6. Transfer characteristics

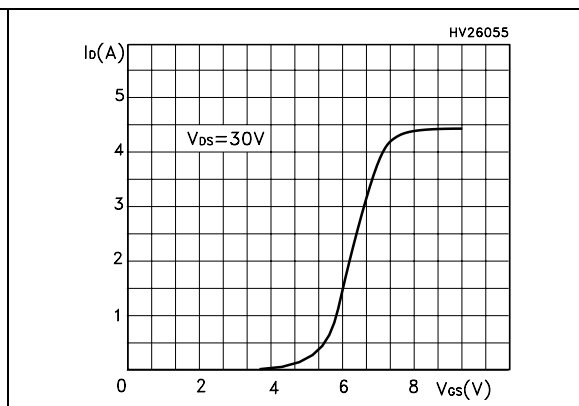
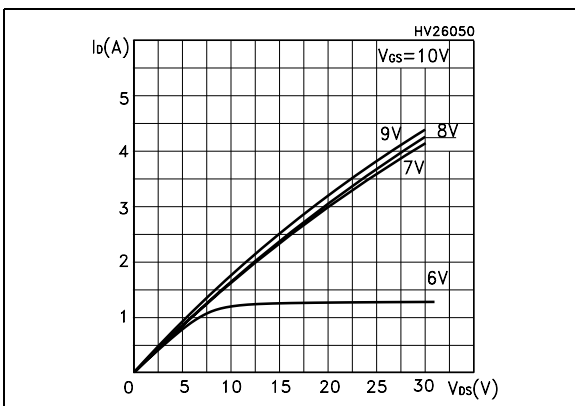


Figure 7. Transconductance

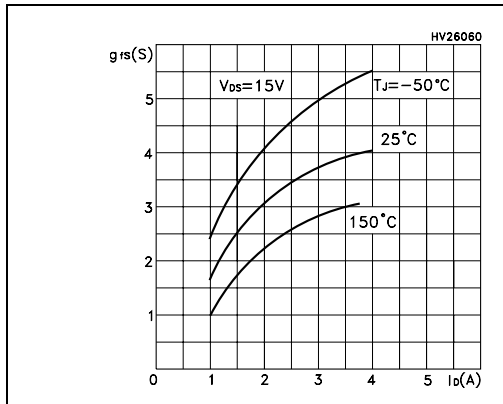


Figure 8. Static drain-source on resistance

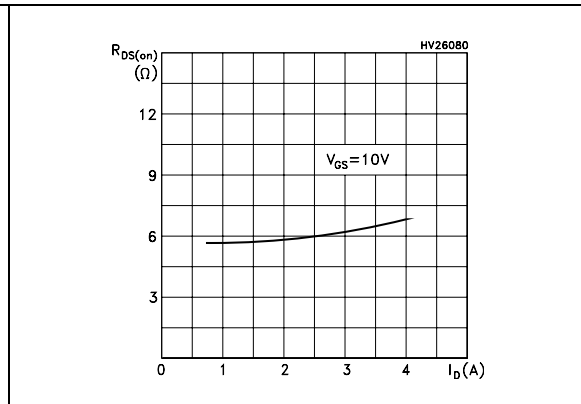


Figure 9. Gate charge vs gate-source voltage

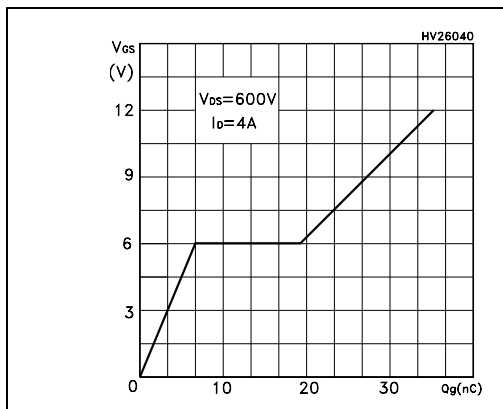


Figure 10. Capacitance variations

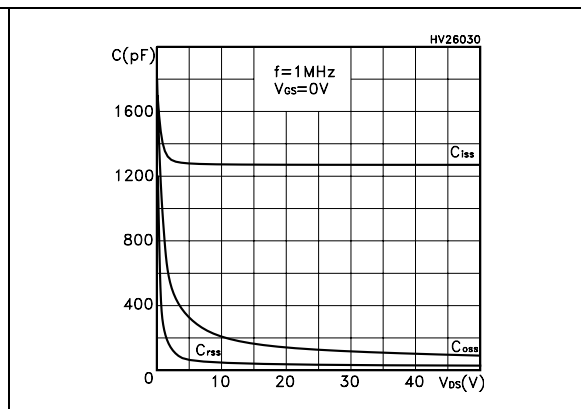


Figure 11. Normalized gate threshold voltage vs temperature

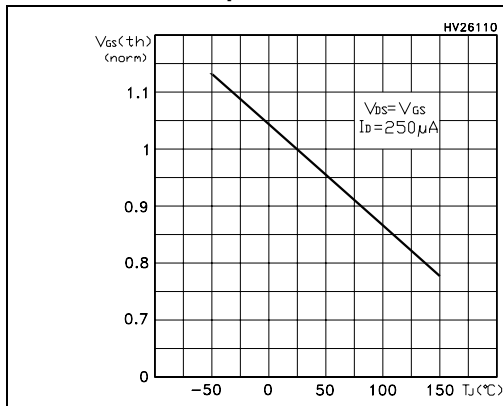


Figure 12. Normalized on resistance vs temperature

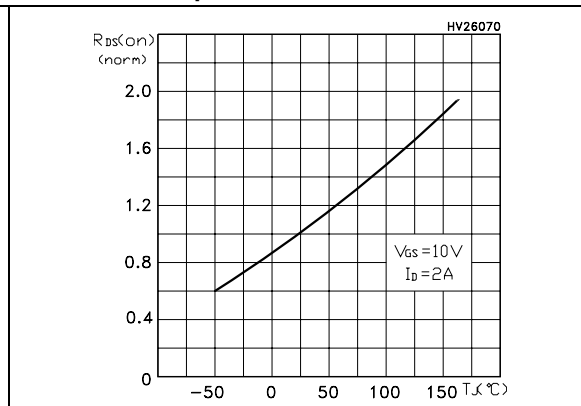


Figure 13. Source-drain diode forward characteristics

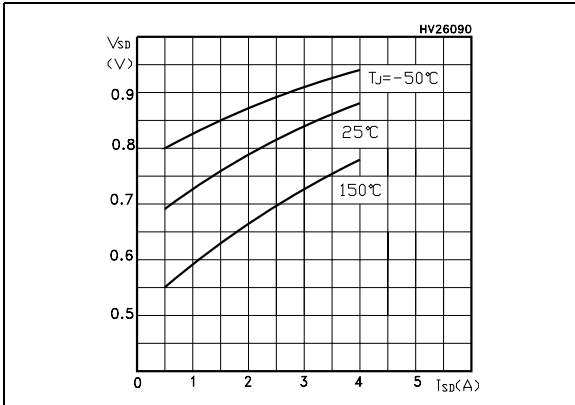


Figure 14. Normalized  $B_{VDSS}$  vs temperature

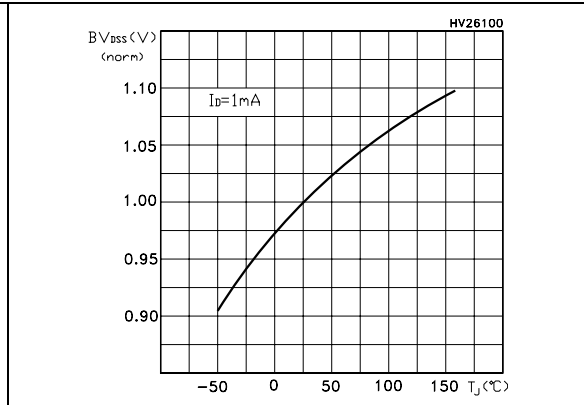
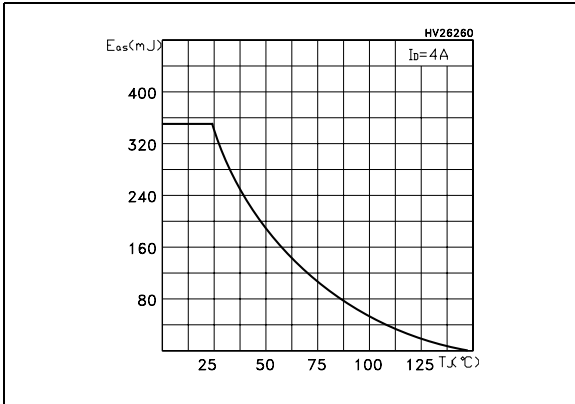


Figure 15. Maximum avalanche energy vs temperature





### 3 Test circuit Package mechanical data

Figure 16. Unclamped inductive load test circuit

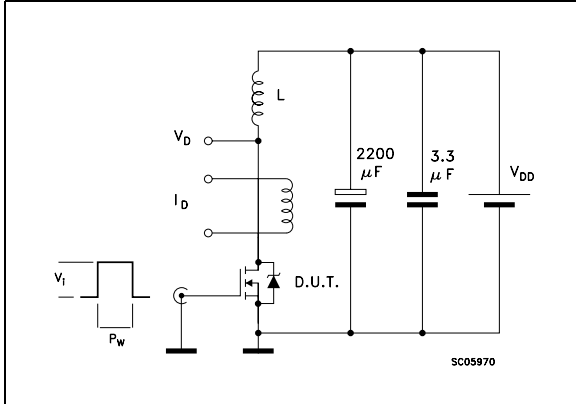


Figure 17. Unclamped inductive waveform

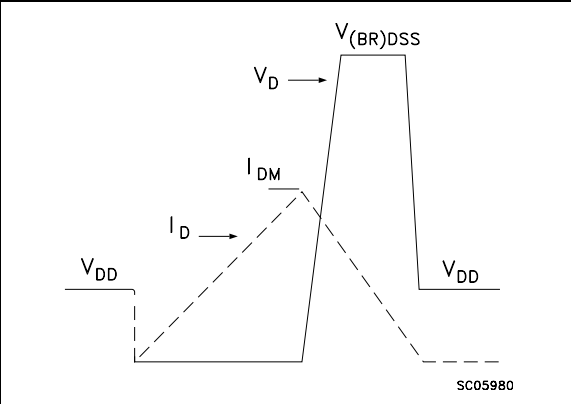


Figure 18. Switching times test circuit for resistive load

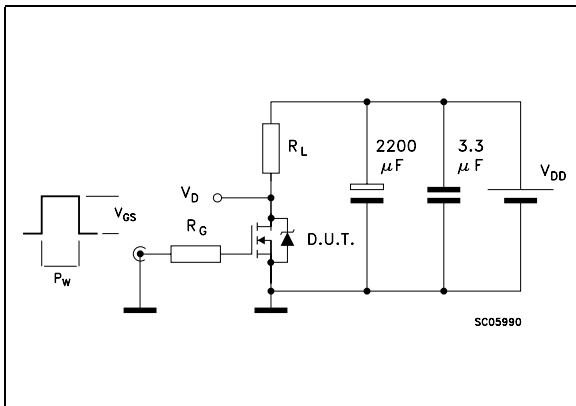


Figure 19. Gate charge test circuit

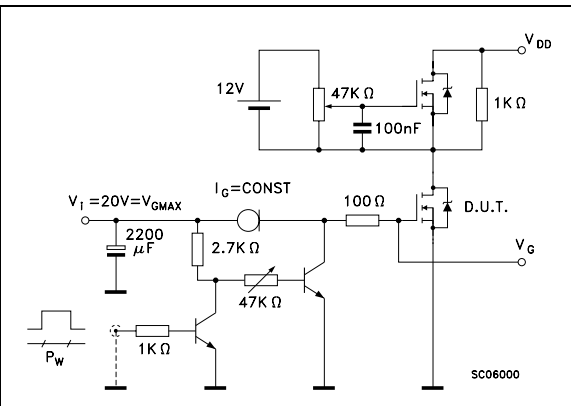
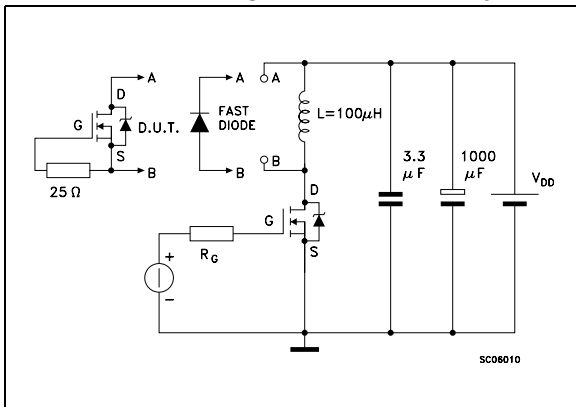


Figure 20. Test circuit for inductive load switching and diode recovery times

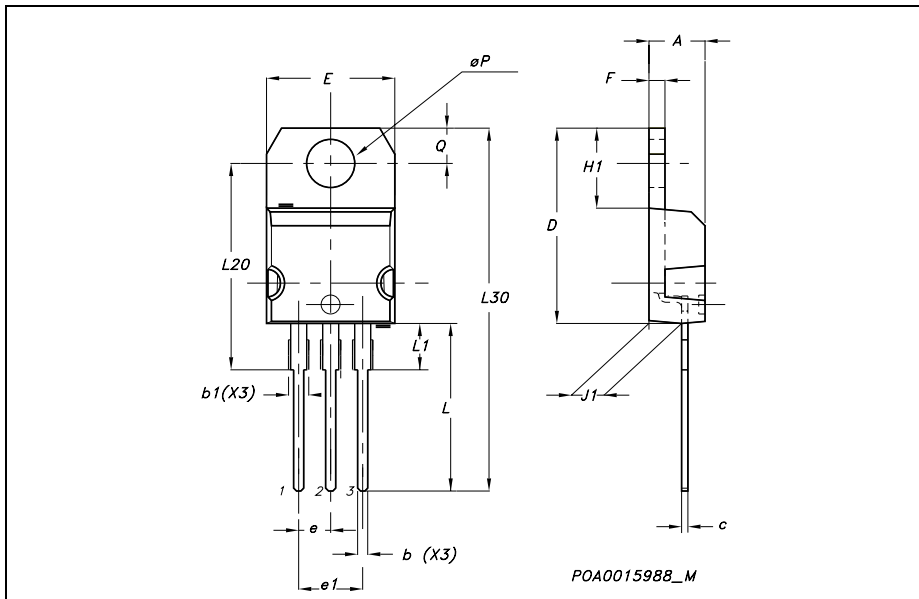


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

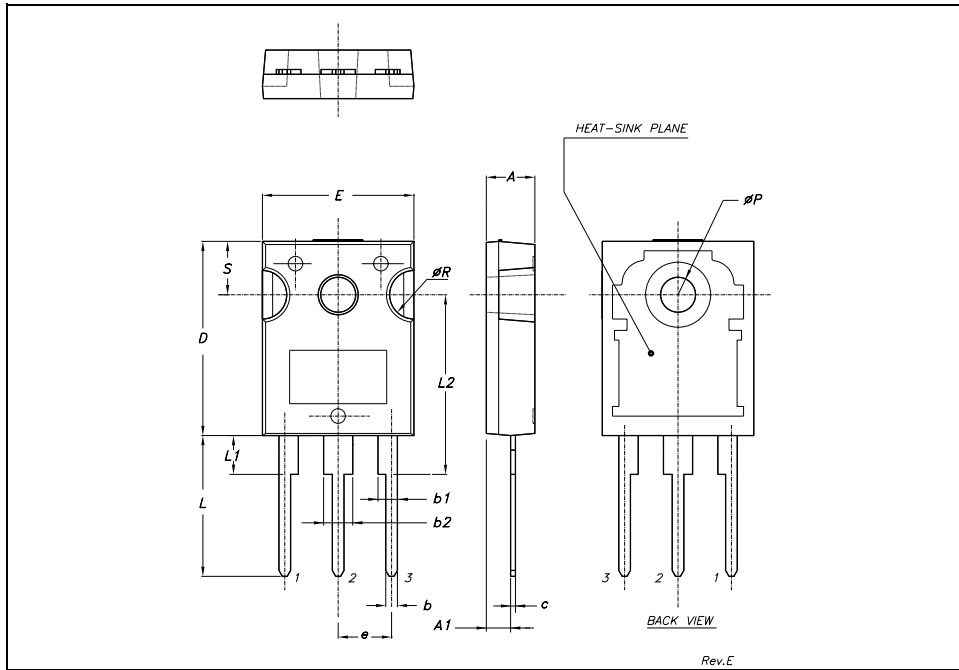
**TO-220 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



**TO-247 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



## 5 Revision history

Table 7. Revision history

Date	Revision	Changes
29-Mar-2005	1	First release
07-Jul-2005	2	Removed TO-220FP
07-Oct-2005	3	Complete version
10-Aug-2006	4	New template, no content change

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