



STP120NF10 - STB120NF10 STW120NF10

N-channel 100V - 0.009Ω - 110A - TO-247 - TO-220 - D²PAK
STripFET™ II Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STW120NF10	100V	<0.0105Ω	110A
STP120NF10	100V	<0.0105Ω	110A
STB120NF10	100V	<0.0105Ω	110A

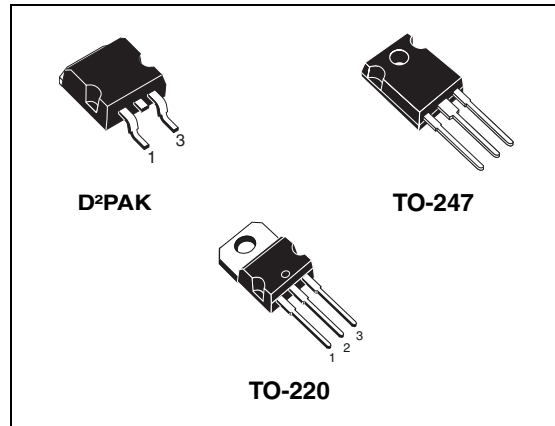
- Exceptional dv/dt capability
- 100% avalanche tested
- Application oriented characterization

Description

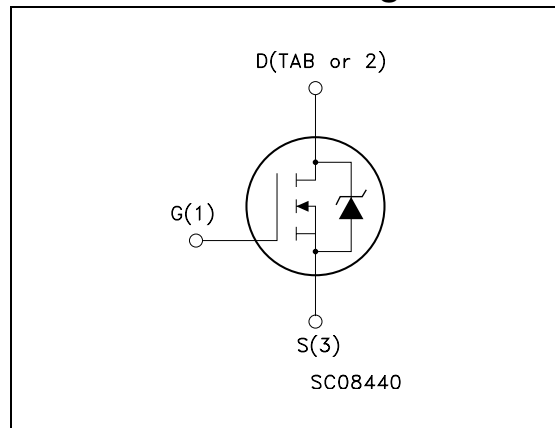
This Power MOSFET series realized with STMicroelectronics unique STripFET™ process has specifically been designed to minimize the on-resistance. It is therefore suitable as primary switch in advanced high-efficiency, high-frequency isolated DC-DC converters for Telecom and Computer application. It is also intended for any applications with low gate drive requirements.

Applications

- Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STW120NF10	W120NF10	TO-247	Tube
STP120NF10	P120NF10	TO-220	Tube
STB120NF10	B120NF10	D ² PAK	Tape & reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	100	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	110	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	77	A
$I_{DM}^{(1)}$	Drain current (pulsed)	440	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	312	W
	Derating factor	2.08	W/°C
dv/dt ⁽²⁾	Peak diode recovery voltage slope	10	V/ns
$E_{AS}^{(3)}$	Single pulse avalanche energy	550	mJ
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C
T_L	Maximum lead temperature for soldering purpose	300	°C

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 120\text{A}$, $di/dt \leq 300\text{A}/\mu\text{s}$, $V_{DD} = 80\%V_{(BR)DSS}$
3. Starting $T_J = 25^\circ\text{C}$, $I_D = 60\text{A}$, $V_{DD} = 50\text{V}$

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.48	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	°C/W

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu A, V_{GS} = 0$	100			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating} @ 125^{\circ}C$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20V$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 60A$		0.009	0.0105	Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 25V, I_D = 60A$		90		S
C_{iss}	Input capacitance	$V_{DS} = 25V, f = 1 \text{ MHz},$ $V_{GS} = 0$		5200		pF
C_{oss}	Output capacitance			785		pF
C_{rss}	Reverse transfer capacitance			325		pF
Q_g	Total gate charge	$V_{DD} = 80V, I_D = 120A$		172	233	nC
Q_{gs}	Gate-source charge	$V_{GS} = 10V$		32		nC
Q_{gd}	Gate-drain charge	(see Figure 13)		64		nC

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=50V, I_D=60A,$ $R_G=4.7\Omega, V_{GS}=10V$ <i>(see Figure 12)</i>		25		ns
t_r	Rise time			90		ns
$t_{d(off)}$	Turn-off delay time			132		ns
t_f	Fall time			68		ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				110	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				440	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=120A, V_{GS}=0$			1.3	V
t_{rr}	Reverse recovery time	$I_{SD}=120A,$ $di/dt = 100A/\mu s,$ $V_{DD}=40V, T_J=150^\circ C$ <i>(see Figure 17)</i>		152		ns
Q_{rr}	Reverse recovery charge			760		nC
I_{RRM}	Reverse recovery current			10		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark.

TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	

