MJE13005

Preferred Device

SWITCHMODE™ Series NPN Silicon Power Transistors

These devices are designed for high−voltage, high−speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V SWITCHMODE applications such as Switching Regulator's, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

Features

- $V_{CEO(sus)}$ 400 V
- Reverse Bias SOA with Inductive Loads @ T_C = 100°C
- Inductive Switching Matrix 2 to 4 A, 25 and 100°C t_c @ 3A, 100°C is 180 ns (Typ)
- 700 V Blocking Capability
- SOA and Switching Applications Information
- Pb−Free Package is Available*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector−Emitter Voltage	V_{CEV}	700	Vdc
Emitter−Base Voltage	V_{EBO}	9	Vdc
Collector Current − Continuous − Peak (Note 1)	I_C I_{CM}	4 8	Adc
Base Current − Continuous − Peak (Note 1)	I_B I_{BM}	2 4	Adc
Emitter Current − Continuous − Peak (Note 1)	I_E I_{EM}	6 12	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	2 16	W W/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 600	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 5 Seconds	T_L	275	°C

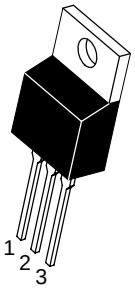
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

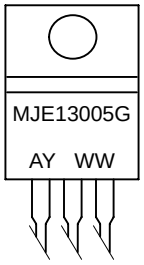
ON Semiconductor®

4 AMPERE NPN SILICON POWER TRANSISTOR 400 VOLTS − 75 WATTS



TO−220AB
CASE 221A−09
STYLE 1

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping
MJE13005	TO−220	50 Units / Rail
MJE13005G	TO−220 (Pb−Free)	50 Units / Rail

Preferred devices are recommended choices for future use and best overall value.

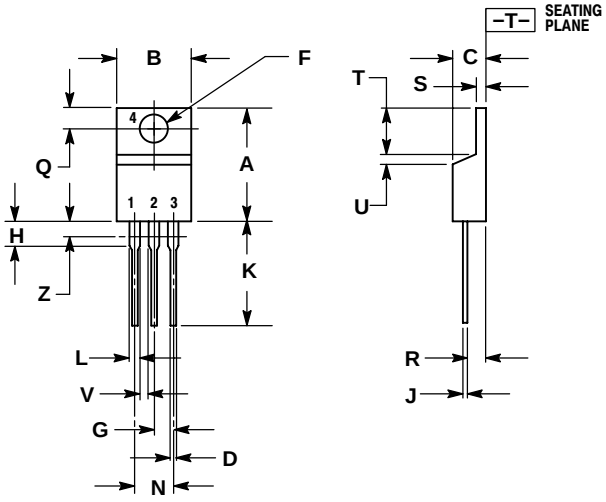
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (Note 2)						
Collector−Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0)		$V_{CEO(sus)}$	400	−	−	Vdc
Collector Cutoff Current		I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			−	−	1	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)			−	−	5	
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}	−	−	1	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	−	See Figure 11		
Clamped Inductive SOA with Base Reverse Biased		RBSOA	−	See Figure 12		
ON CHARACTERISTICS (Note 2)						
DC Current Gain		h_{FE}				−
(I_C = 1 Adc, V_{CE} = 5 Vdc)			10	−	60	
(I_C = 2 Adc, V_{CE} = 5 Vdc)			8	−	40	
Collector−Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 1 Adc, I_B = 0.2 Adc)			−	−	0.5	
(I_C = 2 Adc, I_B = 0.5 Adc)			−	−	0.6	
(I_C = 4 Adc, I_B = 1 Adc)			−	−	1	
(I_C = 2 Adc, I_B = 0.5 Adc, T_C = 100°C)			−	−	1	
Base−Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 1 Adc, I_B = 0.2 Adc)			−	−	1.2	
(I_C = 2 Adc, I_B = 0.5 Adc)			−	−	1.6	
(I_C = 2 Adc, I_B = 0.5 Adc, T_C = 100°C)			−	−	1.5	
DYNAMIC CHARACTERISTICS						
Current−Gain − Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T	4	−	−	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	−	65	−	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 2)						
Delay Time	(V_{CC} = 125 Vdc, I_C = 2 A, I_{B1} = I_{B2} = 0.4 A, t_p = 25 μs, Duty Cycle ≤ 1%)	t_d	−	0.025	0.1	μs
Rise Time		t_r	−	0.3	0.7	μs
Storage Time		t_s	−	1.7	4	μs
Fall Time		t_f	−	0.4	0.9	μs
Inductive Load, Clamped (Table 2, Figure 13)						
Voltage Storage Time	(I_C = 2 A, V_{clamp} = 300 Vdc, I_{B1} = 0.4 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	−	0.9	4	μs
Crossover Time		t_c	−	0.32	0.9	μs
Fall Time		t_{fi}	−	0.16	−	μs

2. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

PACKAGE DIMENSIONS

TO−220AB
CASE 221A−09
ISSUE AA



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR