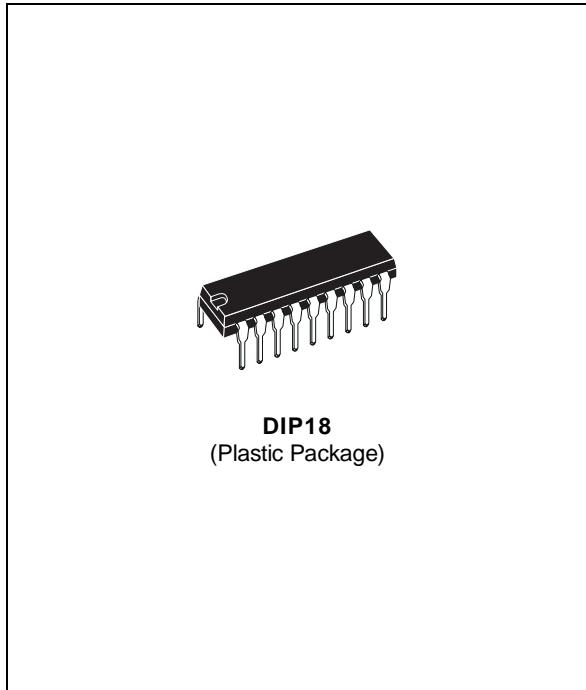


EIGHT DARLINGTON ARRAYS

- EIGHT DARLINGTONS PER PACKAGE
- EXTENDED TEMPERATURE RANGE
(- 40 to 105°C)
- OUTPUT CURRENT TO 500mA
- OUTPUT VOLTAGE TO 50V
- INTEGRAL SUPPRESSION DIODES
- VERSIONS FOR ALL POPULAR LOGIC FAMILIES
- OUTPUT CAN BE PARALLELED
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY BOARD LAYOUT



DIP18
(Plastic Package)

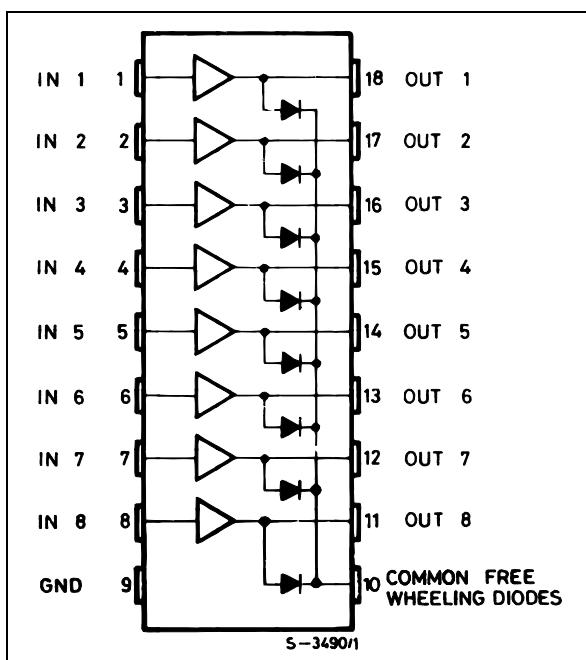
DESCRIPTION

The ULQ2801A-ULQ2805A each contain eight darlington transistors with common emitters and integral suppression diodes for inductive loads. Each darlington features a peak load current rating of 600mA (500mA continuous) and can withstand at least 50V in the off state. Outputs may be paralleled for higher current capability.

Five versions are available to simplify interfacing to standard logic families : the ULQ2801A is designed for general purpose applications with a current limit resistor ; the ULQ2802A has a 10.5kΩ input resistor and zener for 14-25V PMOS ; the ULQ2803A has a 2.7kΩ input resistor for 5V TTL and CMOS ; the ULQ2804A has a 10.5kΩ input resistor for 6-15V CMOS and the ULQ2805A is designed to sink a minimum of 350mA for standard and Schottky TTL where higher output current is required.

All types are supplied in a 18-lead plastic DIP with a copper lead frame and feature the convenient input-opposite-output pinout to simplify board layout.

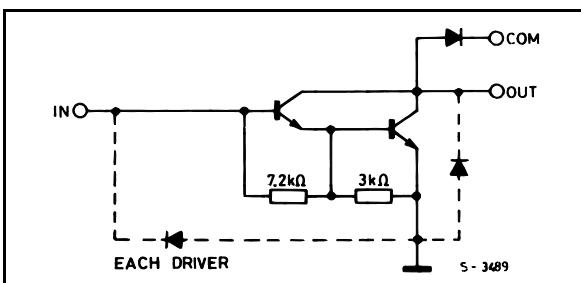
PIN CONNECTION (top view)



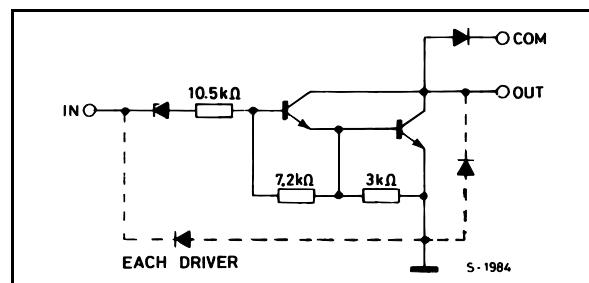
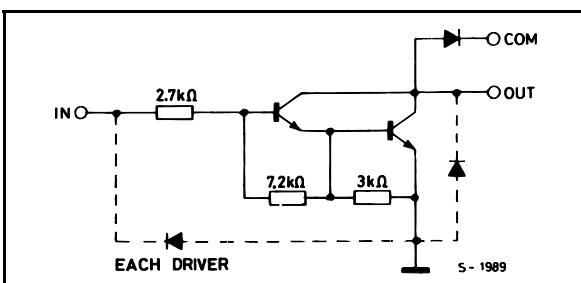
ULQ2801A - ULQ2802A - ULQ2803A - ULQ2804A - ULQ2805A

SCHEMATIC DIAGRAM AND ORDER CODES

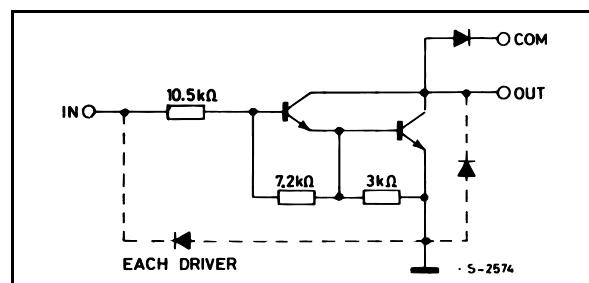
For ULQ2801A (each driver for PMOS-CMOS) For ULQ2802A (each driver for 14-15 V PMOS)



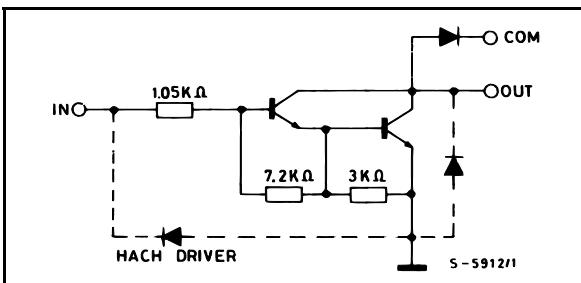
For ULQ2803A (each driver for 5 V, TTL/CMOS)



For ULQ2804A (each driver for 6-15 V CMOS/PMOS)



For ULQ2805A (each driver for high out TTL)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _o	Output Voltage	50	V
V _i	Input Voltage for ULQ2802A, 2803A, 2804A for ULQ2805A	30 15	V V
I _C	Continuous Collector Current	500	mA
I _B	Continuous Base Current	25	mA
P _{tot}	Power Dissipation (one Darlington pair) (total package)	1.0 2.25	W W
T _{amb}	Operating Ambient Temperature Range	- 40 to 105	°C
T _{stg}	Storage Temperature Range	- 55 to 150	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
R _{th j-amb}	Thermal Resistance Junction-ambient	Max.	55 °C/W

ULQ2801A - ULQ2802A - ULQ2803A - ULQ2804A - ULQ2805A

ELECTRICAL CHARACTERISTICS ($T_j = -40$ to 105°C , unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I _{CEx}	Output Leakage Current	$V_{CE} = 50V$ $T_J = 105^\circ\text{C}$, $V_{CE} = 50V$ $T_J = 105^\circ\text{C}$ for ULQ2802A $V_{CE} = 50V$, $V_i = 6V$ for ULQ2804A $V_{CE} = 50V$, $V_i = 1V$			50 100 500 500	μA μA μA μA	1a 1a 1b 1b
V_{CE} (sat)	Collector-emitter Saturation Voltage	$I_C = 100\text{mA}$, $I_B = 250\mu\text{A}$ $I_C = 200\text{mA}$, $I_B = 350\mu\text{A}$ $I_C = 350\text{mA}$, $I_B = 500\mu\text{A}$		0.9 1.1 1.3	1.1 1.3 1.6	V V V	2
I _{i(on)}	Input Current	for ULQ2802A $V_i = 17V$ for ULQ2803A $V_i = 3.85V$ for ULQ2804A $V_i = 5V$ $V_i = 12V$ for ULQ2805A $V_i = 3V$		0.82 0.93 0.35 1 1.5	1.25 1.35 0.5 1.45 2.4	mA mA mA mA mA	3
I _{i(off)}	Input Current	$T_J = 105^\circ\text{C}$, $I_C = 500\mu\text{A}$	50	65		μA	4
V _{i(on)}	Input Voltage	for ULQ2802A $V_{CE} = 2V$, $I_c = 300\text{mA}$ for ULQ2803A $V_{CE} = 2V$, $I_c = 200\text{mA}$ $V_{CE} = 2V$, $I_c = 250\text{mA}$ $V_{CE} = 2V$, $I_c = 300\text{mA}$ for ULQ2804A $V_{CE} = 2V$, $I_c = 125\text{mA}$ $V_{CE} = 2V$, $I_c = 200\text{mA}$ $V_{CE} = 2V$, $I_c = 275\text{mA}$ $V_{CE} = 2V$, $I_c = 350\text{mA}$ for ULQ2805A $V_{CE} = 2V$, $I_c = 350\text{mA}$			13 2.4 2.7 3 5 6 7 8 2.4	V V V V V V V V	5
h_{FE}	DC Forward Current Gain	for ULQ2802A $V_{CE} = 2V$, $I_c = 350\text{mA}$	1000			–	2
C _i	Input Capacitance			15	25 (*)	pF	–
t _{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o		0.25	1 (*)	μs	–
t _{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o		0.25	1 (*)	μs	–
I _R	Clamp Diode Leakage Current	$V_R = 50V$ $T_J = 105^\circ\text{C}$, $V_R = 50V$			50 100	μA μA	6
V _F	Clamp Diode Forward Voltage	$I_F = 350\text{mA}$		1.7	2	V	7

(*) Guaranteed by design

TEST CIRCUITS

Figure 1a.

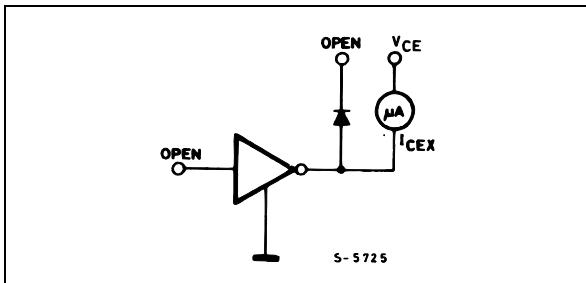


Figure 1b.

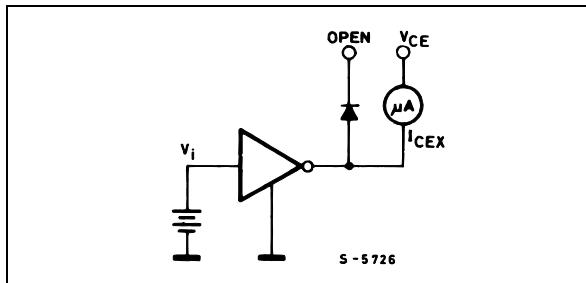


Figure 2.

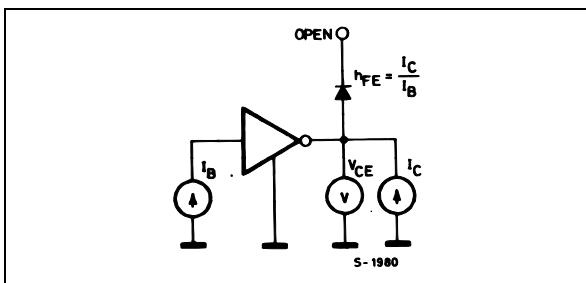


Figure 3.

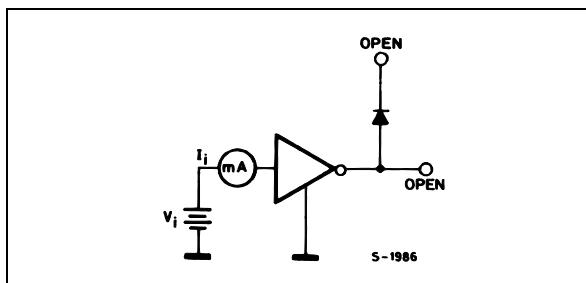


Figure 4.

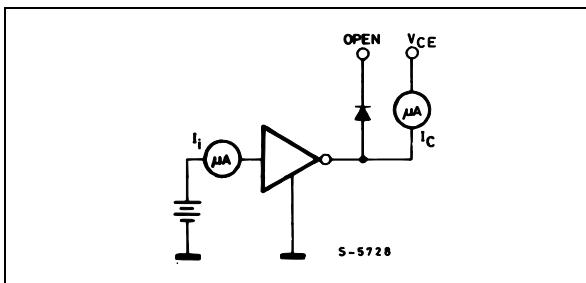


Figure 5.

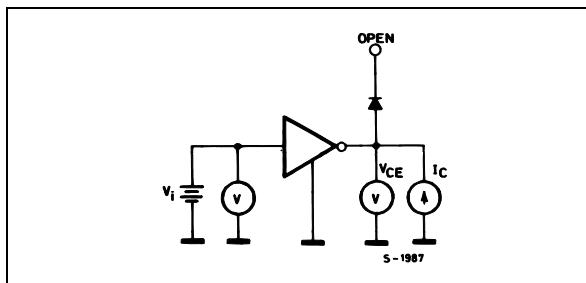


Figure 6.

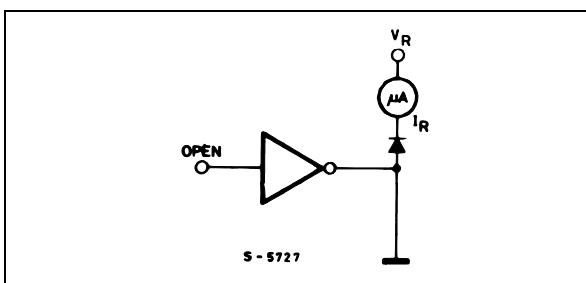


Figure 7.

