# High-precision 10bit 4ch/6ch D/A Converters 

## BU2508FV, BU2507FV

No. 11052 EBT02

## - Description

BU2508FV and BU2507FV ICs are high performance 10bit R-2R-type DACs with 4ch and 6ch outputs, respectively. Each channel incorporates a full swing output-type buffer amplifier with high speed output response characteristics, resulting in a greatly shortened wait time. The ICs also utilize the TTL level input method.

## - Features

1) High performance, multi-channels R-2R-type 10bit D/A converter built-in (BU2508FV: 4 channels, BU2507FV: 6 channels)
2) Full swing output type buffer amplifier incorporated at each output channel
3) The RESET terminal can keep the voltage of all channels within the lower reference voltage range
4) Digital input compatible with TTL levels
5) 14bit 3-line serial data + RESET signal input (address 4bit + data 10bit)
6) Compact package: 14 pins, 0.65 mm pitch (SSOP-B14)

## - Applications

DVDs, CD-Rs, CD-RWs, digital cameras
-Lineup

| Parameter | BU 2507 FV | BU 2508 FV |
| :--- | :---: | :---: |
| Power source voltage range | 4.5 to 5.5 V | 4.5 to 5.5 V |
| Number of channels | 6 ch | 4 ch |
| Differential non linearity error | $\pm 1.0 \mathrm{LSB}$ | $\pm 1.0 \mathrm{LSB}$ |
| Integral non linearity error | $\pm 3.5 \mathrm{LSB}$ | $\pm 3.5 \mathrm{LSB}$ |
| Data transfer frequency | 10 MHz | 10 MHz |
| Package | SSOP-B14 | SSOP-B14 |

- Absolute Maximum Ratings ( $\mathrm{Ta}=25^{\circ} \mathrm{C}$ )

| Parameter | Symbol | Ratings | Unit |
| :--- | :---: | :---: | :---: |
| Power source voltage | VCC | -0.3 to 6.0 | V |
| D/A converter upper standard voltage | VDD | -0.3 to 6.0 | V |
| Input voltage | VIN | -0.3 to 6.0 | V |
| Output voltage | VOUT | -0.3 to 6.0 | V |
| Storage temperature range | Tstg | -55 to 125 | ${ }^{\circ} \mathrm{C}$ |
| Power dissipation | Pd | $350{ }^{*}$ | mW |

Derated at $3.5 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ at $\mathrm{Ta}>25^{\circ} \mathrm{C}$, mounted on a $70 \times 70 \times 1.6 \mathrm{~mm}$ FR4 glass epoxy board (copper foil area less than $3 \%$ ) Note: These products are not robust against radiation

- Recommended Operating Conditions ( $\mathrm{Ta}=25^{\circ} \mathrm{C}$ )

| Parameter | Symbol | Limits | Unit |
| :--- | :---: | :---: | :---: |
| Power supply voltage range | VCC | 4.5 to 5.5 | V |
| Operating temperature range | Topr | -30 to 85 | ${ }^{\circ} \mathrm{C}$ |

-Electrical Characteristics (Unless otherwise specified, VCC=5V, VrefH=5V, VrefL=0V, Ta=25 ${ }^{\circ} \mathrm{C}$ )

| Parameter |  | Symbol | Limits |  |  | Unit | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN. | TYP. | MAX. |  |  |
| <Digital unit> |  |  |  |  |  |  |  |
| Power source current |  |  | ICC | - | 0.85 | 2.8 | mA | At CLK $=10 \mathrm{MHz}, \mathrm{IAO}=0 \mathrm{uA}$ |
| Input leak current |  | IILK | -5 | - | 5 | $\mu \mathrm{A}$ | $\mathrm{VIN}=0$ to VCC |
| Input voltage L |  | VIL | - | - | 0.8 | V | - |
| Input voltage H |  | VIH | 2.0 | - | - | V | - |
| Output voltage L |  | VOL | 0 | - | 0.4 | V | $\mathrm{IOL}=2.5 \mathrm{~mA}$ |
| Output voltage H |  | VOH | 4.6 | - | 5 | V | $\mathrm{IOH}=-2.5 \mathrm{~mA}$ |
| <Analog unit> |  |  |  |  |  |  |  |
| Consumption current |  | IrefH | - | 4.5 | 7.5 | mA | Data condition : at maximum current |
|  |  | - | 2.0 | 3.4 | $m A^{(* 1)}$ |  |  |
| D/A converter upper standard voltage setting range |  |  | VrefH | 3.0 | - | 5 | V | Outputs does not necessarily take a value in standard voltage setting range. Value that output may take is in the buffer amplifier output voltage range (VO). |
| D/A converter lower standard voltage setting range |  | VrefL | 0 | - | 1.5 | V |  |  |
| Buffer amplifier output voltage range |  | VO | 0.1 | - | 4.9 | V | $\mathrm{IO}= \pm 100 \mu \mathrm{~A}$ |  |
|  |  | 0.2 | - | 4.75 | $\mathrm{O}= \pm 1.0 \mathrm{~mA}$ |  |  |  |
| Buffer amplifier output drive range |  |  | 10 | -2 | - | 2 | mA | Upper side saturation voltage $=0.35 \mathrm{~V}$ (on full scale setting, current sourcing ) Lower side saturation voltage $=0.23 \mathrm{~V}$ (on zero scale setting, current sinking ) |
| Precision | Differential non-linearity error | DNL | -1.0 | - | 1.0 | LSB | VrefH $=4.796 \mathrm{~V}$ <br> VrefL $=0.7 \mathrm{~V}$ <br> $\mathrm{VCC}=5.5 \mathrm{~V}(4 \mathrm{mV} / \mathrm{LSB})$ <br> No load (IO = +0mA) |  |
|  | Integral non-linearity error | INL | -3.5 | - | 3.5 |  |  |  |
|  | Zero point error | SZERO | -25 | - | 25 | mV |  |  |
|  | Full scale error | SFULL | -25 | - | 25 |  |  |  |
| Buffer amplifier output impedance |  | RO | - | 5 | 15 | $\Omega$ | - |  |
| Pull-up I/O internal resistance value |  | Rup | 12.5 | 25 | 37.5 | k $\Omega$ | Input voltage 0V (Resistance value changes according to voltage to be impressed.) |  |

*1: Value in the case where $\mathrm{CH} 1 \sim \mathrm{CH} 4$ are set to maximum current (after reset)

- Timing Characteristics (Unless otherwise specified, VCC $=5 \mathrm{~V}$, $\mathrm{VrefH}=5 \mathrm{~V}$, $\mathrm{VrefL}=0 \mathrm{~V}, \mathrm{Ta}=25^{\circ} \mathrm{C}$ )

(note) LD signal is level triggered. When LD input is on H level, internal shift-register state is loaded to DAC control latch. Clock transition during $\mathrm{LD}=\mathrm{H}$ is inhibited.


## -DAC Variable Output Range Function

With the variable output range function, the upper / lower limits of the output voltage as well as the power supply voltage can be set. The upper limit value setting terminal VrefH is used as the power supply terminal, while the lower limit value setting terminal VrefL is used as the GND terminal ( $1 \mathrm{LSB} \fallingdotseq 5 \mathrm{mV}$ ). In the example below, VrefH $=3.5 \mathrm{~V} / \mathrm{VrefL}=1.5 \mathrm{~V}$. Further adjustments can be made in order to achieve greater accuracy ( $1 \mathrm{LSB} \fallingdotseq 2 \mathrm{mV}$ ).


## -Block Diagrams

BU2507FV


BU2508FV


## - Terminal Description

| No | Terminal name | Analog / Digital | I/O | Description of terminal | Equivalent circuit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | VSS | Analog | - | DA converter lower standard voltage (VrefL) input terminal | 6 |
| 2 | AO2 | Analog | O | 10bit D/A output (CH2) | 4 |
| 3 | AO3(TEST1) | Analog | O | 10bit D/A output (CH3) (BU2508FV : test terminal) | 4 |
| 4 | Reset | Digital | I | All ch analog output L fixed | 2 |
| 5 | AO4(TEST2) | Digital | I | 10bit D/A output (CH4) (BU2508FV : test terminal) | 4 |
| 6 | AO5 (AO3) | Analog | 0 | 10bit D/A output (CH5) (BU2508FV : 10bit D/A output (CH3)) | 4 |
| 7 | VDD | Analog | - | DA converter upper standard voltage (VrefH) input terminal | 5 |
| 8 | VCC | - | - | Power source terminal | - |
| 9 | AO6 (AO4) | Analog | 0 | 10bit D/A output (CH6) (BU2508FV : 10bit D/A output (CH4)) | 4 |
| 10 | LD | Digital | I | When High level is input to LD terminal, the value of 14bit shift register is loaded to decoder and D/A output register. | 1 |
| 11 | CLK | Digital | I | Shift clock input terminal. At rise of shift clock, the signal from DI terminal is input to 14bit shift register. | 1 |
| 12 | DI | Digital | 1 | Serial data input terminal. Serial data whose data length is 14bit (address 4bit + data 10bit) is input. | 1 |
| 13 | AO1 | Analog | 0 | 10bit D/A output (CH1) | 4 |
| 14 | GND | - | - | GND terminal | - |

*In the case of BU2508FV, be sure to open TEST1 and TEST2 terminals.

## - Equivalent Circuits


*1: $25 \mathrm{k} \Omega$ at $\mathrm{Vcc}=5.0 \mathrm{~V}$ (changes according to voltage supplied)

## - Command Sending

1) In the case of BU2507FV
(1) Data format [data : LSB first]

(2) Data timing diagram
DACOUT

| D3 | D2 | D1 | D0 | Address selection |
| :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | Inconsequential |
| 0 | 0 | 0 | 1 | Inconsequential |
| 0 | 0 | 1 | 0 | AO1 selection |
| 0 | 0 | 1 | 1 | AO2 selection |
| 0 | 1 | 0 | 0 | Inconsequential |
| 0 | 1 | 0 | 1 | AO3 selection |
| 0 | 1 | 1 | 0 | AO4 selection |
| 0 | 1 | 1 | 1 | Inconsequential |
| 1 | 0 | 0 | 0 | AO5 selection |
| 1 | 0 | 0 | 1 | AO6 selection |
| 1 | 0 | 1 | 0 | Inconsequential |
| 1 | 0 | 1 | 1 | Inconsequential |
| 1 | 1 | 0 | 0 | Inconsequential |
| 1 | 1 | 0 | 1 | Inconsequential |
| 1 | 1 | 1 | 0 | Inconsequential |
| 1 | 1 | 1 | 1 | Inconsequential |


| D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D/A output (VrefH=VDD, VrefL=VSS) |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :--- |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VrefL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | $($ VrefH-VrefL)/1024×1+VrefL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | $($ VrefH-VrefL)/1024×2+VrefL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | $($ VrefH-VrefL)/1024×3+VrefL |
| $:$ | $:$ | $:$ | $:$ | $:$ | $:$ | $:$ | $:$ | $:$ | $:$ |  |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | $($ VrefH-VrefL)/1024×1022+VrefL |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | $($ VrefH-VrefL)/1024×1023+VrefL |

2) In the case of $B U 2508 F V$
(1) Data format [Data: LSB first ]

(2) Data timing diagram


| D3 | D2 | D1 | D0 | Address selection |
| :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | Don't Care |
| 0 | 0 | 0 | 1 | Don't Care |
| 0 | 0 | 1 | 0 | AO1 selection |
| 0 | 0 | 1 | 1 | AO2 selection |
| 0 | 1 | 0 | 0 | Don't Care |
| 0 | 1 | 0 | 1 | Don't Care |
| 0 | 1 | 1 | 0 | Don't Care |
| 0 | 1 | 1 | 1 | Don't Care |
| 1 | 0 | 0 | 0 | AO3 selection |
| 1 | 0 | 0 | 1 | AO4 selection |
| 1 | 0 | 1 | 0 | Don't Care |
| 1 | 0 | 1 | 1 | Don't Care |
| 1 | 1 | 0 | 0 | Don't Care |
| 1 | 1 | 0 | 1 | Don't Care |
| 1 | 1 | 1 | 0 | Don't Care |
| 1 | 1 | 1 | 1 | Don't Care |


| D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D/A output (VrefH=VDD, VrefL=VSS) |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :--- |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VrefL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | $($ VrefH-VrefL)/1024×1+VrefL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | $($ VrefH-VrefL)/1024 $\times 2+$ VrefL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | $($ VrefH-VrefL)/1024 $\times 3+$ VrefL |
| $:$ | $:$ | $:$ | $:$ | $:$ | $:$ | $:$ | $:$ | $:$ | $:$ |  |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | $($ VrefH-VrefL)/1024×1022+VrefL |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | $($ VrefH-VrefL)/1024×1023+VrefL |

## - Electrical Characteristics Curves



Fig. 1 Output voltage linearity $\left(-30^{\circ} \mathrm{C}\right)$


Fig. 4 Differential linearity error ( $-30^{\circ} \mathrm{C}$ )


Fig. 7 Integral linearity error $\left(-30^{\circ} \mathrm{C}\right)$


Fig. 10 Circuit current temperature characteristic


Fig. 2 Output voltage linearity
$\left(25^{\circ} \mathrm{C}\right)$


Fig. 5 Differential linearity error $\left(25^{\circ} \mathrm{C}\right)$


Fig. 8 Integral linearity error $\left(25^{\circ} \mathrm{C}\right)$


Fig. 11 Output load fluctuation characteristic (input code : 1FFh)


Fig. 3 Output voltage linearity $\left(85^{\circ} \mathrm{C}\right)$


Fig. 6 Differential linearity error ( $85^{\circ} \mathrm{C}$ )


Fig. 9 Integral linearity error $\left(85^{\circ} \mathrm{C}\right)$


Fig. 12 Pull-up built in resistance characteristic

## - Standard Example Application Circuit



## - Notes for use

(1) The electrical characteristic and data on graphs for this datasheet, are typically evaluated value, and not guaranteed.
(2) We suppose that application circuits are recommendable, but please make sufficient check for characteristics with the actual application. In case that value of external component for this IC is changed, please check characteristic, not only static but also transient.
(3) About absolute maximum ratings

If operation condition is over the absolute maximum ratings, supply voltage or other operation range, IC will be broken. Please don't apply any voltage or temperature over the absolute maximum ratings. If application have possibilities of become over the absolute maximum ratings, please take safety measures by using fuse and so on. Not to over absolute maximum ratings of IC.
(4) GND voltage

Please keep GND voltage lowest of any other terminal of this IC. Please confirm other terminal voltages is not lower than GND.
(5) Thermal design

Please making a thermal design that allows for a sufficient margin in light of the power dissipation in actual operating condition.
(6) About terminals short and wrong mounting

Please pay full attention to the IC direction and displacement when mounting IC on PCB. If you assemble them by mistake and electrify it, IC might be destroyed. And it is happen to short among IC terminals or terminals and power supply, by foreign substance.
(7) About operation in strong electromagnetic field

If you use it in strong electromagnetic field, please evaluate fully as there is a possibility of malfunction.
(8) Place a bypass capacitor as close as possible between each power supply terminal and ground in order to prevent deterioration of the D/A conversion accuracy due to ripple and noise signals from power supply or GND.
(9) A capacitor should be inserted between the analog output and ground in order to eliminate noise.

A capacitance up to 100 pF is recommended (including the capacitance of the wire).

## - Ordering part number



Part No.


Part No.
2507 2508


Package
FV: SSOP-B14


Packaging and forming specification E2: Embossed tape and reel

SSOP-B14


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