MC14536B

Programmable Timer

The MC14536B programmable timer is a 24−stage binary ripple counter with 16 stages selectable by a binary code. Provisions for an on−chip RC oscillator or an external clock are provided. An on−chip monostable circuit incorporating a pulse−type output has been included. By selecting the appropriate counter stage in conjunction with the appropriate input clock frequency, a variety of timing can be achieved.

Features

- 24 Flip−Flop Stages − Will Count From 2^0 to 2^{24}
- Last 16 Stages Selectable By Four−Bit Select Code
- 8−Bypass Input Allows Bypassing of First Eight Stages
- Set and Reset Inputs
- Clock Inhibit and Oscillator Inhibit Inputs
- On−Chip RC Oscillator Provisions
- On−Chip Monostable Output Provisions
- Clock Conditioning Circuit Permits Operation with Very Long Rise and Fall Times
- Test Mode Allows Fast Test Sequence
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−Power TTL Loads or One Low−Power Schottky TTL Load over the Rated Temperature Range
- Pb−Free Packages are Available*

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	−0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	V_{in}, V_{out}	−0.5 to V_{DD} + 0.5	V
Input or Output Current (DC or Transient) per Pin	I_{in}, I_{out}	±10	mA
Power Dissipation per Package (Note 1)	P_D	500	mW
Ambient Temperature Range	T_A	−55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Lead Temperature, (8−Second Soldering)	T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C from 65°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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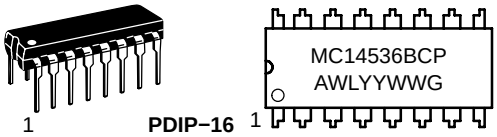
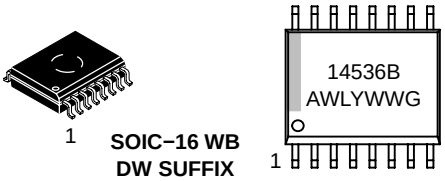
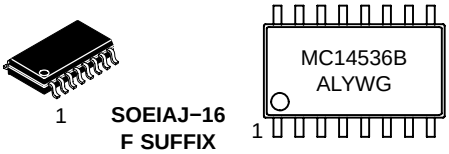
MARKING DIAGRAMS



PDIP−16
P SUFFIX
CASE 648



SOIC−16 WB
DW SUFFIX
CASE 751G



SOEIAJ−16
F SUFFIX
CASE 966

A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

Publication Order Number:
MC14536B/D

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage “0” Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	− − −	0.05 0.05 0.05	− − −	0 0 0	0.05 0.05 0.05	− − −	0.05 0.05 0.05	Vdc
“1” Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	− − −	4.95 9.95 14.95	5.0 10 15	− − −	4.95 9.95 14.95	− − −	Vdc
Input Voltage “0” Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	− − −	1.5 3.0 4.0	− − −	2.25 4.50 6.75	1.5 3.0 4.0	− − −	1.5 3.0 4.0	Vdc
“1” Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	− − −	3.5 7.0 11	2.75 5.50 8.25	− − −	3.5 7.0 11	− − −	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) Pins 4 & 5 (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	− 1.2 − 0.25 − 0.62 − 1.8	− − − −	− 1.0 − 0.25 − 0.5 − 1.5	− 1.7 − 0.36 − 0.9 − 3.5	− − − −	− 0.7 − 0.14 − 0.35 − 1.1	− − − −	mAdc
(V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) Pin 13 (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)		5.0 5.0 10 15	− 3.0 − 0.64 − 1.6 − 4.2	− − − −	− 2.4 − 0.51 − 1.3 − 3.4	− 4.2 − 0.88 − 2.25 − 8.8	− − − −	− 1.7 − 0.36 − 0.9 − 2.4	− − − −	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	− − −	0.51 1.3 3.4	0.88 2.25 8.8	− − −	0.36 0.9 2.4	− − −	mAdc
Input Current	I_{in}	15	−	±0.1	−	±0.00001	±0.1	−	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	−	−	−	−	5.0	7.5	−	−	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	− − −	5.0 10 20	− − −	0.010 0.020 0.030	5.0 10 20	− − −	150 300 600	μAdc
Total Supply Current (Note 3, 4) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (1.50 μA/kHz) f + I_{DD} I_T = (2.30 μA/kHz) f + I_{DD} I_T = (3.55 μA/kHz) f + I_{DD}							μAdc

2. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.003.

SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time (Pin 13)	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
Clock to Q1, 8−Bypass (Pin 6) High	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 1715 ns		5.0	–	1800	3600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 617 ns		10	–	650	1300	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 425 ns		15	–	450	1000	
Clock to Q1, 8−Bypass (Pin 6) Low	t_{PLH},					μs
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 3715 ns	t_{PHL}	5.0	–	3.8	7.6	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 1467 ns		10	–	1.5	3.0	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 1075 ns		15	–	1.1	2.3	
Clock to Q16	t_{PLH},					μs
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 6915 ns	t_{PHL}	5.0	–	7.0	14	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 2967 ns		10	–	3.0	6.0	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 2175 ns		15	–	2.2	4.5	
Reset to Q_n	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 1415 ns		5.0	–	1500	3000	
t_{PHL} = (0.66 ns/pF) C_L + 567 ns		10	–	600	1200	
t_{PHL} = (0.5 ns/pF) C_L + 425 ns		15	–	450	900	
Clock Pulse Width	t_{WH}	5.0	600	300	–	ns
		10	200	100	–	
		15	170	85	–	
Clock Pulse Frequency (50% Duty Cycle)	f_{cl}	5.0	–	1.2	0.4	MHz
		10	–	3.0	1.5	
		15	–	5.0	2.0	
Clock Rise and Fall Time	t_{TLH},	5.0	No Limit			–
	t_{THL}	10				
		15				
Reset Pulse Width	t_{WH}	5.0	1000	500	–	ns
		10	400	200	–	
		15	300	150	–	

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

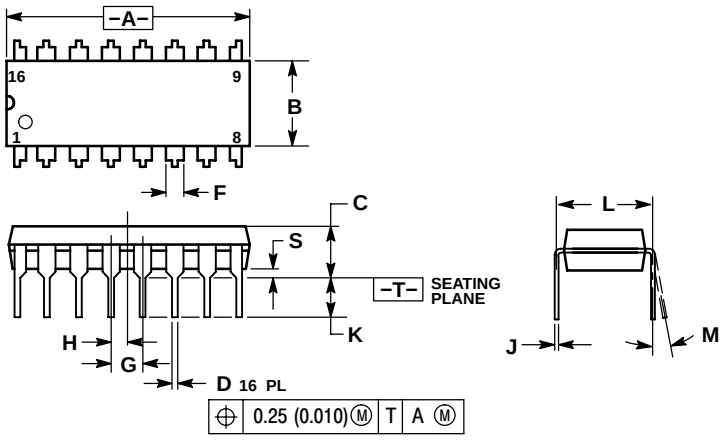
ORDERING INFORMATION

Device	Package	Shipping†
MC14536BCP	PDIP−16	25 Units / Rail
MC14536BCPG	PDIP−16 (Pb−Free)	
MC14536BDW	SOIC−16	47 Units / Rail
MC14536BDWG	SOIC−16 (Pb−Free)	
MC14536BDWR2	SOIC−16	1000 / Tape & Reel
MC14536BDWR2G	SOIC−16 (Pb−Free)	
MC14536BFEL	SOEIAJ−16	2000 / Tape & Reel
MC14536BFELG	SOEIAJ−16 (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

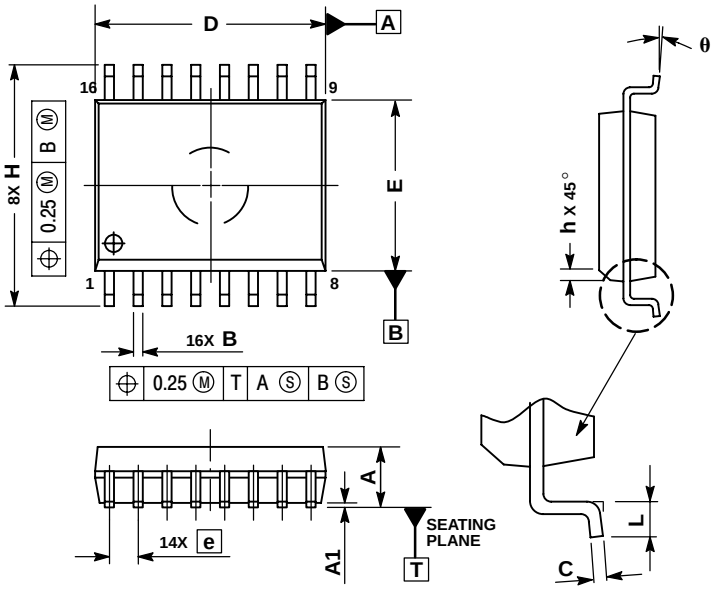
PDIP−16
CASE 648−08
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

SOIC−16WB
CASE 751G−03
ISSUE C



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
q	0 °	7 °