M48T08
M48T08Y, M48T18

5 V, 64 Kbit (8 Kb x 8) TIMEKEEPER® SRAM

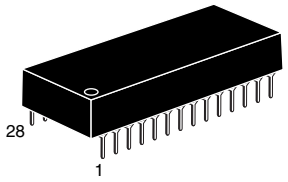
Features

- Integrated ultra low power SRAM, real-time clock, power-fail control circuit, and battery
- BYTEWIDE™ RAM-like clock access
- BCD coded year, month, day, date, hours, minutes, and seconds
- Typical clock accuracy of ±1 minute a month, at 25°C
- Automatic power-fail chip deselect and write protection
- Write protect

  V_{PFD} = Power-fail deselect voltage):
  - M48T08: V_{CC} = 4.75 to 5.5 V

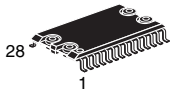
    4.5 V ≤ V_{PFD} ≤ 4.75 V
  - M48T18/T08Y: V_{CC} = 4.5 to 5.5 V

    4.2 V ≤ V_{PFD} ≤ 4.5 V
- Software controlled clock calibration for high accuracy applications
- Self-contained battery and crystal in the CAPHAT™ DIP package
- Packaging includes a 28-lead SOIC and SNAPHAT® top (to be ordered separately)
- SOIC package provides direct connection for a snaphat top which contains the battery and crystal
- Pin and function compatible with DS1643 and JEDEC standard 8 K x 8 SRAMs
- RoHS compliant
  - Lead-free second level interconnect



PCDIP28 (PC)
battery/crystal
CAPHAT™

SNAPHAT® (SH)
battery/crystal



SOH28 (MH)

1 Description

The M48T08/18/08Y TIMEKEEPER® RAM is an 8 K x 8 non-volatile static RAM and real time clock which is pin and functional compatible with the DS1643. The monolithic chip is available in two special packages to provide a highly integrated battery backed-up memory and real time clock solution.

The M48T08/18/08Y is a non-volatile pin and function equivalent to any JEDEC standard 8 K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special WRITE timing or limitations on the number of WRITEs that can be performed.

The 28-pin, 600 mil DIP CAPHAT™ houses the M48T08/18/08Y silicon with a quartz crystal and a long-life lithium button cell in a single package.

The 28-pin, 330 mil SOIC provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT® housing containing the battery and crystal. The unique design allows the SNAPHAT battery package to be mounted on top of the SOIC package after the completion of the surface mount process. Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SOIC and battery/crystal packages are shipped separately in plastic anti-static tubes or in tape & reel form. For the 28-lead SOIC, the battery/crystal package (e.g., SNAPHAT) part number is “M4T28-BR12SH” or “M4T32-BR12SH” (see *Table 17 on page 28*).

Figure 1. Logic diagram

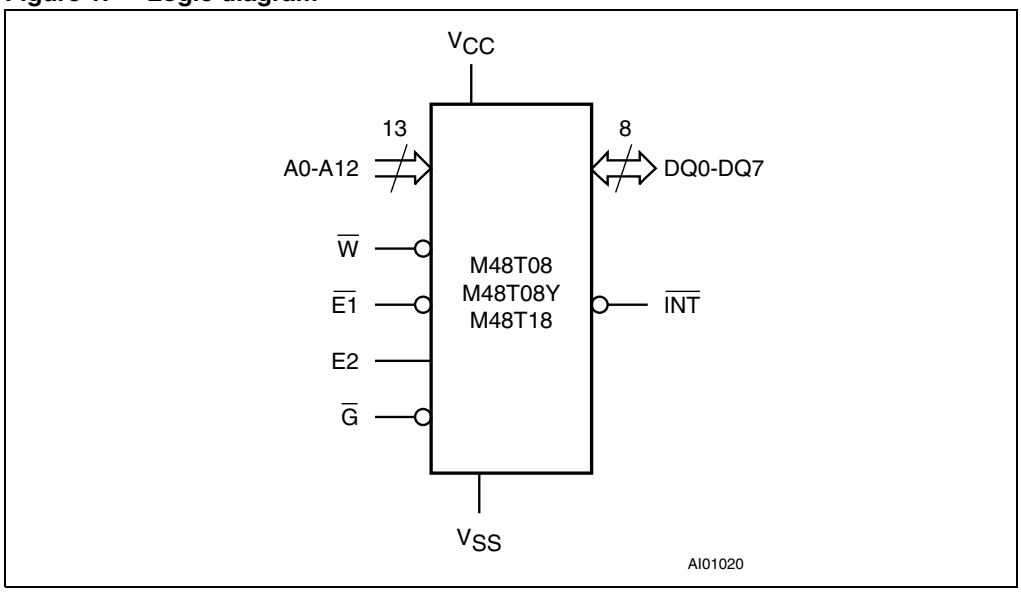


Table 3. Read mode AC characteristics

Symbol	Parameter[1]	M48T08/M48T18/T08Y				Unit
		–100/–10 (T08Y)		–150/–15 (T08Y)		
		Min	Max	Min	Max	
t_{AVAV}	READ cycle time	100		150		ns
t_{AVQV}	Address valid to output valid		100		150	ns
t_{E1LQV}	Chip enable 1 low to output valid		100		150	ns
t_{E2HQV}	Chip enable 2 high to output valid		100		150	ns
t_{GLQV}	Output enable low to output valid		50		75	ns
t_{E1LQX}	Chip enable 1 low to output transition	10		10		ns
t_{E2HQX}	Chip enable 2 high to output transition	10		10		ns
t_{GLQX}	Output enable low to output transition	5		5		ns
t_{E1HQZ}	Chip enable 1 high to output Hi-Z		50		75	ns
t_{E2LQZ}	Chip enable 2 low to output Hi-Z		50		75	ns
t_{GHQZ}	Output enable high to output Hi-Z		40		60	ns
t_{AXQX}	Address transition to output transition	5		5		ns

Note: Valid for ambient operating temperature: T_A = 0 to 70°C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).

2.2 Write mode

The M48T08/18/08Y is in the WRITE mode whenever $\overline{W}$, $\overline{E1}$, and E2 are active. The start of a WRITE is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E1}$, or the rising edge of E2. A WRITE is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E1}$, or the falling edge of E2. The addresses must be held valid throughout the cycle. $\overline{E1}$ or $\overline{W}$ must return high or E2 low for a minimum of t_{E1HAX} or t_{E2LAX} from chip enable or t_{WHAX} from WRITE enable prior to the initiation of another READ or WRITE cycle. Data-in must be valid t_{DVWH} prior to the end of WRITE and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during WRITE cycles to avoid bus contention; however, if the output bus has been activated by a low on $\overline{E1}$ and $\overline{G}$ and a high on E2, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

Table 4. Write mode AC characteristics

Symbol	Parameter[1]	M48T08/M48T18/T08Y				Unit
		–100/–10 (T08Y)		–150/–15 (T08Y)		
		Min	Max	Min	Max	
t_{AVAV}	WRITE cycle time	100		150		ns
t_{AVWL}	Address valid to WRITE enable low	0		0		ns
t_{AVE1L}	Address valid to chip enable 1 low	0		0		ns
t_{AVE2H}	Address valid to chip enable 2 high	0		0		ns
t_{WLWH}	WRITE enable pulse width	80		100		ns
t_{E1LE1H}	Chip enable 1 low to chip enable 1 high	80		130		ns
t_{E2HE2L}	Chip enable 2 high to chip enable 2 low	80		130		ns
t_{WHAX}	WRITE enable high to address transition	10		10		ns
t_{E1HAX}	Chip enable 1 high to address transition	10		10		ns
t_{E2LAX}	Chip enable 2 low to address transition	10		10		ns
t_{DVWH}	Input valid to WRITE enable high	50		70		ns
t_{DVE1H}	Input valid to chip enable 1 high	50		70		ns
t_{DVE2L}	Input valid to chip enable 2 low	50		70		ns
t_{WHDX}	WRITE enable high to input transition	5		5		ns
t_{E1HDX}	Chip enable 1 high to input transition	5		5		ns
t_{E2LDX}	Chip enable 2 low to input transition	5		5		ns
t_{WLQZ}	WRITE enable low to output Hi-Z		50		70	ns
t_{AVWH}	Address valid to WRITE enable high	80		130		ns
t_{AVE1H}	Address valid to chip enable 1 high	80		130		ns
t_{AVE2L}	Address valid to chip enable 2 low	80		130		ns
t_{WHQX}	WRITE enable high to output transition	10		10		ns

1. Valid for ambient operating temperature: T_A = 0 to 70°C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).

2.3 Data retention mode

With valid V_{CC} applied, the M48T08/18/08Y operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. All outputs become high impedance, and all inputs are treated as “Don't care.”

Note: A power failure during a WRITE cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48T08/18/08Y may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

4 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 6. Absolute maximum ratings

Symbol	Parameter	Value	Unit
T_A	Ambient operating temperature	0 to 70	°C
T_{STG}	Storage temperature (V_{CC} off, oscillator off)	–40 to 85	°C
T_{SLD}(1)(2)(3)	Lead solder temperature for 10 seconds	260	°C
V_{IO}	Input or output voltages	–0.3 to 7	V
V_{CC}	Supply voltage	–0.3 to 7	V
I_O	Output current	20	mA
P_D	Power dissipation	1	W

1. For DIP package: soldering temperature not to exceed 260°C for 10 seconds (total thermal budget not to exceed 150°C for longer than 30 seconds).
2. For SO package, standard (SnPb) lead finish: reflow at peak temperature of 225°C (the time above 220°C must not exceed 20 seconds).
3. For SO package, lead-free (Pb-free) lead finish: reflow at peak temperature of 260°C (the time above 255°C must not exceed 30 seconds).

Caution: *Negative undershoots below –0.3 V are not allowed on any pin while in the battery backup mode.*

Caution: *Do NOT wave solder SOIC to avoid damaging SNAPHAT® sockets.*

5 DC and AC parameters

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC characteristic tables are derived from tests performed under the measurement conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 7. Operating and AC measurement conditions

Parameter	M48T08	M48T18/T08Y	Unit
Supply voltage (V_{CC})	4.75 to 5.5	4.5 to 5.5	V
Ambient operating temperature (T_A)	0 to 70	0 to 70	°C
Load capacitance (C_L)	100	100	pF
Input rise and fall times	≤ 5	≤ 5	ns
Input pulse voltages	0 to 3	0 to 3	V
Input and output timing ref. voltages	1.5	1.5	V

Note: Output Hi-Z is defined as the point where data is no longer driven.

Figure 11. AC testing load circuit

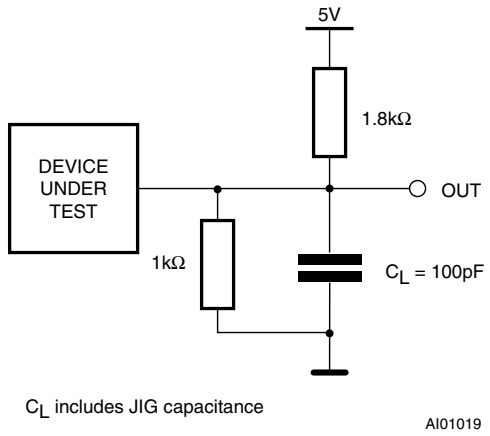


Table 8. Capacitance

Symbol	Parameter[1][2]	Min	Max	Unit
C_{IN}	Input capacitance		10	pF
C_{IO}[3]	Input / output capacitance		10	pF

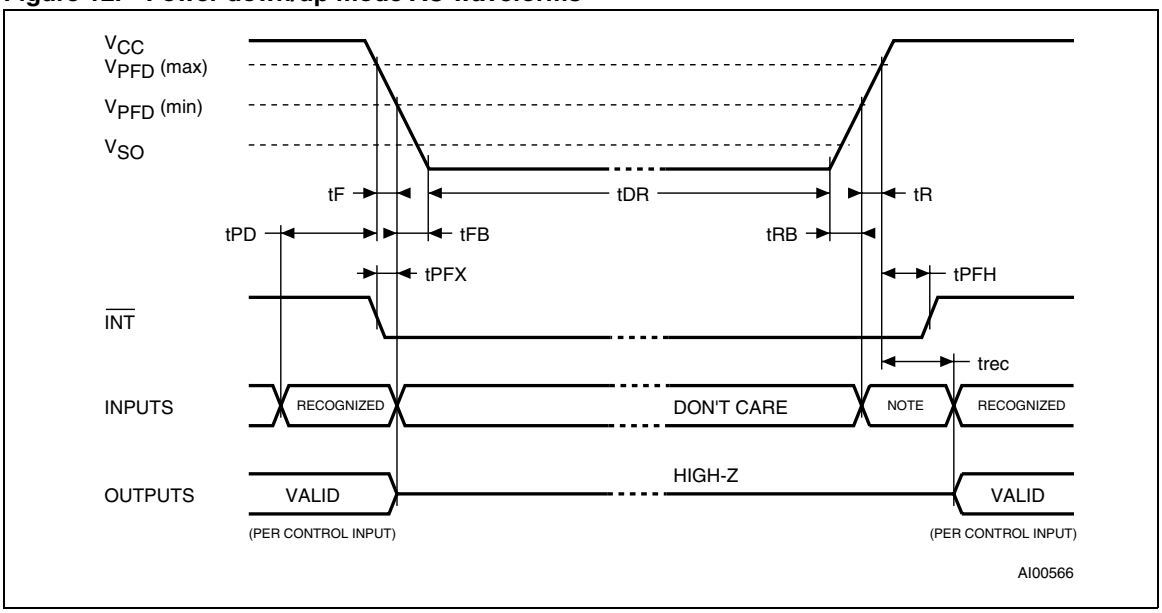
1. Effective capacitance measured with power supply at 5 V; sampled only, not 100% tested.
2. At 25°C, f = 1 MHz.
3. Outputs deselected.

Table 9. DC characteristics

Symbol	Parameter	Test condition(1)	M48T08/M48T18/T08Y		Unit
			Min	Max	
I_{LI}	Input leakage current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}(2)	Output leakage current	$0V \le V_{OUT} \le V_{CC}$		±1	µA
I_{CC}	Supply current	Outputs open		80	mA
I_{CC1}(3)	Supply current (standby) TTL	$\overline{E1} = V_{IH}$, $E2 = V_{IL}$		3	mA
I_{CC2}(3)	Supply current (standby) CMOS	$\overline{E1} = V_{CC} - 0.2V$, $E2 = V_{SS} + 0.2V$		3	mA
V_{IL}	Input low voltage		–0.3	0.8	V
V_{IH}	Input high voltage		2.2	$V_{CC} + 0.3$	V
V_{OL}	Output low voltage	$I_{OL} = 2.1$ mA		0.4	V
	Output low voltage ($\overline{INT}$)(4)	$I_{OL} = 0.5$ mA		0.4	V
V_{OH}	Output high voltage	$I_{OH} = –1$ mA	2.4		V

1. Valid for ambient operating temperature: T_A = 0 to 70°C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).
2. Outputs deselected.
3. Measured with control bits set as follows: R = '1'; W, ST, FT = '0.'
4. The $\overline{INT}$ pin is open drain.

Figure 12. Power down/up mode AC waveforms



Note: Inputs may or may not be recognized at this time. Caution should be taken to keep $\overline{E1}$ high or E2 low as V_{CC} rises past V_{PFD} (min). Some systems may perform inadvertent WRITE cycles after V_{CC} rises above V_{PFD} (min) but before normal system operations begin. Even though a power on reset is being applied to the processor, a reset condition may not occur until after the system clock is running.

Table 10. Power down/up AC characteristics

Symbol	Parameter[1]	Min	Max	Unit
t_{PD}	$\overline{E1}$ or $\overline{W}$ at V_{IH} or E2 at V_{IL} before power-down	0		µs
t_F[2]	V_{PFD} (max) to V_{PFD} (min) V_{CC} fall time	300		µs
t_{FB}[3]	V_{PFD} (min) to V_{SS} V_{CC} fall time	10		µs
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} rise time	0		µs
t_{RB}	V_{SS} to V_{PFD} (min) V_{CC} rise time	1		µs
t_{rec}	$\overline{E1}$ or $\overline{W}$ at V_{IH} or E2 at V_{IL} before power-up	1		ms
t_{PFX}	$\overline{INT}$ low to auto deselect	10	40	µs
t_{PFH}	V_{PFD} (max) to $\overline{INT}$ high		120	µs

1. Valid for ambient operating temperature: T_A = 0 to 70°C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).
2. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
3. V_{PFD} (min) to V_{SS} fall time of less than t_{FB} may cause corruption of RAM data.

Table 11. Power down/up trip points DC characteristics

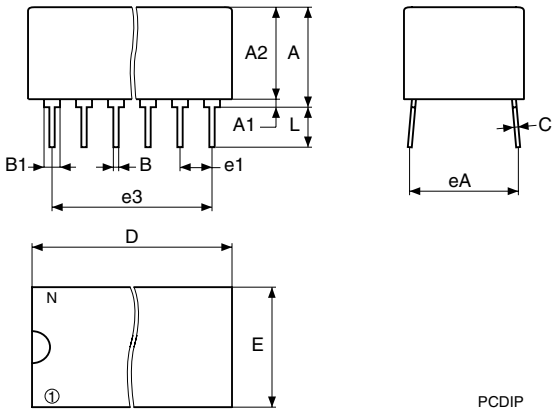
Symbol	Parameter[1][2]		Min	Typ	Max	Unit
V_{PFD}	Power-fail deselect voltage	M48T08	4.5	4.6	4.75	V
		M48T18/T08Y	4.2	4.3	4.5	V
V_{SO}	Battery backup switchover voltage			3.0		V
t_{DR}	Expected data retention time		10[3]			Years

1. All voltages referenced to V_{SS}.
2. Valid for ambient operating temperature: T_A = 0 to 70°C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).
3. At 55°C, V_{CC} = 0 V; t_{DR} = 8.5 years (typ) at 70°C. Requires use of M4T32-BR12SH SNAPHAT® top when using the SOH28 package.

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 13. PCDIP28 – 28-pin plastic DIP, battery CAPHAT™, package outline



Note: Drawing is not to scale.

Table 12. PCDIP28 – 28-pin plastic DIP, battery CAPHAT™, package mech. data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.38	8.89		0.330	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		39.37	39.88		1.550	1.570
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3		29.72	36.32		1.170	1.430
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N	28			28		

7 Part numbering

Table 16. Ordering information scheme

Example: M48T 18 –100 PC 1 E

Device type

M48T

Supply voltage and write protect voltage

08[1] = V_{CC} = 4.75 to 5.5 V; V_{PFD} = 4.5 to 4.75 V

18/08Y = V_{CC} = 4.5 to 5.5 V; V_{PFD} = 4.2 to 4.5 V

Speed

–100 = 100 ns

–150 = 150 ns

–10 = 100 ns (M48T08Y)

Package

PC[1] = PCDIP28

MH[2] = SOH28

Temperature range

1 = 0 to 70°C

Shipping method

For SOH28:

blank = Tubes (not for new design - use E)

E = ECOPACK® package, tubes

F = ECOPACK® package, tape & reel

TR = Tape & reel (not for new design - use F)

For PCDIP28:

blank = ECOPACK® package, tubes

1. The M48T08/18 part is offered with the PCDIP28 (e.g., CAPHAT™) package only.
2. The SOIC package (SOH28) requires the SNAPHAT® battery/crystal package which is ordered separately under the part number “M4TXX-BR12SH” in plastic tube or “M4TXX-BR12SHTR” in tape & reel form (see *Table 17*). The M48T08Y part is offered in the SOH28 (SNAPHAT) package only.

Caution: Do not place the SNAPHAT® battery package “M4TXX-BR12SH” in conductive foam as it will drain the lithium button-cell battery.

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.