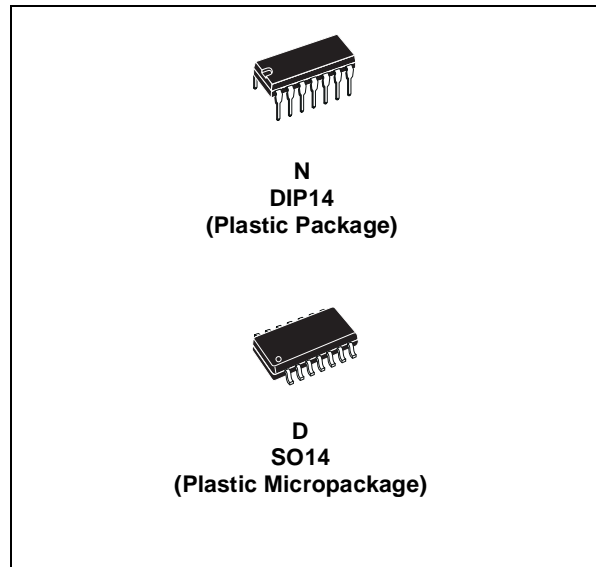


**WIDE BANDWIDTH
QUAD J-FET OPERATIONAL AMPLIFIERS**

- LOW POWER CONSUMPTION
- WIDE COMMON-MODE (UP TO V_{CC}^+) AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J-FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : $16V/\mu s$ (typ)



DESCRIPTION

These circuits are high speed J-FET input quad operational amplifiers incorporating well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

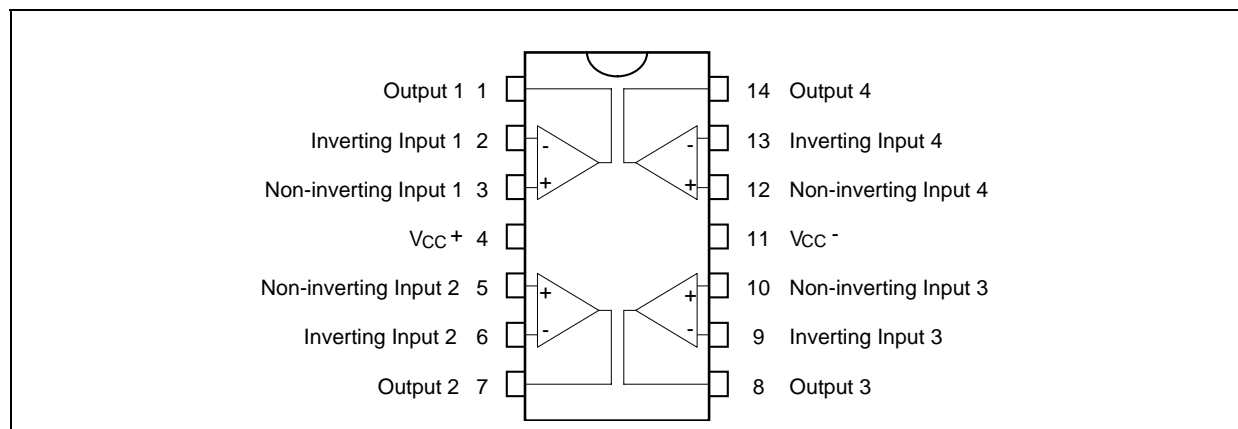
ORDER CODE

Part Number	Temperature Range	Package	
		N	D
LF147	-55°C, +125°C	•	•
LF247	-40°C, +105°C	•	•
LF347	0°C, +70°C	•	•

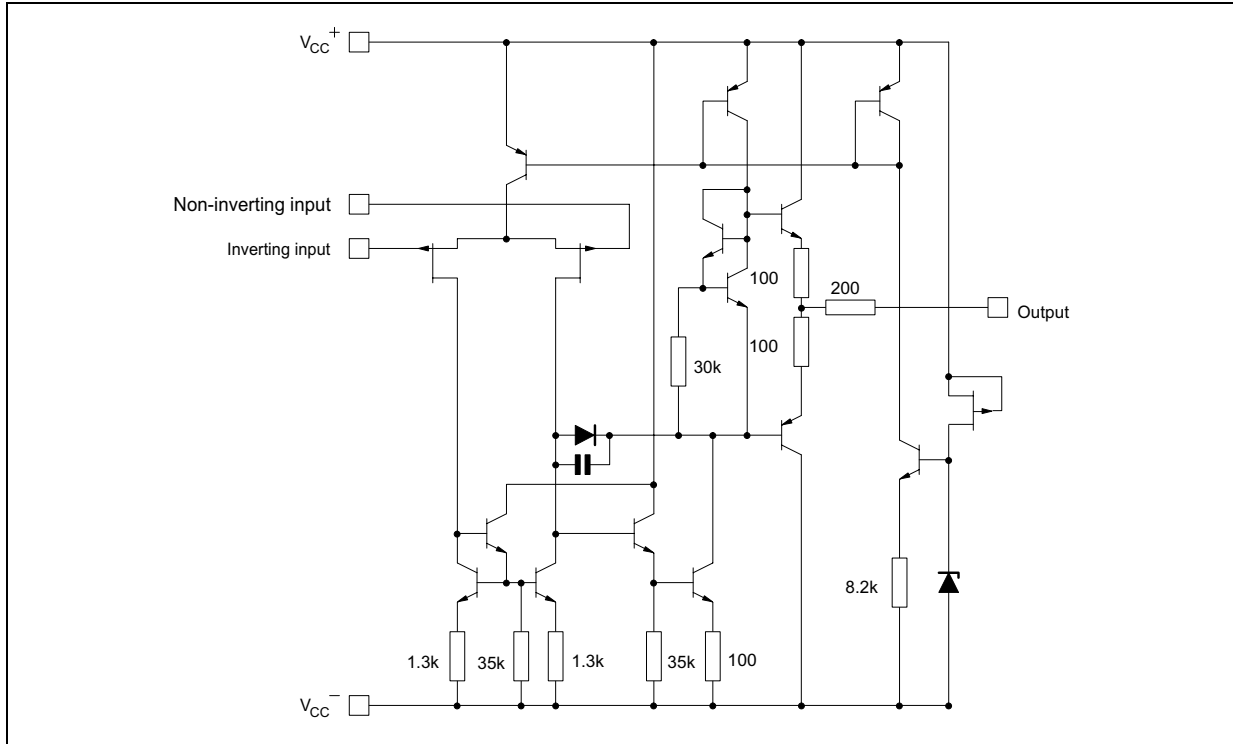
Example : LF347IN

N = Dual in Line Package (DIP)
D = Small Outline Package (SO) - also available in Tape & Reel (DT)

PIN CONNECTIONS (top view)



SCHEMATIC DIAGRAM (each amplifier)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LF147	LF247	LF347	Unit
V_{CC}	Supply voltage - note ¹⁾	±18			V
V_i	Input Voltage - note ²⁾	±15			V
V_{id}	Differential Input Voltage - note ³⁾	±30			V
P_{tot}	Power Dissipation	680			mW
	Output Short-circuit Duration - note ⁴⁾	Infinite			
T_{oper}	Operating Free-air Temperature Range	-55 to +125	-40 to +105	0 to +70	°C
T_{stg}	Storage Temperature Range	-65 to +150			°C

1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-} .
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
3. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded

ELECTRICAL CHARACTERISTICS

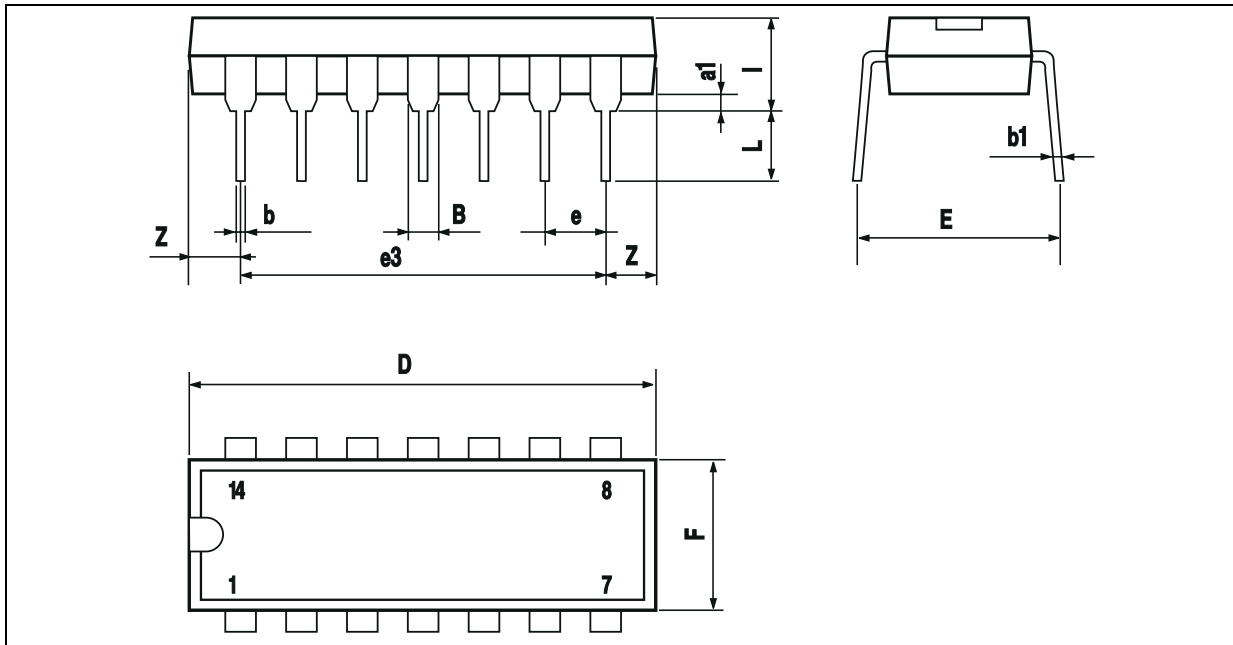
$V_{CC} = \pm 15V$, $T_{amb} = +25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage ($R_S = 10k\Omega$) $T_{amb} = 25^{\circ}C$ $T_{min} \leq T_{amb} \leq T_{max}$		3	10 13	mV
DV_{io}	Input Offset Voltage Drift		10		$\mu V/^{\circ}C$
I_{io}	Input Offset Current - note 1) $T_{amb} = 25^{\circ}C$ $T_{min} \leq T_{amb} \leq T_{max}$		5	100 4	pA nA
I_{ib}	Input Bias Current - note 1 $T_{amb} = 25^{\circ}C$ $T_{min} \leq T_{amb} \leq T_{max}$		20	200 20	pA nA
A_{vd}	Large Signal Voltage Gain ($R_L = 2k\Omega$, $V_O = \pm 10V$), $T_{amb} = 25^{\circ}C$ $T_{min} \leq T_{amb} \leq T_{max}$	50 25	200		V/mV
SVR	Supply Voltage Rejection Ratio ($R_S = 10k\Omega$) $T_{amb} = 25^{\circ}C$ $T_{min} \leq T_{amb} \leq T_{max}$	80 80	86		dB
I_{CC}	Supply Current, Per Amp, no Load $T_{amb} = 25^{\circ}C$ $T_{min} \leq T_{amb} \leq T_{max}$		1.4	2.7 2.7	mA
V_{icm}	Input Common Mode Voltage Range	± 11	+15 -12		V
CMR	Common Mode Rejection Ratio ($R_S = 10k\Omega$) $T_{amb} = 25^{\circ}C$ $T_{min} \leq T_{amb} \leq T_{max}$	70 70	86		dB
I_{OS}	Output Short-Circuit Current $T_{amb} = 25^{\circ}C$ $T_{min} \leq T_{amb} \leq T_{max}$	10 10	40	60 60	mA
$\pm V_{opp}$	Output Voltage Swing $T_{amb} = 25^{\circ}C$ $T_{min} \leq T_{amb} \leq T_{max}$	$R_L = 2k\Omega$ 10 $R_L = 10k\Omega$ 12 $R_L = 2k\Omega$ 10 $R_L = 10k\Omega$ 12	12 13.5		V
SR	Slew Rate $V_i = 10V$, $R_L = 2k\Omega$, $C_L = 100pF$, $T_{amb} = 25^{\circ}C$, unity gain	12	16		V/ μs
t_r	Rise Time $V_i = 20mV$, $R_L = 2k\Omega$, $C_L = 100pF$, $T_{amb} = 25^{\circ}C$, unity gain		0.1		μs
K_{ov}	Overshoot $V_i = 20mV$, $R_L = 2k\Omega$, $C_L = 100pF$, $T_{amb} = 25^{\circ}C$, unity gain		10		%
GBP	Gain Bandwidth Product $f = 100kHz$, $T_{amb} = 25^{\circ}C$, $V_{in} = 10mV$, $R_L = 2k\Omega$, $C_L = 100pF$	2.5	4		MHz
R_i	Input Resistance		10^{12}		Ω
THD	Total Harmonic Distortion $f = 1kHz$, $A_v = 20dB$, $R_L = 2k\Omega$, $C_L = 100pF$ $T_{amb} = 25^{\circ}C$, $V_O = 2V_{pp}$		0.01		%
e_n	Equivalent Input Noise Voltage ($R_S = 100\Omega$, $f = 1kHz$)		15		$\frac{nV}{\sqrt{Hz}}$
ϕ_m	Phase Margin		45		Degrees
V_{O1}/V_{O2}	Channel Separation ($A_v = 100$)		120		dB

1. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature.



PACKAGE MECHANICAL DATA
14 PINS - PLASTIC DIP



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
i			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100