MC34071,2,4,A
MC33071,2,4,A, NCV33074A

Single Supply 3.0 V to 44 V Operational Amplifiers

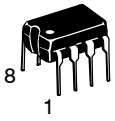
ON Semiconductor®

Quality bipolar fabrication with innovative design concepts are employed for the MC33071/72/74, MC34071/72/74 series of monolithic operational amplifiers. This series of operational amplifiers offer 4.5 MHz of gain bandwidth product, 13 V/μs slew rate and fast settling time without the use of JFET device technology. Although this series can be operated from split supplies, it is particularly suited for single supply operation, since the common mode input voltage range includes ground potential (V_{EE}). With a Darlington input stage, this series exhibits high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source/sink AC frequency response.

The MC33071/72/74, MC34071/72/74 series of devices are available in standard or prime performance (A Suffix) grades and are specified over the commercial, industrial/vehicular or military temperature ranges. The complete series of single, dual and quad operational amplifiers are available in plastic DIP, SOIC and TSSOP surface mount packages.

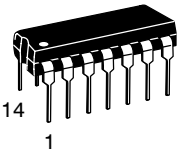
Features

- Wide Bandwidth: 4.5 MHz
- High Slew Rate: 13 V/μs
- Fast Settling Time: 1.1 μs to 0.1%
- Wide Single Supply Operation: 3.0 V to 44 V
- Wide Input Common Mode Voltage Range: Includes Ground (V_{EE})
- Low Input Offset Voltage: 3.0 mV Maximum (A Suffix)
- Large Output Voltage Swing: −14.7 V to +14 V (with ±15 V Supplies)
- Large Capacitance Drive Capability: 0 pF to 10,000 pF
- Low Total Harmonic Distortion: 0.02%
- Excellent Phase Margin: 60°
- Excellent Gain Margin: 12 dB
- Output Short Circuit Protection
- ESD Diodes/Clamps Provide Input Protection for Dual and Quad
- Pb−Free Packages are Available

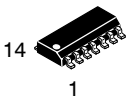


PDIP−8
P SUFFIX
CASE 626

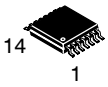
SOIC−8
D SUFFIX
CASE 751



PDIP−14
P SUFFIX
CASE 646



SOIC−14
D SUFFIX
CASE 751A



TSSOP−14
DTB SUFFIX
CASE 948G

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 17 of this data sheet.

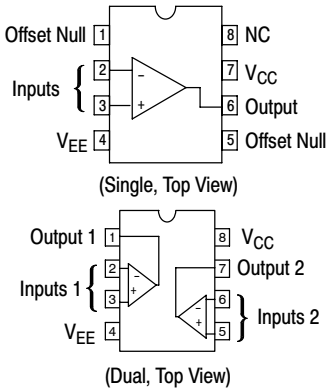
DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 20 of this data sheet.

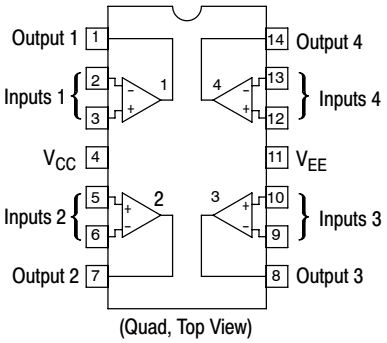
Publication Order Number:
MC34071/D

PIN CONNECTIONS

CASE 626/CASE 751



CASE 646/CASE 751A/CASE 948G



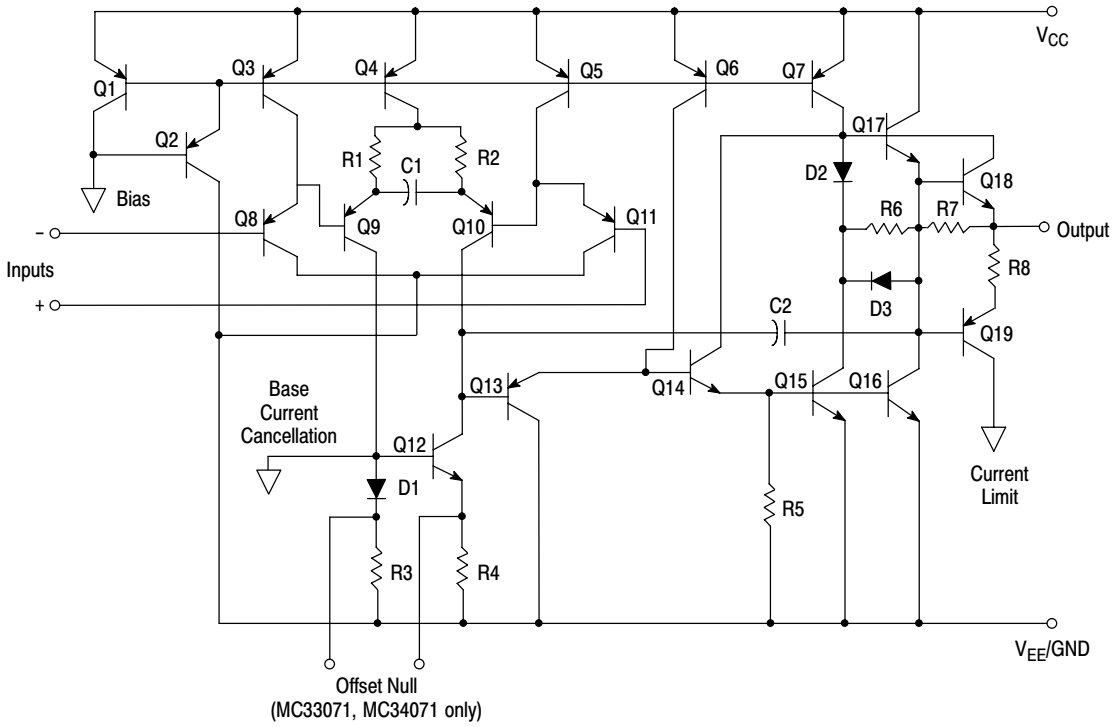


Figure 1. Representative Schematic Diagram
(Each Amplifier)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{EE} to V_{CC})	V_S	+44	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	Sec
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	−60 to +150	°C

1. Either or both input voltages should not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 2).

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, R_L = connected to ground, unless otherwise noted. See Note 3 for $T_A = T_{low}$ to T_{high})

Characteristics	Symbol	A Suffix			Non−Suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S = 100 Ω, V_{CM} = 0 V, V_O = 0 V) V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C V_{CC} = +5.0 V, V_{EE} = 0 V, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, $T_A = T_{low}$ to T_{high}	V_{IO}	– – –	0.5 0.5 –	3.0 3.0 5.0	– – –	1.0 1.5 –	5.0 5.0 7.0	mV
Average Temperature Coefficient of Input Offset Voltage R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V, $T_A = T_{low}$ to T_{high}	$\Delta V_{IO}/\Delta T$	–	10	–	–	10	–	μV/°C
Input Bias Current (V_{CM} = 0 V, V_O = 0 V) T_A = +25°C $T_A = T_{low}$ to T_{high}	I_{IB}	– –	100 –	500 700	– –	100 –	500 700	nA
Input Offset Current (V_{CM} = 0 V, V_O = 0V) T_A = +25°C $T_A = T_{low}$ to T_{high}	I_{IO}	– –	6.0 –	50 300	– –	6.0 –	75 300	nA
Input Common Mode Voltage Range T_A = +25°C $T_A = T_{low}$ to T_{high}	V_{ICR}	V_{EE} to (V_{CC} −1.8) V_{EE} to (V_{CC} −2.2)			V_{EE} to (V_{CC} −1.8) V_{EE} to (V_{CC} −2.2)			V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ) T_A = +25°C $T_A = T_{low}$ to T_{high}	A_{VOL}	50 25	100 –	– –	25 20	100 –	– –	V/mV
Output Voltage Swing (V_{ID} = ±1.0 V) V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 2.0 kΩ, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 kΩ, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, R_L = 2.0 kΩ, $T_A = T_{low}$ to T_{high}	V_{OH}	3.7 13.6 13.4	4.0 14 –	– – –	3.7 13.6 13.4	4.0 14 –	– – –	V
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 2.0 kΩ, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 kΩ, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, R_L = 2.0 kΩ, $T_A = T_{low}$ to T_{high}	V_{OL}	– – –	0.1 −14.7 –	0.3 −14.3 −13.5	– – –	0.1 −14.7 –	0.3 −14.3 −13.5	V
Output Short Circuit Current (V_{ID} = 1.0 V, V_O = 0 V, T_A = 25°C) Source Sink	I_{SC}	10 20	30 30	– –	10 20	30 30	– –	mA
Common Mode Rejection $R_S \le$ 10 kΩ, $V_{CM} = V_{ICR}$, T_A = 25°C	CMR	80	97	–	70	97	–	dB
Power Supply Rejection (R_S = 100 Ω) V_{CC}/V_{EE} = +16.5 V/−16.5 V to +13.5 V/−13.5 V, T_A = 25°C	PSR	80	97	–	70	97	–	dB
Power Supply Current (Per Amplifier, No Load) V_{CC} = +5.0 V, V_{EE} = 0 V, V_O = +2.5 V, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, V_O = 0 V, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, V_O = 0 V, $T_A = T_{low}$ to T_{high}	I_D	– – –	1.6 1.9 –	2.0 2.5 2.8	– – –	1.6 1.9 –	2.0 2.5 2.8	mA

3. T_{low} = −40°C for MC33071, 2, 4, /A
= 0°C for MC34071, 2, 4, /A
= −40°C for MC34072, 4/V
T_{high} = +85°C for MC33071, 2, 4, /A
= +70°C for MC34071, 2, 4, /A
= +125°C for MC34072, 4/V

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, R_L = connected to ground. T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	A Suffix			Non−Suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 kΩ, C_L = 500 pF) A_V = +1.0 A_V = −1.0	SR	 8.0 −	 10 13	 − −	 8.0 −	 10 13	 − −	V/μs
Setting Time (10 V Step, A_V = −1.0) To 0.1% (+1/2 LSB of 9−Bits) To 0.01% (+1/2 LSB of 12−Bits)	t_s	 − −	 1.1 2.2	 − −	 − −	 1.1 2.2	 − −	μs
Gain Bandwidth Product (f = 100 kHz)	GBW	3.5	4.5	−	3.5	4.5	−	MHz
Power Bandwidth A_V = +1.0, R_L = 2.0 kΩ, V_O = 20 V_{pp}, THD = 5.0%	BW	−	160	−	−	160	−	kHz
Phase margin R_L = 2.0 kΩ R_L = 2.0 kΩ, C_L = 300 pF	f_m	 − −	 60 40	 − −	 − −	 60 40	 − −	Deg
Gain Margin R_L = 2.0 kΩ R_L = 2.0 kΩ, C_L = 300 pF	A_m	 − −	 12 4.0	 − −	 − −	 12 4.0	 − −	dB
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1.0 kHz	e_n	−	32	−	−	32	−	nV/√Hz
Equivalent Input Noise Current f = 1.0 kHz	i_n	−	0.22	−	−	0.22	−	pA/√Hz
Differential Input Resistance V_{CM} = 0 V	R_{in}	−	150	−	−	150	−	MΩ
Differential Input Capacitance V_{CM} = 0 V	C_{in}	−	2.5	−	−	2.5	−	pF
Total Harmonic Distortion A_V = +10, R_L = 2.0 kΩ, 2.0 $V_{pp} \le V_O \le$ 20 V_{pp}, f = 10 kHz	THD	−	0.02	−	−	0.02	−	%
Channel Separation (f = 10 kHz)	−	−	120	−	−	120	−	dB
Open Loop Output Impedance (f = 1.0 MHz)	$\|Z_O\|$	−	30	−	−	30	−	W

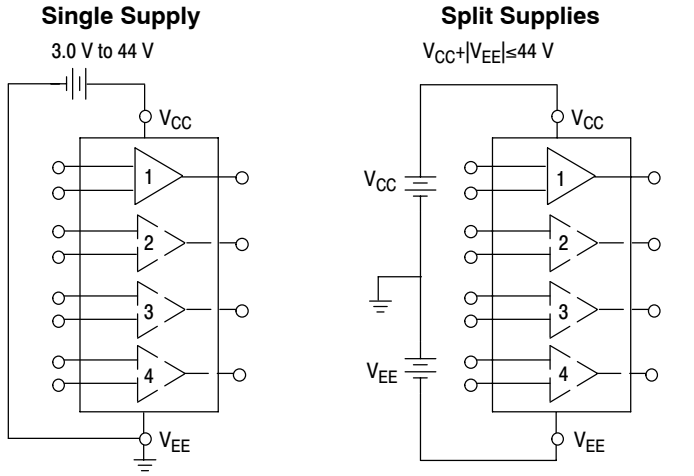
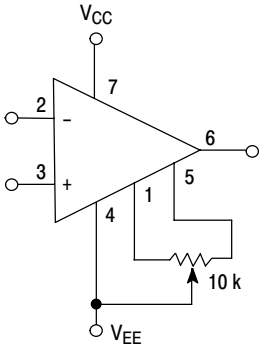


Figure 2. Power Supply Configurations



Offset nulling range is approximately ±80 mV with a 10 k potentiometer (MC33071, MC34071 only).

Figure 3. Offset Null Circuit

ORDERING INFORMATION

Op Amp Function	Device	Operating Temperature Range	Package	Shipping†
Single	MC34071P	T_A = 0° to +70°C	PDIP−8	50 Units / Rail
	MC34071PG		PDIP−8 (Pb−Free)	
	MC34071AP		PDIP−8	50 Units / Rail
	MC34071APG		PDIP−8 (Pb−Free)	
	MC34071D		SOIC−8	98 Units / Rail
	MC34071DG		SOIC−8 (Pb−Free)	
	MC34071DR2		SOIC−8	2500 / Tape & Reel
	MC34071DR2G		SOIC−8 (Pb−Free)	
	MC34071AD		SOIC−8	98 Units / Rail
	MC34071ADG		SOIC−8 (Pb−Free)	
	MC34071ADR2		SOIC−8	2500 / Tape & Reel
	MC34071ADR2G		SOIC−8 (Pb−Free)	
	MC33071D	T_A = −40° to +85°C	SOIC−8	98 Units / Rail
	MC33071DG		SOIC−8 (Pb−Free)	
	MC33071DR2		SOIC−8	2500 / Tape & Reel
	MC33071DR2G		SOIC−8 (Pb−Free)	
	MC33071AD		SOIC−8	98 Units / Rail
	MC33071ADG		SOIC−8 (Pb−Free)	
	MC33071ADR2		SOIC−8	2500 / Tape & Reel
	MC33071ADR2G		SOIC−8 (Pb−Free)	
	MC33071AP		PDIP−8	50 Units / Rail
	MC33071APG		PDIP−8 (Pb−Free)	
	MC33071P		PDIP−8	
	MC33071PG		PDIP−8 (Pb−Free)	
Dual	MC34072P	T_A = 0° to +70°C	PDIP−8	
	MC34072PG		PDIP−8 (Pb−Free)	
	MC34072AP		PDIP−8	
	MC34072APG		PDIP−8 (Pb−Free)	
	MC34072D		SOIC−8	98 Units / Rail
	MC34072DG		SOIC−8 (Pb−Free)	
	MC34072AD		SOIC−8	
	MC34072ADG		SOIC−8 (Pb−Free)	
	MC34072DR2		SOIC−8	2500 Units / Tape & Reel
	MC34072DR2G		SOIC−8 (Pb−Free)	
	MC34072ADR2		SOIC−8	
	MC34072ADR2G		SOIC−8 (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

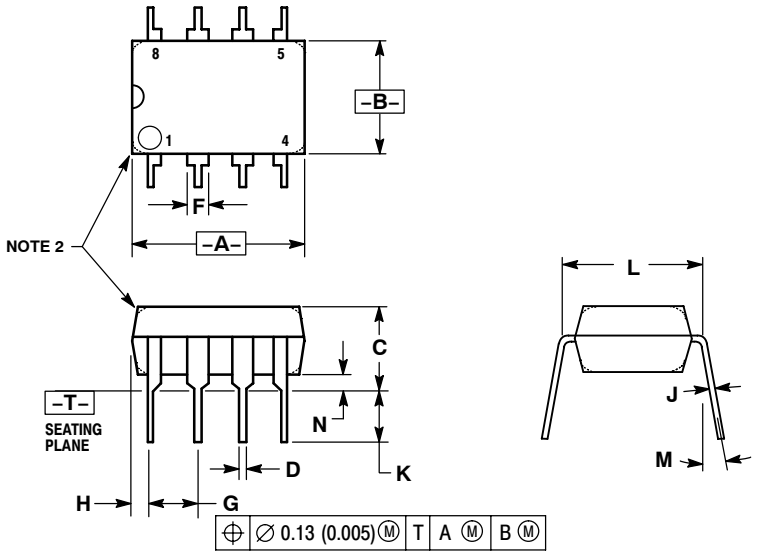
ORDERING INFORMATION (continued)

Op Amp Function	Device	Operating Temperature Range	Package	Shipping†
Dual	MC33072P	T_A = −40° to +85°C	PDIP−8	50 Units / Rail
	MC33072PG		PDIP−8 (Pb−Free)	
	MC33072AP		PDIP−8	
	MC33072APG		PDIP−8 (Pb−Free)	
	MC33072D		SOIC−8	98 Units / Rail
	MC33072DG		SOIC−8 (Pb−Free)	
	MC33072AD		SOIC−8	
	MC33072ADG		SOIC−8 (Pb−Free)	
	MC33072DR2		SOIC−8	2500 / Tape & Reel
	MC33072DR2G		SOIC−8 (Pb−Free)	
	MC33072ADR2		SOIC−8	
	MC33072ADR2G		SOIC−8 (Pb−Free)	
	MC34072VD	T_A = −40° to +125°C	SOIC−8	98 Units / Rail
	MC34072VDG		SOIC−8 (Pb−Free)	
	MC34072VDR2		SOIC−8	2500 / Tape & Reel
	MC34072VDR2G		SOIC−8 (Pb−Free)	
	MC34072VP		PDIP−8	50 Units / Rail
	MC34072VPG		PDIP−8 (Pb−Free)	
Quad	MC34074P	T_A = 0° to +70°C	PDIP−14	25 Units / Rail
	MC34074PG		PDIP−14 (Pb−Free)	
	MC34074AP		PDIP−14	
	MC34074APG		PDIP−14 (Pb−Free)	
	MC34074D		SOIC−14	55 Units / Rail
	MC34074DG		SOIC−14 (Pb−Free)	
	MC34074AD		SOIC−14	
	MC34074ADG		SOIC−14 (Pb−Free)	
	MC34074ADR2		SOIC−14	2500 Units / Tape & Reel
	MC34074ADR2G		SOIC−14 (Pb−Free)	
	MC34074DR2		SOIC−14	
	MC34074DR2G		SOIC−14 (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

PDIP−8
P SUFFIX
CASE 626−05
ISSUE L



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040