Signal Analysis

Probing TCK and RTCK

The output (TCK) and return (RTCK) test clocks are easily accessible via the target board's JTAG header on pin 11 (TCK) and pin 9 (RTCK). Attaching oscilloscope probes to these pins will give you the ability to view the clock synchronization with and without the adapter in place.

Figure 6 below shows the output of the test clock signals using an emulator that does not handle the adaptive clocking feature of the TI OMAP cores.

For this example, measurements were made with the emulator connected to an OSK5912 as the target board. You can see that the clocks are not synchronized, which can lead to data corruption and reduced performance.

Figure 7 shows the output from the same clock signals, using the same emulator connected to the same OSK5912 target board.

The only difference is that we inserted the JACK between the target board's JTAG header and the JTAG connector of the emulator.

This shows that, without changing the emulator, target board, or any settings, the clock edges are fully synchronized. The TCK signal is ***adapting*** to the changes in RTCK from the OMAP device's core clock.

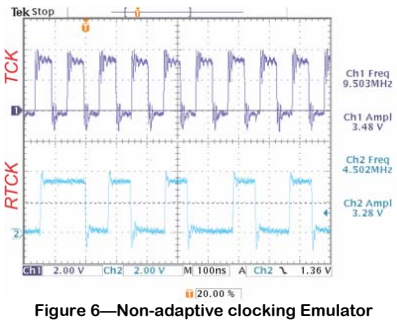

Figure 6—Non-adaptive clocking Emulator

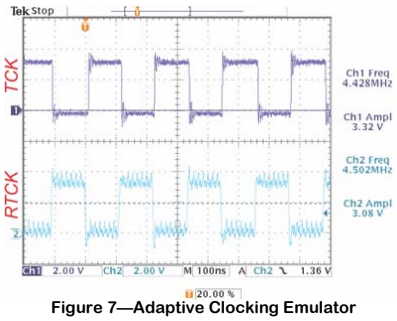

Figure 7—Adaptive Clocking Emulator

Solving the TRST Issue with the TI XDS510

XDS510-class emulators that depend on the TI SN74ACT8990 test bus controller (TBC) to assert the TRST signal are susceptible to a dead-lock condition with certain OMAP cores that stop RTCK when TRST is asserted. Because these cores stop RTCK, the TBC enters a suspended state, never updates, and will not clear the asserted TRST signal.

To solve this issue, the adapter board will route TCK to RTCK if it detects RTCK has stopped when TRST is asserted (see Figure 3). You will find that the TI XDS510 ISA card and other TBC-based emulators will now work with all OMAP devices when this adapter kit is being used.

XDS560-class emulators, which do not rely on the TBC for asserting TRST, will not be affected by the JACK's TRST logic.

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QUICK START GUIDE

Blackhawk™ JTAG Adaptive Clocking Kit for OMAP™

Overview

The JTAG Adaptive Clocking Kit (JACK), shown in figure 1, is designed to allow JTAG emulators for TI DSPs to synchronize with the adaptive clocking cores of Texas Instruments OMAP™ devices providing complete data integrity and increased performance.

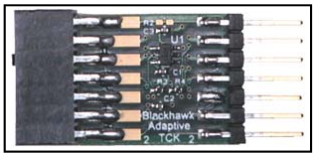


Figure 1 - JACK hardware

Part No. BH-EMU-JACK

What is Adaptive Clocking?

Adaptive clocking is a feature of synthesizable cores, introduced by ARM® Ltd. and adopted by TI in their OMAP platform, wherein the input test clock (TCK) is delayed and synchronized with the core clock before producing the output clock (RTCK). Emulators need to ***adapt*** to this changing RTCK signal.

During this delay (synchronizing period) the target core samples Test Data In (TDI), Test Mode Select (TMS), and TCK with the core clock. This delay is variable and changes in real time, which can cause data corruption.

Figure 2 shows an example of this synchronizing mechanism inside the OMAP processor core. Here you can see the multi-stage synchronizer consisting of several D-triggers, which is dependant on the core clock rate.

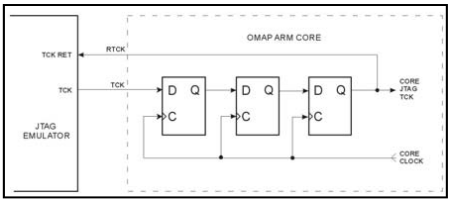


Figure 2—OMAP Adaptive Clocking Mechanism

Figure 3 illustrates the JACK logic to handle these real time changes to RTCK. The resulting logic will maintains synchronization with the JTAG signals as the rate of the OMAP core clock changes.

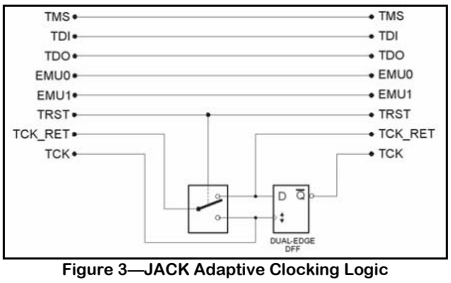


Figure 3—JACK Adaptive Clocking Logic

*You may find **emulator** release notes that describe setup changes (**workarounds**) that are necessary to operate with these TI OMAP adaptive clocking cores. This usually involves decreasing the output TCK rate of the emulator. While this may seem to correct the problem, the **data** and clock signals will still **not** be **synchronized** with the OMAP core clock and you will only **decrease performance**.*

Compatibility

This JACK is designed to be compatible with the traditional 14-pin emulators supporting the common JTAG functions and signals. This includes XDS510™-class and XDS560™-class emulators. The JACK will also work when connected to non-adaptive clocking targets.

Orientation

The JACK is keyed (pin 6), but care should be taken when connecting it to a target board JTAG header or emulator. Pin 1 of the JACK socket should align with pin 1 on the target board header.

Figure 4 shows the JACK connected to a target board's JTAG header. The emulator can now be connected to the JACK in the same manner it would normally be connected to the target board.

WARNING

If the JACK is installed incorrectly, damage can occur to the target board, emulator, and adapter. The adapter is keyed, and so should the emulator's connector and target board header.

Be sure to align connections correctly, with no power applied to the emulator or target board.

The JACK is NOT hot-pluggable!

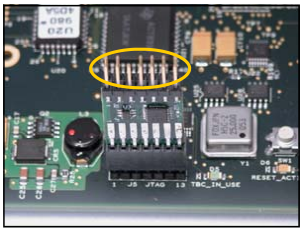


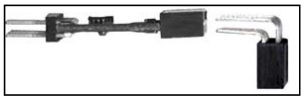
Figure 4—JACK connected to a target board's JTAG header

Optional Configurations

The JACK ships with an additional right-angle connector, pictured in options 1 and 2. This connector is also keyed to match the standard TI 14-pin JTAG header. The right angle connector is provided to allow two additional configurations where the straight, vertical connection will not work.

Each right-angle option can be easily configured by attaching the right-angle connector to a different end of the JACK. Options 1 and 2, pictured here, show the different orientations that are possible and highlights how the right angle connecter should be attached the JACK.

If the right-angle connector is attached, the resulting JACK will have a keyed socket to attach to a target board, and keyed header where the emulator can be attached.



Option 1

Option 2

Mechanical Considerations

The JACK hardware was designed using quality components, fast LVC logic, and an FR4 base-laminate material suitable of supporting most legacy board designs and speeds.

The JACK has an impedance of approximately 50 ohms to reduce the chance of mismatch with typical target boards.

Table 1 provides the signal to pin relationship. These signals follow the standard TI JTAG layout recommendations.

The header and socket on the JACK conform to the standard 0.100" spacing in a double row configuration.

Pin	Name	Pin	Name
1	TMS	2	$\overline{\text{TRST}}$
3	TDI	4	TDIS
5	TVD	6	KEY
7	TDO	8	GND
9	RTCK	10	GND
11	TCK	12	GND
13	EMU0	14	EMU1

Table 1 - 14-pin JTAG Header Pin-out

Optimization

Using the JACK does not require any changes to your emulator or CCStudio setup. The adapter will automatically synchronize the JTAG data and clocks for increased stability and data integrity.

However, to maximize performance, you should set your emulator to generate its maximum TCK frequency, if applicable. Increasing your emulator's TCK output rate will not affect data integrity. Below is a description covering some of the popular TI JTAG emulators and how you can optimize your configuration for maximum performance.

- **Fixed TCK Emulators**

  Emulators that have a fixed TCK rate are typically XDS510-class and generate a TCK frequency between 10 or 12 MHz (please consult your emulator's documentation for the correct specifications on your emulator). These fixed TCK emulators, such as most XDS510 ISA, Parallel Port, and USB versions, do not require any changes to get the benefits from the JTAG Adaptive Clocking Kit.

  Just insert the JACK between the 14-pin JTAG connectors of the emulator and target board. Then setup and start CCS as you would normally and the adapter board will automatically synchronize the TCK, TCK_RET, and data signals.

- **Variable TCK Capable Emulators**

  Emulators that support variable TCK frequencies, such as the Blackhawk USB510 and PCI510 JTAG models, as well as all XDS560-class emulators, can also be used without changes.

  However, these emulators typically support TCK rates well above 10 MHz. So you can configure them to generate their highest TCK rate possible to yield maximum performance. TCK frequencies are usually set with a configuration parameter (i.e. in CCSetup), but please refer to your emulator's documentation on how to set a maximum TCK rate. Figure 5 shows how to change the setting for an XDS560-class emulator from the Connection Properties dialog in CCStudio v3.1 setup.

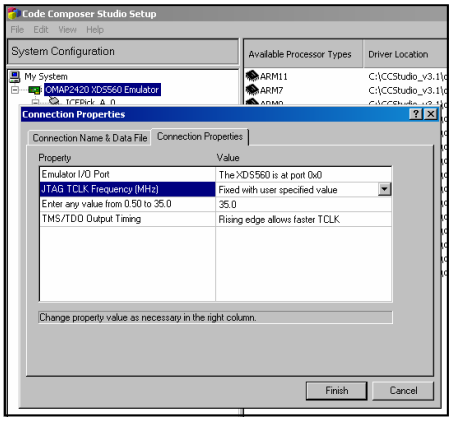


Figure 5—Setting the maximum TCK rate

If you are using an OMAP device and have been instructed to slow down the TCK rate of the emulator you are using, this workaround will no longer be necessary. You can set it back to its original, maximum value. The data will be synchronized and performance will be back to its original speed.

DISCLAIMERS

Read the following for important information to be aware of when using this hardware.

- **Blackhawk is not responsible for any damage that may occur to the JACK, target board, or emulator if misused, mishandled, or forced into place.**
- **The JACK is not intended to be hot pluggable, damage may occur. Make sure you emulator and target board are not powered when making connections.**
- **The JACK is keyed (pin 6). Removing or modifying the JACK's connectors is not recommended or supported and can harm connected hardware.**