The World of AVR32 Series RISC Microcontrollers

Member of ATMEL RISC MCU Family

Product Overview 2008

32-bit AVR32 RISC MCU for Linux® Application and Real-Time System

- USB2.0 HS Device and HS OTG
- LCD Controller and Graphic Accelerator
- Up to 2 x Fast Ethernet MAC 10/100Mbit/s
- Fast embedded Flash/SRAM and external bus interface
- Up to 280DMIPS at 200MHz
- Linux® and RTOS support

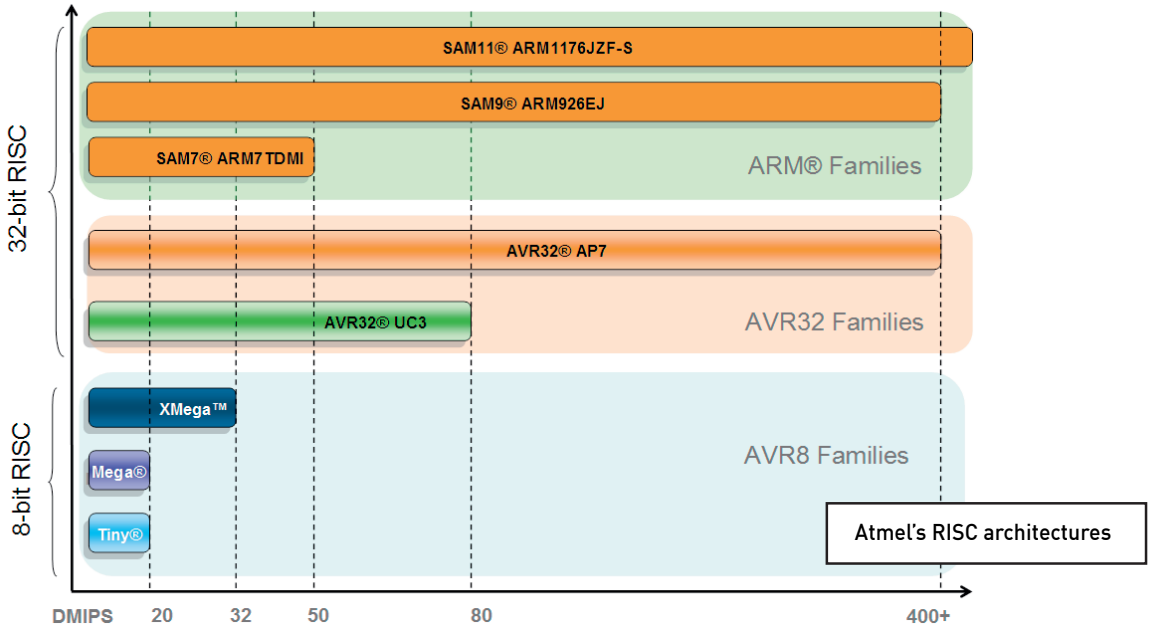
MSC - Distributor of

MICROCOMPUTERS · SYSTEMS · COMPONENTS · VERTRIEBS GMBH

AVR32 RISC MCU Families

Welcome to the World of Atmel's RISC microcontrollers

Join the big world of Atmel's 8-bit and 32-bit RISC MCU families!
From lowest cost **ATTINY**, high performance **ATMEGA** or new **XMEGA** family, Atmel's 8-bit AVR portfolio covers devices from 16 MIPS up 32 MIPS with pin counts from 8 up to 100 pins. Flash memories from 1K up to 256K are available.

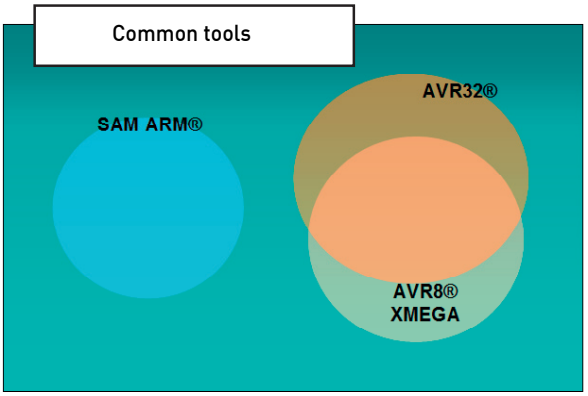


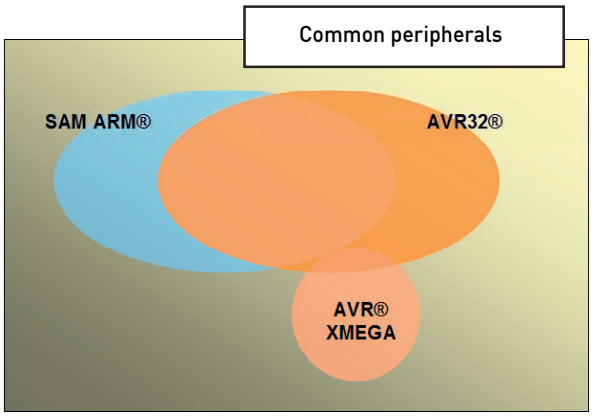
Atmel's new **AVR32 32-bit** core is introduced in **UC3** flash based derivates and in the **AP7** application processor products. A lot of intelligent technologies make this core the winner in performance and power consumption over all existing 32-bit technologies. Here, will find flash based products up to 512K with a lot of communication interfaces as well as high performance processors with MMU and cashes especially for embedded Linux, which is supported directly by Atmel.

Atmel's **SAM ARM®** families cover a broad range of products from flash based **SAM7** and **SAM9** products as well as bigger SAM9 machines for Windows CE® and embedded Linux.
A rich set of communication peripherals, lots of smart implementations and different available development tools and operating systems in the market make this products very successful.

Migration

Both AVR32 and SAM ARM® use many common peripherals, enabling migration between the families much more easier, than jumping between different MCU technology.



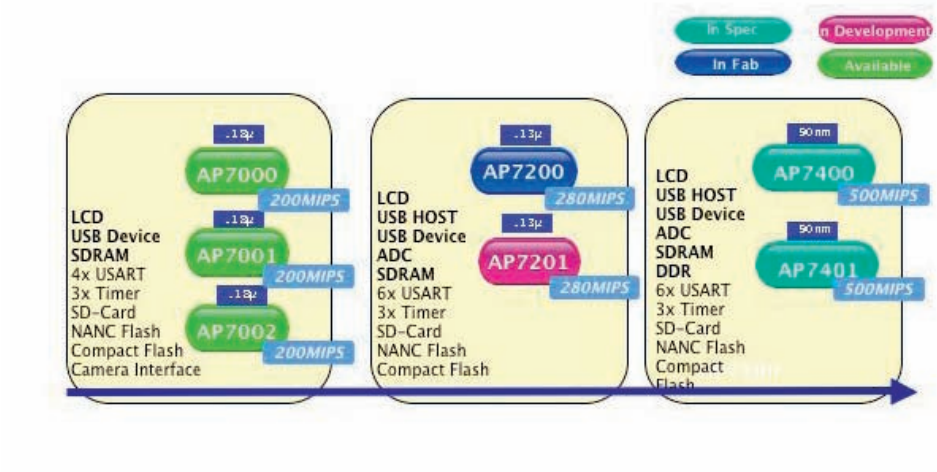


Tools

AVR32, AVR and XMEGA products come with dedicated free of charge AVR Studios and can be debugged with JTAGICE-MK2. So feel free to start with AVR, enlarge your application to XMEGA and proceed to AVR32 MCUs with the same set of tools.

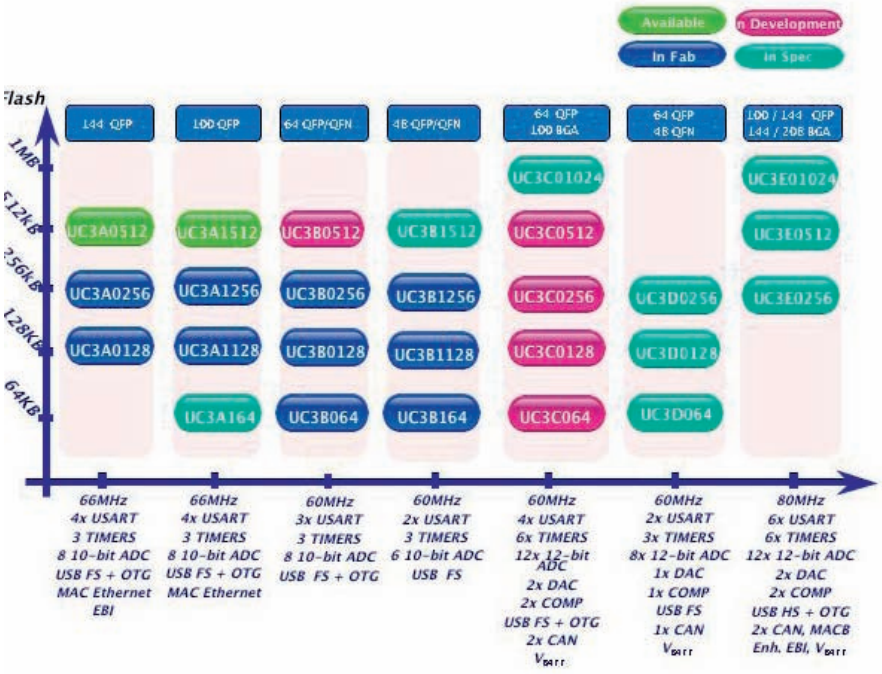
AP7 Family Roadmap

The AVR32 Family is currently the most expanding product in the 32-bit area. This is valid for both, the flash-less AP7 Family and the embedded flash UC3. The AP7 family is equipped with all system components and peripherals to build up digital systems for process controlling and visualization which normally are engaged with full fledged operating system like Linux. The AT32AP7000 was the first product on the market which features highest performance at low power consumption and was targeting to the portable console market. But the huge offer in software, specially the Linux Kernel and driver support directly from Atmel, was ideal for a lot of customer to use this package for their application. All next products based on AP7 will have new or additional peripherals and also will be shrinked for more speed and lower power consumption.



UC3 Family Roadmap

The UC3 family is an optimized version of the AVR32 Core for real-time systems and will be equipped with embedded flash. It optimally fits into application where highest performance at low power consumption is needed and also PCB space is less available. The UC3 Core implements a high efficient DSP instruction set and speed up signal processing applications significantly. The UC3 family is planned to be automotive AEC-Q100 as well.



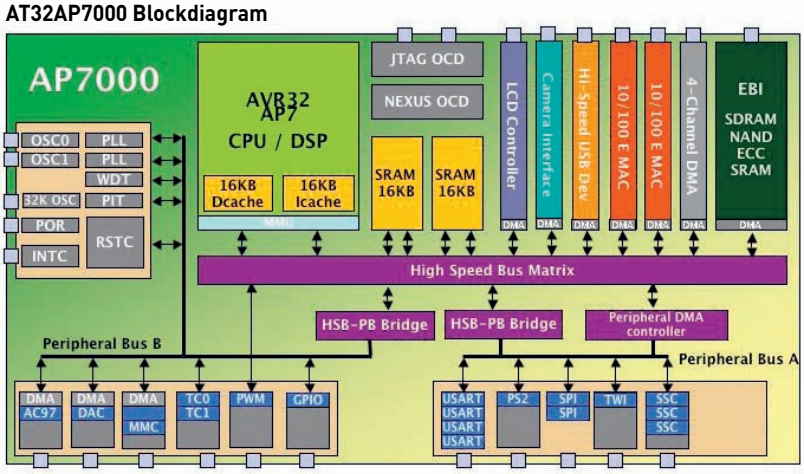
Family Overview AT32AP7000

The **AT32AP7000** is the first AVR32-based processor family and the first to integrate on a single chip, virtually all the functionalities required for multimedia systems deployed in cell phones, digital cameras, PDAs, automotive infotainment, set top boxes, and home entertainment systems, as well as network switches/routers and printers. The embedded Pixel-Coprocessor accelerates processing of images and video streams and is directly connected to the core to perform single cycle execution on processor speed.

The AT32AP7000 operates at 210 MIPS with a 150 MHz clock. It features 32K bytes of SRAM directly connected to the high-speed bus matrix, an **external bus interface** with controllers for SDRAM and static memories including **NAND Flash** and CompactFlash™ with ECC. Its extensive peripheral set includes an **USB High Speed Device** interface, two 10/100 Base-T **Ethernet MAC**, **Image Sensor Interface**, **Multimedia Card Interface** (MCI), a **LCD-Controller** for TFT and STN Displays, Synchronous Serial Controllers (SSC), USARTs, Master/Slave Serial Peripheral Interfaces (SPI), two three-channel 16-bit Timer Counter (TC) and a Two Wire Interface (TWI). Up to five GPIO Controller (each 32-bit wide) are selecting general I/O's or do connect the peripherals to dedicated pins via multiplexer. Peripheral DMA channels maximize the data throughput between these interfaces and the on- and off-chip memories.

The AT32AP7000 is available in a 256-ball CTBGA RoHS-compliant package providing up to 160 GPIO multiplexed with peripherals.

AT32AP7000 Blockdiagram



AT32AP7000 Development Tools

AP7000 is supported by the **ATSTK1000** evaluation kit and AT90JTAGICE-mkII debugger. Also an ultra low-cost Network Reference Design Kit **ATNGW100** with pre-installed Linux Image is available.

All related Software and documentation may be downloaded via www.atmel.com/products/avr32 :

- Ready to use example projects
- Linux demonstration software
- Getting Started Application Notes
- Schematics, BOM and Gerber files
- Free Atmel tools (Linux Kernel and BSP)

ATSTK1000 is equipped with AT32AP7000-CTUT (CTBGA).

MSC's **AT32AP7000-Startup Paket** gives you all you need for your first AP7000 design: ATSTK1000, AT90JTAGICE-mkII. The BSP and Linux Kernel is supported by Atmel and can be downloaded free of cost.

AT32AP7000 in brief

System	
7	AVR32, 150MHz Pixel-Coprocessor 16-layer AHB Matrix
Debug	JTAG / Nexus Class III
Caches	16K-I, 16K-D
MMU	yes
Memory	
Flash	-
SRAM	2 x 16KB
Ext. Bus interface	8/16/32-bit static,
	16/32-bit dynamic,
	NAND (ECC), CompactFlash™
Boot	EBI CS0
Communication	
Ethernet	2 x MAC 10/100 RMII/MII with DMA
USB UDP UHP	1 USB2.0 HS Device
U(S)ART	4 with DMA
SPI	2 with DMA
TWI (I²C)	1 (Master)
SSC	3 with DMA
Timer	
16-bit	6 x with Cap/Com
RTT	1
Watchdog	1
PWM	4 ch / 20-bit
Multimedia	
LCD Contr.	2048 x 2048 24-bit
Camera IF	1
MMC IF	1
Audio DAC	1
AC97	1
Misc.	
PS2	1
I/O	160 max.
Oscillators	2 x Osc., 2 x PLL
System	POR, Shut Down Ctrl.
Evaluation Boards	
	
ATSTK1000 Resources	
SDRAM	8MByte
Flash	8MByte
SD-Card	256MByte
ATNGW100 Resources	
SDRAM	32MByte
Flash	8MByte
DataFlash™	8MByte

Schematics, BOM, Gerber etc. provided by Atmel.

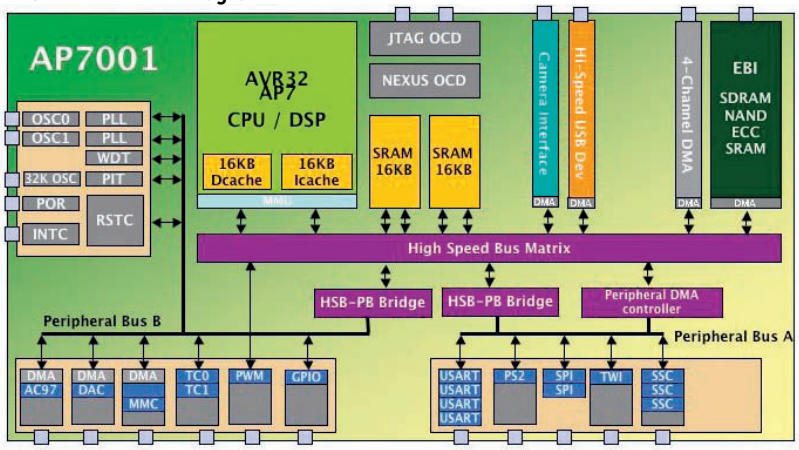
Family Overview AT32AP7001

The **AT32AP7001** is a device reduction of the full-fledged AP7000 related to some peripherals. It can be used in applications where no Ethernet connection and no process visualization are needed. The AP7001 can be used for applications deployed in cell phones, digital cameras, automotive infotainment, process automation, set top boxes, and home entertainment systems. The embedded Pixel-Coprocessor accelerates processing of images and video streams and is directly connected to the core to perform single cycle execution on processor speed.

The AT32AP7001 operates at 210 MIPS with a 150 MHz clock. It features 32K bytes of SRAM directly connected to the high-speed bus matrix, an **external bus interface** with controllers for SDRAM and static memories including **NAND Flash** and CompactFlash™ with ECC. Its extensive peripheral set includes a **USB High Speed Device** interface, **Image Sensor Interface, Multimedia Card Interface** (MCI), Synchronous Serial Controllers (SSC), USARTs, Master/Slave Serial Peripheral Interfaces (SPI), two three-channel 16-bit Timer Counter (TC), and a Two Wire Interface (TWI). Up to three GPIO Controller (each 32-bit wide) are selecting general I/O's or do connect the peripherals to dedicated pins via multiplexer. Peripheral DMA channels maximize the data throughput between these interfaces and the on- and off-chip memories.

The AT32AP7001 is available in a 208-ball QFP RoHS-compliant package

AT32AP7001 Blockdiagram



AT32AP7000 Development Tools

AP7000 is supported by the **ATSTK1000** evaluation kit and AT90JTAGICE-mkII debugger. Also an ultra low-cost Network Reference Design Kit **ATNGW100** with pre-installed Linux Image is available.

All related Software and documentation may be downloaded via www.atmel.com/products/avr32 :

- Ready to use example projects
- Linux demonstration software
- Getting Started Application Notes
- Schematics, BOM and Gerber files
- Free Atmel tools (Linux Kernel and BSP)

ATSTK1000 is equipped with AT32AP7000-CTUT (CTBGA).

MSC's **AT32AP7000-Startup Paket** gives you all you need for your first AP7000 design: ATSTK1000, AT90JTAGICE-mkII. The BSP and Linux Kernel is supported by Atmel and can be downloaded free of cost.

AT23AP7001 in brief

System	
CPU	AVR32, 150MHz Pixel-Coprocessor 16-layer AHB Matrix
Debug	JTAG / Nexus Class III
Caches	16K-I, 16K-D
MMU	yes
Memory	
Flash	-
SRAM	2 x 16KB
Ext. Bus interface	8/16/32-bit static, 16/32-bit dynamic, NAND (ECC), CompactFlash™
Boot	EBI CS0
Communication	
USB UDP UHP	1 USB2.0 HS Device
U(S)ART	4 with DMA
SPI	2 with DMA
TWI (I²C)	1 (Master)
SSC	3 with DMA
Timer	
16-bit	6 x with Cap/Com
RTT	1
Watchdog	1
PWM	4 ch / 20-bit
Multimedia	
Camera IF	1
MMC IF	1
Audio DAC	1
AC97	1
Misc.	
PS2	1
I/O	160 max.
Oscillators	2 x Osc., 2 x PLL
System	POR, Shut Down Ctrl.
Evaluation Boards	
	
ATSTK1000 Resources	
SDRAM	8MByte
Flash	8MByte
SD-Card	256MByte
ATNGW100 Resources	
SDRAM	32MByte
Flash	8MByte
DataFlash™	8MByte

Schematics, BOM, Gerber etc. provided by Atmel.

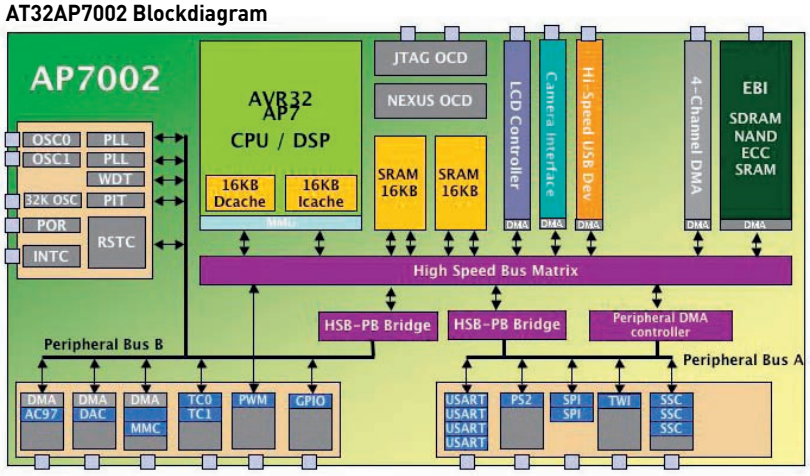
Family Overview AT32AP7002

The **AT32AP7002** is a device reduction of the full-fledged AP7000 related to some peripherals. It can be used in applications where no Ethernet connection is needed but process visualization is an issue. The AP7002 can be used for applications deployed in cell phones, digital cameras, automotive infotainment, process automation, set top boxes, and home entertainment systems. The embedded Pixel-Coprocessor accelerates processing of images and video streams and is directly connected to the core to perform single cycle execution on processor speed.

The AT32AP7002 operates at 210 MIPS with a 150 MHz clock. It features 32K bytes of SRAM directly connected to the high-speed bus matrix, an **external bus interface** with controllers for SDRAM and static memories including **NAND Flash** and CompactFlash™ with ECC. Its extensive peripheral set includes a **USB High Speed Device** interface, **Image Sensor Interface, Multimedia Card Interface** (MCI), a **LCD-Controller** for TFT and STN Displays, Synchronous Serial Controllers (SSC), USARTs, Master/Slave Serial Peripheral Interfaces (SPI), two three-channel 16-bit Timer Counter (TC) and a Two Wire Interface (TWI). Up to three GPIO Controller (each 32-bit wide) are selecting general I/O's or do connect the peripherals to dedicated pins via multiplexer. Peripheral DMA channels maximize the data throughput between these interfaces and the on- and off-chip memories.

The AT32AP7002 is available in a 196-ball CTBGA RoHS-compliant package providing up to 88 GPIO multiplexed with peripherals.

AT32AP7002 Blockdiagram



AT32AP7000 Development Tools

AP7000 is supported by the **ATSTK1000** evaluation kit and AT90JTAGICE-mkII debugger. Also an ultra low-cost Network Reference Design Kit **ATNGW100** with pre-installed Linux Image is available.

All related Software and documentation may be downloaded via www.atmel.com/products/avr32 :

- Ready to use example projects
- Linux demonstration software
- Getting Started Application Notes
- Schematics, BOM and Gerber files
- Free Atmel tools (Linux Kernel and BSP)

ATSTK1000 is equipped with AT32AP7000-CTUT (CTBGA).

MSC's **AT32AP7000-Startup Paket** gives you all you need for your first AP7000 design: ATSTK1000, AT90JTAGICE-mkII. The BSP and Linux Kernel is supported by Atmel and can be downloaded free of cost.

AT32AP7002 in brief

System	
CPU	AVR32, 150MHz Pixel-Coprocessor 16-layer AHB Matrix
Debug	JTAG / Nexus Class III
Caches	16K-I, 16K-D
MMU	yes
Memory	
Flash	-
SRAM	2 x 16KB
Ext. Bus interface	8/16/32-bit static, 16/32-bit dynamic, NAND (ECC), CompactFlash™
Boot	EBI CS0
Communication	
USB UDP UHP	1 USB2.0 HS Device
U(S)ART	4 with DMA
SPI	2 with DMA
TWI (I²C)	1 (Master)
SSC	3 with DMA
Timer	
16-bit	6 x with Cap/Com
RTT	1
Watchdog	1
PWM	4 ch / 20-bit
Multimedia	
LCD Contr.	2048 x 2048 24-bit
Camera IF	1
MMC IF	1
Audio DAC	1
AC97	1
Misc.	
PS2	1
I/O	160 max.
Oscillators	2 x Osc., 2 x PLL
System	POR, Shut Down Ctrl.
Evaluation Boards	
	
ATSTK1000 Resources	
SDRAM	8MByte
Flash	8MByte
SD-Card	256MByte
ATNGW100 Resources	
SDRAM	32MByte
Flash	8MByte
DataFlash™	8MByte

Schematics, BOM, Gerber etc. provided by Atmel.

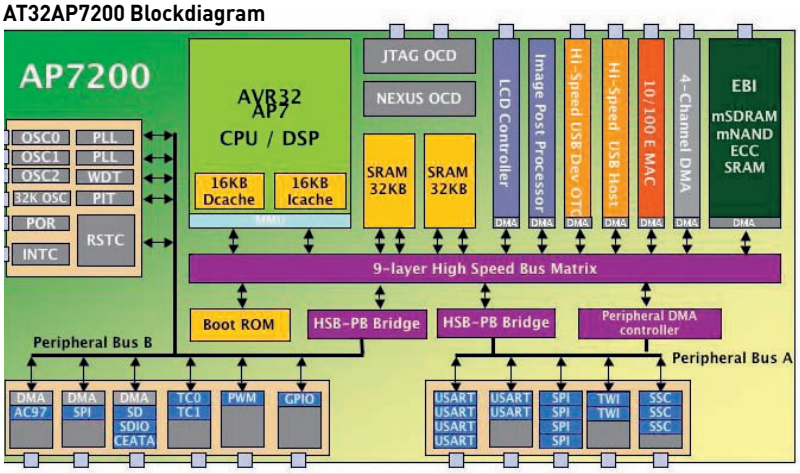
Family Overview AT32AP7200

The **AT32AP7200** is the second Generation full-fledged AVR32-based processor families and expands the previous version by additional peripherals required for multimedia systems deployed in cell phones, digital cameras, PDAs, automotive infotainment, set top boxes, and home entertainment systems, as well as network switches/routers and printers. The embedded Pixel-Coprocessor accelerates processing of images and video streams and is directly connected to the core to perform single cycle execution on processor speed.

The AT32AP7200 operates at 280 DMIPS with a 200 MHz clock. It features 32K bytes of SRAM directly connected to the high-speed bus matrix, an **external bus interface** with controllers for SDRAM and static memories including **NAND Flash** and CompactFlash™ with ECC. Its extensive peripheral set includes a **USB High Speed Host** interface, a **High-Speed On-The-Go** interface, one 10/100 Base-T **Ethernet MAC, Multimedia Card Interface** (MCI), a **LCD-Controller** for TFT and STN Displays with a **Image Post Processor**, Synchronous Serial Controllers (SSC), USARTs, Master/Slave Serial Peripheral Interfaces (SPI), two three-channel 16-bit Timer Counter (TC), a Two Wire Interface (TWI) and a six-channel 10-bit ADC with Touch Screen support. Up to six GPIO Controller (each 32-bit wide) are selecting general I/O's or do connect the peripherals to dedicated pins via multiplexer. Peripheral DMA channels maximize the data throughput between these interfaces and the on- and off-chip memories.

The AT32AP7200 is available in a 324-ball BGA RoHS-compliant package providing up to 189 GPIO multiplexed with peripherals.

AT32AP7200 Blockdiagram



AT32AP7200 Development Tools

The AT32AP7200 will be supported by a future evaluation board and the existing AT90JTAGICE-mkII debugger. The evaluation board will be designed for industrial use with pre-installed Linux Image and may be ordered in high quantities as well.

All related Software and documentation may be downloaded via www.atmel.com/products/avr32 :

- Ready to use example projects
- Linux demonstration software
- Getting Started Application Notes
- Schematics, BOM and Gerber files
- Free Atmel tools (Linux Kernel and BSP)

ATSTK1000 is equipped with AT32AP7000-CTUT (BGA).

MSC's **AT32AP7200-Startup Paket** gives you all you need for your first AP7000 design: The Evaluation Board and the AT90JTAGICE-mkII. The BSP and Linux Kernel is supported by Atmel and can be downloaded free of cost.

AT32AP7200 in brief

System	
CPU	AVR32, 200MHz Pixel-Coprocessor 9-layer AHB Matrix
Debug	JTAG / Nexus Class III
Caches	16K-I, 16K-D
MMU	yes
Memory	
Flash	-
SRAM	2 x 32KB
Ext. Bus interface	8/16/32-bit static, 16/32-bit dynamic, NAND (ECC), CompactFlash™
Boot	EBI CS0
Communication	
Ethernet	1 x MAC 10/100 RMII/MII with DMA
USB UDP UHP	1 USB2.0 HS OTG 1 USB2.0 HS Host
U(S)ART	6 with DMA
SPI	1 with DMA / 4 Ch.
TWI (I²C)	2 (Master/Slave)
SSC	3 with DMA
Timer	
16-bit	6 x with Cap/Com
RTT	1
Watchdog	1
PWM	4 ch / 20-bit
Multimedia	
LCD Contr.	2048 x 2048 24-bit
MPOP	Media Post Processor
MMC IF	1
Audio DAC	1
AC97	1
Misc.	
ADC	Touch Screen Support
Keypad	1 x Rotary Encoder
DIE IF	1
Oscillators	3 x Osc., 3 x PLL
System	POR, Shut Down Ctrl.

Schematics, BOM, Gerber etc. provided by Atmel.

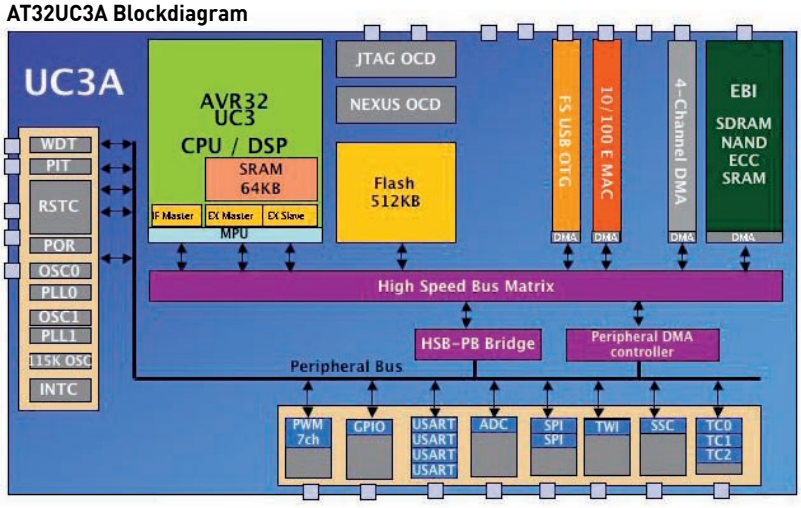
Family Overview AT32UC3A

The **AT32UC3A** is based on the high-performance AVR32 core with logic optimization for real-time applications. Cache and MMU have been removed and instead a memory protection unit (MPU) was added. Also the core pipeline was reduced to a 3-stage pipeline to achieve the requirements needed for real-time systems.

The AT32UC3A operates at 80 DMIPS with a 66 MHz clock. It features up to 64K bytes of SRAM directly connected to the core and performs single cycle access at maximum processor speed. The AT32UC3A family is designed for communication systems providing fast **Ethernet 10/100Mbits/s** and **Full-Speed USB2.0 OTG** at very low power consumption. Additional an **external bus interface** with controllers for SDRAM and static memories expands the embedded Flash and SRAM by cost effective memory options and also do provide more system functionality. Synchronous Serial Controllers (SSC), many USART's, Master/Slave Serial Peripheral Interfaces (SPI), two three-channel 16-bit Timer Counter (TC), a Two Wire Interface (TWI) and a **10-bit ADC** are part of this implementation and are speed up by the peripheral DMA controller to reduce CPU intervention. Up to 109-Pins are controlled by the Parallel I/O Controller and do switch connection for general purpose I/O's or peripherals.

The AT32UC3A is available in a 144-pin TQFP RoHS-compliant package providing all described functionality and also in a 100-pin TQFP package with no external bus interface.

AT32UC3A Blockdiagram



AT32UC3A Development Tools

The AT32UC3A is supported by ATEVK1100 evaluation kit and AT90JTAGICE-mkII debugger. It is pre-installed with a Panel Controller application also available in source code and support Mass-Storage Device Class a Web Server Application and much more. All source code is available through the UC3A Software Framework free of cost.

It may be downloaded via www.atmel.com/products/avr32 :

- Ready to use example projects
- Control Panel demonstration software
- Getting Started Application Notes
- Schematics, BOM, Gerber files
- Free Atmel tools (AVR32 Studio Integrated Development Tool)

ATEVK1100 is equipped with AT32UC3A0512-ALUT (TQFP144).

AT32UC3A in brief

System	
CPU	AVR32, 66MHz High-Speed AHB Matrix
Debug	JTAG / Nexus Class 2+
Caches	-
MPU	yes
Memory	
Flash	128/256/512KB
SRAM	32/64/64KB
Ext. Bus interface	8/16-bit static, 16-bit dynamic,
Boot	DFU Bootloader
Communication	
Ethernet	1 x MAC 10/100 RMII/MII with DMA
USB UDP UHP	1 USB2.0 FS OTG
U(S)ART	4 with DMA
SPI	2 with DMA
TWI (I²C)	1 with DMA
SSC	1 with DMA
Timer	
16-bit	3 x with Cap/Com
RTC	1
Watchdog	1
PWM	7 ch / 16-bit
Analogue	
ADC	10-bit / 8ch
Misc.	
I/O	109/69
Oscillators	115KHz RC
	2 x Osc., 2 x PLL
System	POR, BOD
Evaluation Boards	
	
ATEVK1100 Resources	
SDRAM	16Mbit (1M x 16)
DataFlash	8MByte
SD-Card	Slot only
Ethernet	RJ-45
USART	2 x RS232
USB	MiniAB
Display	4 x 20 Characters (SPI)

Schematics, BOM, Gerber etc. provided by Atmel.

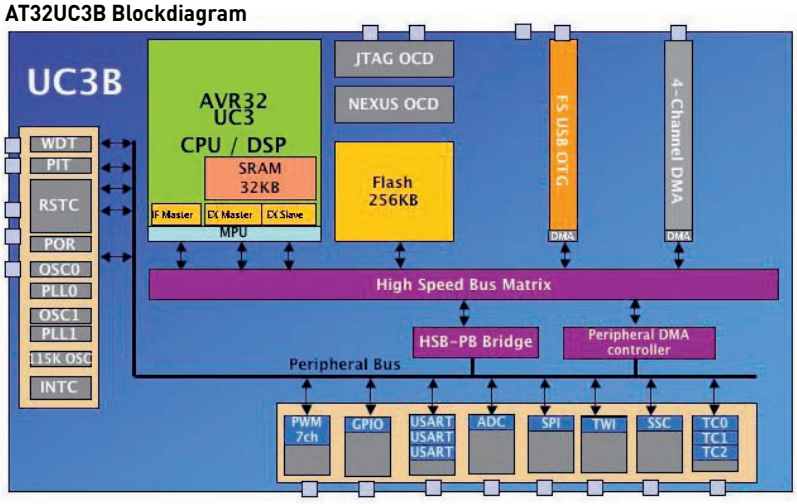
Family Overview AT32UC3B

The **AT32UC3B** is based on the high-performance AVR32 core with logic optimization for real-time applications. Cache and MMU have been removed and instead a memory protection unit (MPU) was added. Also the core pipeline was reduced to a 3-stage pipeline to achieve the requirements needed for real-time systems.

The AT32UC3B operates at 75 DMIPS with a 60 MHz clock. It features up to 32K bytes of SRAM directly connected to the core and performs single cycle access at maximum processor speed. The AT32UC3B family is designed for general purpose low pin-count applications providing **Full-Speed USB2.0 OTG** at very low power consumption. This family is specially fabricated in a very low leakage process which results in **23mA@60MHz at 3.3V** and ideally fits into battery powered applications. Synchronous Serial Controllers (SSC), many USART's, Master/Slave Serial Peripheral Interface (SPI), one three-channel 16-bit Timer Counter (TC), a Two Wire Interface (TWI) and a **10-bit ADC** are part of this implementation and are speed up by the peripheral DMA controller to reduce CPU intervention. Up to 44-Pins are controlled by the Parallel I/O Controller and provide connections for general purpose I/O's or peripherals.

The AT32UC3B is available in a 64-pin TQFP and 64-pin QFN RoHS-compliant package providing all described functionality. Also a 48-pin TQFP package and a 48-pin QFN package with reduced functionality can be offered.

AT32UC3B Blockdiagram



AT32UC3B Development Tools

The AT32UC3B is supported by **ATEVK1101** evaluation kit and AT90JTAGICE-mkII debugger. It is pre-installed with a Panel Controller application also available in source and a PC based Java based Dialog example to provide a quick overview. All source code is available by the UC3B Software Framework free of cost.

It may be downloaded via www.atmel.com/products/avr32 :

- Ready to use example projects
- Control Panel demonstration software
- Getting Started Application Notes
- Schematics, BOM, Gerber files
- Free Atmel tools (AVR32 Studio Integrated Development Env.)

ATEVK1101 is equipped with AT32UC3A0256-A2UT (TQFP64).

AT32UC3B in brieff

System	
CPU	AVR32, 60MHz High-Speed AHB Matrix
Debug	JTAG / Nexus Class 2+
Caches	-
MPU	yes
Memory	
Flash	64/128/256KB
SRAM	16/32/32KB
Boot	DFU Bootloader
Communication	
USB UDP UHP	1 USB2.0 FS OTG
U(S)ART	3 with DMA
SPI	1 with DMA
TWI (I²C)	1 with DMA
SSC	1 with DMA
Timer	
16-bit	3 x with Cap/Com
RTC	1
Watchdog	1
PWM	7 ch / 16-bit
Analogue	
ADC	10-bit / 8ch
Misc.	
I/O	44/28
Oscillators	115KHz RC
	2 x Osc., 2 x PLL
System	POR, BOD
Evaluation Boards	
	
ATEVK1100 Resources	
DataFlash	8MByte
SD-Card	Slot only
Sensors	Accelerometer
	Ligth, Temperature
USART	1 x RS232
USB	MiniAB
Control	Joystick

Schematics, BOM, Gerber etc. provided by Atmel.

AVR32 Selection Guide

Family, Part		Core			Memory								Communication									Video				
AT32 AVR32 Series	Device	CORE	MMU/ I-D Cache	MHz (@85°C)	SRAM Bytes (x32)	FLASH Bytes (x16/x32)	BOOT ROM Bytes	External Businterface	SDRAM EBI	Mem-to-Mem DMA	Peripheral DMA	LIN/J1587 USART	USART/DBGU	Enhanced USART	SPI	TWI	SSC	CAN	USB Device HS/FS	USB Host FS / OTG	Ethernet MAC10/100	AES & Triple-DES	Camera Interface	LCD Controller	Graphic Acceleration	AC97	Audio DAC
AT32 AP7000 Multimedia, low cost, single chip Flashless MCUs																											
AP7000	AT32AP7000-CTUT/R	AVR32	yes/16KB/16KB	150	2x16K	-	-	y	y	y	11	-	4/-	4	2	1	3	-	HS	-	2	-	y	y	-	y	y
	AT32AP7001-ALUT	AVR32	yes/16KB/16KB	150	2x16K	-	-	y	y	y	7	-	4/-	4	2	1	3	-	HS	-	-	-	y	-	-	y	y
	AT32AP7002-CTUT/R	AVR32	yes/16KB/16KB	150	2x16K	-	-	y	y	y	8	-	4/-	4	2	1	3	-	HS	-	-	-	y	y	-	y	y
	AT32AP7200-CTUT	AVR32	yes/16KB/16KB	200	2x32K	-	yes	y	y	y	13	-	6/-	6	4	2	3	-	HS	HS OTG	1	-	-	y	y	y	-
AT32 UC3 low cost, single chip Flash MCUs																											
UC3	AT32UC3A0128-ALUT	UC3	MPU/no/no	66	32K	128K	-	y	y	-	15	-	4/-	4	2	1	1	-	-	FS OTG	1	-	-	-	-	-	-
	AT32UC3A0256-ALUT	UC3	MPU/no/no	66	64K	256K	-	y	y	-	15	-	4/-	4	2	1	1	-	-	FS OTG	1	-	-	-	-	-	-
	AT32UC3A0512-AL UT	UC3	MPU/no/no	66	64K	512K	-	y	y	-	15	-	4/-	4	2	1	1	-	-	FS OTG	1	-	-	-	-	-	-
	AT32UC3A1128-AUT	UC3	MPU/no/no	66	32K	128K	-	-	-	-	15	-	4/-	4	2	1	1	-	-	FS OTG	1	-	-	-	-	-	-
	AT32UC3A1256-AUT	UC3	MPU/no/no	66	64K	256K	-	-	-	-	15	-	4/-	4	2	1	1	-	-	FS OTG	1	-	-	-	-	-	-
	AT32UC3A1512-AUT	UC3	MPU/no/no	66	64K	512K	-	-	-	-	15	-	4/-	4	2	1	1	-	-	FS OTG	1	-	-	-	-	-	-
UC3B	AT32UC3B064-A2UT/Z2UT	UC3	MPU/no/no	60	16K	64K	-	-	-	-	7	-	3/-	2	1	1	1	-	-	FS OTG	-	-	-	-	-	-	-
	AT32UC3B0128-A2UT/Z2UT	UC3	MPU/no/no	60	32K	128K	-	-	-	-	7	-	3/-	2	1	1	1	-	-	FS OTG	-	-	-	-	-	-	-
	AT32UC3B0256-A2UT/Z2UT	UC3	MPU/no/no	60	32K	256K	-	-	-	-	7	-	3/-	2	1	1	1	-	-	FS OTG	-	-	-	-	-	-	-
	AT32UC3B164-AUT/Z1UT	UC3	MPU/no/no	60	16K	64K	-	-	-	-	7	-	3/-	3	1	1	-	-	FS	-	-	-	-	-	-	-	-
	AT32UC3B1128-AUT/Z1UT	UC3	MPU/no/no	60	32K	128K	-	-	-	-	7	-	3/-	3	1	1	-	-	FS	-	-	-	-	-	-	-	-
	AT32UC3B1256-AUT/Z1UT	UC3	MPU/no/no	60	32K	256K	-	-	-	-	7	-	3/-	3	1	1	-	-	FS	-	-	-	-	-	-	-	-

AVR32 AP7 Series

High-Performance MCU for Linux-base Applications:

The AT32AP7 was designed to fit into high-performance, low-power consuming Systems for process control and visualization. The core is equipped with a Memory-Management-Unit (MMU) and Cache for Instructions and Data and so prepared to run full-fledged operation systems like Linux.

The core of the AT32AP7 family is attached to a Vector-Multiplication-Unit (Pixel Coprocessor) which may be used to scale or rotate images as well as for color conversion algorithm. The embedded LCD controller supports STN and TFT display up to 2048x2048 pixel resolution at 8 pixels per color. Several other media interfaces like Audio Codec's, Multimedia Card and high-speed USB device interfaces opens a wide range of applications needed in consumer, automotive and industrial areas.

Media			Timer						Analogue I/O						Oscillators			Supply		Miscelleanous					
MCI	Touch Screen Ctrl.	Keyboard Controller	16-bit Timers	PWM Controller	Intervall Timer	Watchdog Timer	RTT	RTC	10-bit ADC	10-bit DAC	I/O Pins	High-Current-Pads	Brown Out Detection	Power On Reset	RC Oscillator	Cryst.Oscillator/PLL	PGM Clock Out	Vcc Core [V]	Vcc I/O [V]	Process Technology	Package	Boot SW-Support	Evalution Kit MSC Bundle	Status Q1 2007	Pin Compatible with
y	-	PS2	6	4	-	-	-	y	-	-	160	-	-	y	-	2/2	5	1.65-1.95	3.0-3.6	0.18µ	CTBGA256	-	ATSTK1000 AT32AP7000-Startup Paket	P	-
y	-	PS2	6	4	-	-	-	y	-	-	90	-	-	y	-	2/2	5	1.65-1.95	3.0-3.6	0.18µ	QFP208	-		P	-
y	-	PS2	6	4	-	-	-	y	-	-	88	-	-	y	-	2/2	5	1.65-1.95	3.0-3.6	0.18µ	CTBGA196	-		P	-
y	ADC	y	6	-	y	y	-	y	6ch	-	189	-	-	y	-	3/3	5	1.08-1.32	3.0-3.6	0.13µ	BGA324	SAM-BA	TBD	I	-
-	-	-	3	7	-	y	-	y	y	-	69	-	y	y	y	2/2	4	1.65-1.95	3.0-3.6	0.13µ	LQFP144	Flip	ATEVK1100	S	AT32UC3A0xxx
-	-	-	3	7	-	y	-	y	y	-	69	-	y	y	y	2/2	4	1.65-1.95	3.0-3.6	0.13µ	LQFP144	Flip		S	
-	-	-	3	7	-	y	-	y	y	-	69	-	y	y	y	2/2	4	1.65-1.95	3.0-3.6	0.13µ	LQFP144	Flip		S	
-	-	-	3	7	-	y	-	y	y	-	109	-	y	y	y	2/2	4	1.65-1.95	3.0-3.6	0.13µ	LQFP100	Flip		S	AT32UC3A1xxx
-	-	-	3	7	-	y	-	y	y	-	109	-	y	y	y	2/2	4	1.65-1.95	3.0-3.6	0.13µ	LQFP100	Flip		S	
-	-	-	3	7	-	y	-	y	y	-	109	-	y	y	y	2/2	4	1.65-1.95	3.0-3.6	0.13µ	LQFP100	Flip		S	
-	-	-	3	7	-	-	-	-	y	-	44	4	y	y	y	2/2	4	1.65-1.95	3.0-3.6	0.13µ	TQFP64/QFN64	Flip	ATEVK1101	S	AT32UC3B0xxx
-	-	-	3	7	-	-	-	-	y	-	44	4	y	y	y	2/2	4	1.65-1.95	3.0-3.6	0.13µ	TQFP64/QFN64	Flip		S	
-	-	-	3	7	-	-	-	-	y	-	44	4	y	y	y	2/2	4	1.65-1.95	3.0-3.6	0.13µ	TQFP64/QFN64	Flip		S	
-	-	-	3	7	-	-	-	-	y	-	28	4	y	y	y	1/1	4	1.65-1.95	3.0-3.6	0.13µ	TQFP48/QFN48	Flip		S	AT32UC3B1xxx
-	-	-	3	7	-	-	-	-	y	-	28	4	y	y	y	1/1	4	1.65-1.95	3.0-3.6	0.13µ	TQFP48/QFN48	Flip		S	
-	-	-	3	7	-	-	-	-	y	-	28	4	y	y	y	1/1	4	1.65-1.95	3.0-3.6	0.13µ	TQFP48/QFN48	Flip		S	

AVR32 UC3A Series

Flash MCU with Extensive Communication Capabilities:

The UC3A Series offers modern communication interfaces like the 10/100-Mbps IEEE 802.3-compliant Ethernet MAC and full-speed USB 2.0 with on-the-go capability. Designing TCP/IP aware applications that integrate well in a PC environment becomes very easy. An additional SRAM/SDRAM external bus interface allows expansion by adding more memory or by interfacing with other peripherals such as LCD controllers, FPGA and any other memory mapped device.
The high performance AVR32 UC core, the memory system and on-chip peripherals are all connected to a 6-layer high speed system bus operating at 66 MHz and allow concurrent DMA transfer to each bus up to 264MBytes/s.
The excellent performance over operating frequency ratio allows delivering 80 DMIPS at 66 MHz. This is achieved with only 40mA at 3.3V

AVR32 UC3B Series

Low-Power Flash MCU with USB On-The-Go:

The AVR32 UC3B perfectly fits applications requiring high performance Flash MCU where space and/or power consumption is a concern. The AVR32 UC3B Series delivers 72 DMIPS at 60 MHz any only consumes 23mA at 3.3V.
The integrated full-speed USB 2.0 interface with on-the-go capabilities provides an easy way to interface with off-the-shelf ISB devices or with other embedded applications already designed to offer a USB device interface.
The advanced DSP capabilities and the USB interfaces also makes the UC3B series ideal as an MCU host companion to extend existing systems, with an interface to real-time sensors/actuators and to open up applications to USB device and host capabilities.

AVR32 Inside

Introducing the AVR32

Traditionally chip vendors have increased processing power by making processors run faster. This is a real issue for portable devices because tuning up the clock directly increases power consumption and reduces battery life. The approach taken by Atmel with the AVR32 is to increase the amount of processing the processor can do internally and actually turn the clock frequency down.

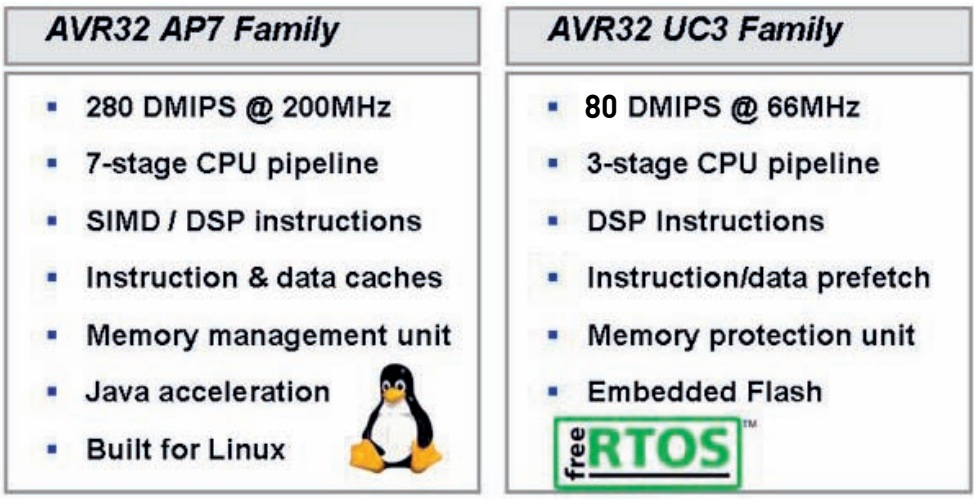
The AVR32 core architecture is optimized for highest data throughput. Most RISC architectures are wasting processor cycles for non productive operations like load, store or moving data, for branches, for loading data which are not in the cache or waiting until a multi cycle instruction is done. All those operations do not contribute to the execution of the application.

AVR32 AP Core Features

There are a lot of improvements which have been made to speed up the overall core performance. With the Accumulator-Cache a new and patent method was developed which multiplies and accumulates within one clock cycle, without using an additional port. The accumulator cache is used to store the value which has to be added.
The Pipeline also supports „Data Forwarding". All instructions that are completed will be forwarded to the beginning of the pipeline so they can be used for waiting instructions without needing additional cycles.
With SIMD instructions (Single Instruction/Multiple Data) the data throughput of certain DSP algorithm can be extremely accelerated.
The advantage of deep pipelines is clear higher frequencies, but also they may loose performance when a jump is performed and the pipeline has to be reloaded. Especially in cases where small nested loops have to be executed the efficiency of the pipeline is dramatically reduced. By memorizing the jump address the branch can be folded to zero cycle branching which is also known as „Predictable Branching".

One Architecture - Two Families

The first device was designed to be used in full-fledge OS like Linux. Linux supporting architectures require Memory Management Unit for virtual address support but do have disadvantages for real-time applications. Also instruction- and data-cache are not supporting predictable timing and response times. So Atmel decided to go two different ways: One is the AP7 (Application Processor) which is optimized for Linux and the other is UC3 (simple for µController) which was optimized for real-time OS. Both families will be expanded in future by new derivates.

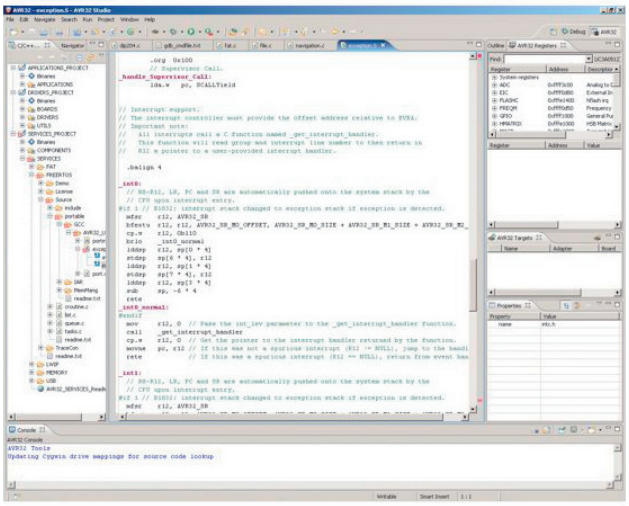


The UC3 family is also equipped with an extensive DSP instruction set providing high-speed signal processing by hardware. An optimized DSP software library is supported from Atmel and can be downloaded from the Web free of charge.

AVR32 Development Tools

AVR32® Studio

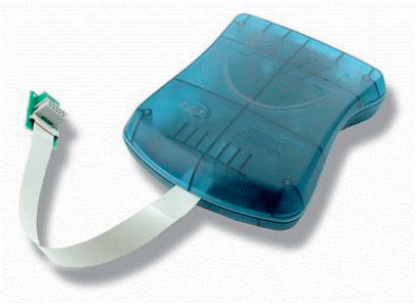
AVR32 Studio is a free Integrated Development Environment (IDE) for AVR32 that enables you to write, build, deploy and debug your C/C++ and assembler code. The AVR32 Studio integrates with the AVR32 GNU Tool chain including GCC for building applications for AVR32. AVR32 Studio is build on Eclipse™ and supports



- Integrated Development Environment (IDE)
- Source code editor with syntax highlighting
- Supports for writing and debugging Linux® applications
- Debugging views (I/O and system registers, CPU registers and memory)
- Disassemble view
- Target Control
- Online help including tutorials
- Edit and transfer MCU fuse settings
- Supports AT90JTAGICE-MK2 for JTAG programming and debugging

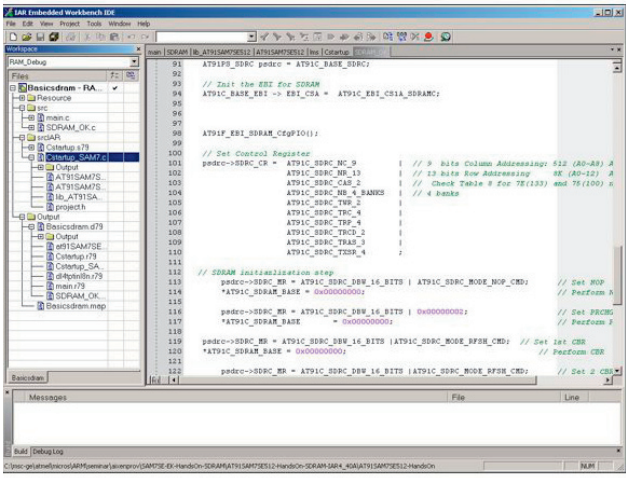
AT90JTAGICE-mk2

The AT90JTAGICE-MK2 is a very well established powerful development tool for on-chip debugging for all new AVR32 AP7 and UC3 devices as well as for all standard AVR's. This tool includes now the traditional JTAG interface with the same feature set as the JTAGICE and in addition the new debugWIRE™ interface. The link to your PC is realized either by RS232 or USB1.1 link. The emulator comes with the JTAG/debugWIRE™ box, a user manual, a RS232 cable and a USB cable.



IAR Embedded Workbench for AVR32

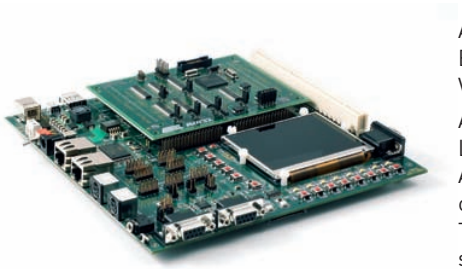
IAR Embedded Workbench provides a suite of AVR32 development tools for embedded systems. IAR Embedded Workbench for AVR32 offers a continuous workflow, efficient code generation and ease of use.



- Integrated development environment with project management tools and editor
- Highly optimizing AVR32 compiler supporting C and C++
- Configuration files for all AVR32 devices
- AVR32 JTAGICE-mkII debugger support
- Run-time libraries
- Relocating AVR32 assembler
- Linker and librarian tools
- C-SPY debugger with AVR32 simulator and support for RTOS-aware debugging on hardware
- Ready-made code and project examples for Atmel evaluation boards
- User and reference guides, both printed and in PDF format
- Context-sensitive online help

AVR32 Inside

ATSTK1000



ATSTK1000 provides a complete AT32AP7000 development environment. The kit has two Ethernet ports, a high quality VGA LCD, a loudspeaker, and connectors for USART, PS2, VGA and USB. A expansion header can be used for prototyping.

A pre-installed Linux image on the enclosed 256MB SD card ensures that the user can boot Linux and start program development directly after power up.
ATSTK1000 is also supported by AVR AT90JTAGICE-MK2. With either GNU GCC or the IAR compiler, the AT90JTAGICE-MK2 supports basic runtime control and limited trace.
The Vitra and Opella products from Ashling provide high-end debugging capabilities as e.g. sustained trace and SQA (software quality assurance).

ATNGW100

The NGW100 uses the AT32AP7000 which combines Atmel's state of the art AVR32 Digital Signal Processor CPU with an unrivalled selection of communication interfaces.

- The Network Gateway provides the following features:
- Two Ethernet connectors
- 32MB SDRAM
- 16MB on-board flash
- Expandable memory through SD or MMC memory cards
- USB connector
- JTAG connector for debugging or programming of flash
- Expansion connectors with 63 general purpose IO or peripheral modules from AP7000
- Power system and status LEDs
- Two user controllable LEDs
- Footprint for mictor-38 connector for NEXUS emulator

The NGW100 is also an ideal development board for the AT32AP7000. All resources are available, and it supports communication on any of the device's communication interfaces. The board is preloaded with Linux and shipped with I/O interface drivers that can be called from your own code.

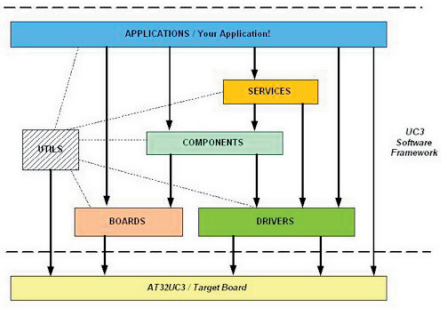
ATSTK600

The Atmel AVR STK600 evaluation board provides a complete programming and development system. All ATtiny, ATmega, Xmega and UC3 family devices are supported through different sockets and adapters available from Atmel.

- Bus connections and physical links for:
- Mini AB-USB connector
- CAN physical layer chip connected to pin header
- LIN physical layer
- RS-232 interface with level converter.

UC3 Framework

The AVR®32 AT32UC3 Software Framework consists of AVR®32 UC3 microcontroller drivers, software services & libraries, and demonstration applications. Each software module is provided with full source code, example of usage, rich html documentation and ready-to-use projects for the IAR EWAVR32 and GNU GCC compilers. Atmel recommends that you upgrade your software by visiting http://www.atmel.com/avr32 and download the latest versions.



The AVR®32 UC3 Software Framework is made of the following:

Drivers

- Software drivers for all on-chip resources
- Board definition files and utilities

Services

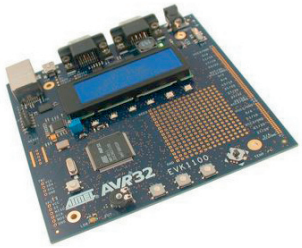
- Application specific pieces of code

Application

- Application examples using driver and services and support evalustion kits

ATEVK1100

The EVK1100 is an evaluation and development system for the AVR32 AT32UC3A microcontroller.



- Supports the AT32UC3A
- Ethernet port
- Sensors: Light, Temperature, Potentiometer
- 4x20 Blue LCD (PWM Adjustable backlight)
- Connectors for JTAG, Nexus, USAART, USB 2.0, TWI, SPI
- SD and MMC Card Reader

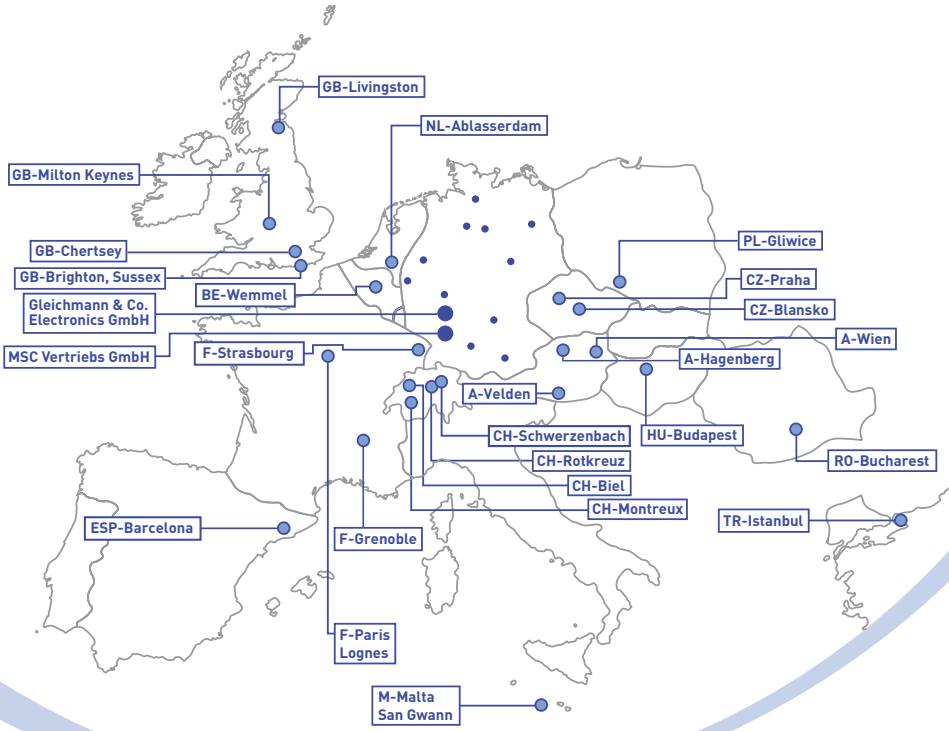
The EVK1100 evaluation board is pre-programmed with a Control Panel application. Its purpose is to automatically log local sensors and actuators data and events and make these available through the various connectivity channels supported by the AVR®32. The logs are accessible locally through USART or USB (Mass Storage class), and/or remotely through the Internet (Web server). The Control Panel is locally configurable through USART or USB (Mass Storage class) or remotely configurable through the Internet (Web server).

ATEVK1101

The EVK1101 is an evaluation and development system for the AVR32 AT32UC3B microcontroller

- Supports the AT32UC3B
- Connectors for JTAG, Nexus, USART, USB 2.0, TWI, SPI

The EVK1101 evaluation board is pre-programmed with demonstration software. Its purpose is to scan onboard sensors and actuators data and events (data acquisition through ADC channels) and make these available to a PC application (known as «AVR32 Control Panel») through a simple USB cable.



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