Unit: mm

TOSHIBA Photocoupler GaAlAs IRED + Photo IC

# **TLP351**

Inverter for Air Conditioner
IGBT/Power MOS FET Gate Drive
Industrial Inverter

The TOSHIBA TLP351 consists of a GaAlAs light emitting diode and a integrated photodetector.

This unit is 8-lead DIP package.

TLP351 is suitable for gate driving circuit of IGBT or power MOS FET. Especially TLP351 is capable of "direct" gate drive of lower Power IGBTs.

- Peak output current: ±0.6 A (max)
- Guaranteed performance over temperature: -40 to 100°C
- Supply current: 2 mA (max)
- Power supply voltage: 10 to 30 V
- Threshold input current : IF = 5 mA (max)
- Switching time (t<sub>pLH</sub>/t<sub>pHL</sub>): 700 ns (max)
- Common mode transient immunity: 10 kV/μs
- Isolation voltage: 3750 Vrms
- Option(D4)

VDE Approved: DIN EN60747-5-2

Maximum Operating Insulation Voltage :  $890V_{PK}$ Highest Permissible Over Voltage :  $4000V_{PK}$ 

(Note):When a EN60747-5-2 approved type is needed, Please designate "Option(D4)"

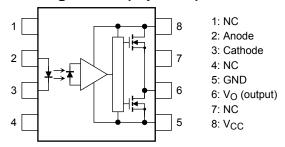
#### 8 7 6 5 9.66±0.25 1 2 3 4 9.66±0.25 9.66±0.25 9.66±0.25 9.60

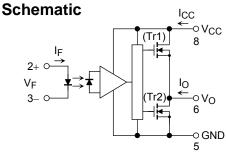
Weight: 0.54 g (typ.)

#### **Truth Table**

Input	LED	Tr1	Tr2	Output
Н	ON	ON	OFF	Н
L	OFF	OFF	ON	L

# Pin Configuration (top view)





A 0.1  $\mu$ F bypass capacitor must be connected between pin 8 and 5.

#### Absolute Maximum Ratings (Ta = 25°C)

	Characteristics	Symbol	Rating	Unit	
	Forward current	lF	20	mA	
	Forward current derating (Ta ≥ 85°C)		∆l <sub>F</sub> /∆Ta	-0.54	mA/°C
LED	Peak transient forward current	(Note 1)	IFP	1	Α
	Reverse voltage		V <sub>R</sub>	5	V
	Junction temperature		Tj	125	°C
	"H" peak output current	(Note 2)	I <sub>OPH</sub>	-0.6	Α
o	"L" peak output current	(Note 2)	I <sub>OPL</sub>	0.6	Α
Detector	Output voltage		VO	35	V
ă	Supply voltage		V <sub>CC</sub>	35	V
	Junction temperature		Tj	125	°C
Operating frequency (Note 3)		(Note 3)	f	25	kHz
Storage temperature range			T <sub>stg</sub>	-55 to 125	°C
Operating temperature range			T <sub>opr</sub>	-40 to 100	°C
Lead soldering temperature (10 s) (Note 4)			T <sub>sol</sub>	260	°C
Isolation voltage (AC, 1 minute, R.H. ≤ 60%) (Note 5)			BVS	3750	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width  $P_W \le 1 \mu s$ , 300 pps

Note 2: Exponential waveform pulse width  $P_W \le 10 \mu s$ ,  $f \le 15 kHz$ 

Note 3: Exponential waveform  $I_{OPH} \le -0.4 \text{ A} (\le 2.0 \text{ }\mu\text{s}), I_{OPL} \le +0.4 \text{ A} (\le 2.0 \text{ }\mu\text{s}), Ta = 100^{\circ}\text{C}$ 

Note 4: It is 2 mm or more from a lead root.

Note 5: Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

Note 6: A ceramic capacitor  $(0.1 \, \mu F)$  should be connected from pin 8 to pin 5 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property. The total lead length between capacitor and coupler should not exceed 1 cm.

#### **Recommended Operating Conditions**

Characteristics		Symbol	Min	Тур.	Max	Unit
Input current, ON	(Note 7)	I <sub>F (ON)</sub>	7.5		10	mA
Input voltage, OFF		V <sub>F (OFF)</sub>	0		0.8	V
Supply voltage		V <sub>CC</sub>	10		30	<b>V</b>
Peak output current		I <sub>OPH</sub> /I <sub>OPL</sub>	_	_	±0.2	Α
Operating temperature		T <sub>opr</sub>	-40	_	100	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Note 7: Input signal rise time (fall time)  $< 0.5 \mu s$ .

## Electrical Characteristics (Ta = -40 to 100°C, unless otherwise specified)

Characteristics		Symbol	Test Circuit	Test Co	ondition	Min	Тур.*	Max	Unit
Forward voltage		V <sub>F</sub>	_	I <sub>F</sub> = 5 mA, Ta = 25°C		_	1.55	1.70	V
Temperature coefficient of forward voltage		∆V <sub>F</sub> /∆Ta	_	I <sub>F</sub> = 5 mA		_	-2.0	_	mV/°C
Input reverse current		$I_{R}$	_	V <sub>R</sub> = 5 V, Ta = 25	V <sub>R</sub> = 5 V, Ta = 25°C		_	10	μΑ
Input capacitance		C <sub>T</sub>	_	V = 0, $f = 1$ MHz,	Ta = 25°C	_	45	_	pF
	"H" Level	I <sub>OPH1</sub>	1	V <sub>CC</sub> = 15 V	V <sub>8-6</sub> = 4 V	-0.2	-0.4	_	
Output current	II Level	I <sub>OPH2</sub>	$I_F = 5 \text{ mA}$	V <sub>8-6</sub> = 10 V	-0.4	-0.67	_	A	
(Note 8)	"L" Level	I <sub>OPL1</sub>	2	V <sub>CC</sub> = 15 V	V <sub>6-5</sub> = 2 V	0.2	0.35	_	
	L Level	I <sub>OPL2</sub>	_	$I_F = 0 \text{ mA}$	V <sub>6-5</sub> = 10 V	0.4	0.63	_	
	"H" Level	V <sub>OH</sub>	3	V <sub>CC</sub> = 10 V	$I_O = -100 \text{ mA},$ $I_F = 5 \text{ mA}$	6.0	8.5	_	
Output voltage	"L" Level	V <sub>OL</sub>	4		I <sub>O</sub> = 100 mA, V <sub>F</sub> = 0.8 V	_	0.4	1.0	
Cumply ourrant	"H" Level	Icch	5	V <sub>CC</sub> = 10 to 30 V	I <sub>F</sub> = 10 mA	_	1.4	2.0	
Supply current	"L" Level	ICCL	6	V <sub>O</sub> open	I <sub>F</sub> = 0 mA	_	1.3	2.0	mA
Threshold input current	$L \rightarrow H$	I <sub>FLH</sub>	_	V <sub>CC</sub> = 15 V, V <sub>O</sub> > 1 V		_	2.5	5	mA
Threshold input voltage	$H \rightarrow L$	V <sub>FHL</sub>	_	V <sub>CC</sub> = 15 V, V <sub>O</sub> < 1 V		0.8	_	_	V
Supply voltage		V <sub>CC</sub>	_	_	_	10		30	V

<sup>\*:</sup> All typical values are at Ta = 25°C

Note 8: Duration of I<sub>O</sub> time  $\leq$  50  $\mu$ s

Note 9: This product is more sensitive than the conventional product to static electricity (ESD) because of a lowest power consumption design.

General precaution to static electricity (ESD) is necessary for handling this component.

## **Isolation Characteristics (Ta = 25°C)**

Characteristic	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Capacitance input to output	CS	V = 0,f = 1MHz (Note5)	_	1.0	_	pF
Isolation resistance	R <sub>S</sub>	$V_S = 500 \text{ V}, \text{ Ta} = 25^{\circ}\text{C},$ R.H. $\leq 60\%$ (Note5)	1×10 <sup>12</sup>	10 <sup>14</sup>	_	Ω
		AC,1 minute	3750	_	_	V <sub>rms</sub>
Isolation voltage	$BV_S$	AC,1 second,in oil	_	10000	_	
		DC,1 minute,in oil	_	10000	_	Vdc

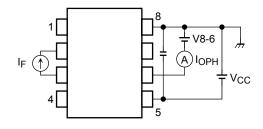
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# Switching Characteristics (Ta = -40 to $100^{\circ}$ C, unless otherwise specified)

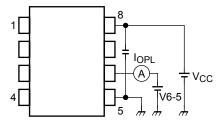
Characteristics		Symbol	Test Circuit	Test Condition		Min	Тур.*	Max	Unit
Propagation delay time	$L \rightarrow H$	t <sub>pLH</sub>		V <sub>CC</sub> = 30 V	$I_F = 0 \rightarrow 5 \text{ mA}$	100	_	700	ns
Tropagation delay time	$H \rightarrow L$	t <sub>pHL</sub>		$R_g = 47 \Omega$ $C_g = 3 \text{ nF}$	$I_F = 5 \rightarrow 0 \text{ mA}$	100	_	700	115
Propagation delay difference between any two parts or channels		PDD	7	$V_{CC} = 30 \text{ V}, R_g = 47 \Omega, C_g = 3 \text{ nF}$		-500		500	ns
		t <sub>pHL</sub> -t <sub>pLH</sub>		C <sub>g</sub> = 3 nF		200		000	110
Output rise time (10-90%)		t <sub>r</sub>		$V_{CC} = 30 \text{ V}$ $R_q = 47 \Omega$	$I_F = 0 \rightarrow 5 \text{ mA}$		50		ns
Output fall time (90-10%)		t <sub>f</sub>		$C_g = 3 \text{ nF}$	$I_F = 5 \rightarrow 0 \text{ mA}$	_	50	_	113
Common mode transient immunity at high level output		CM <sub>H</sub>	. 8	V <sub>CM</sub> = 1000 Vp-p Ta = 25°C	$I_F = 5 \text{ mA}$ $V_{O \text{ (min)}} = 26 \text{ V}$	-10000			\//us
Common mode transient immunity at low level output		CML	0	V <sub>CC</sub> = 30 V	I <sub>F</sub> = 0 mA V <sub>O (max)</sub> = 1 V	10000	_		- V/μs

<sup>\*:</sup> All typical values are at Ta = 25°C

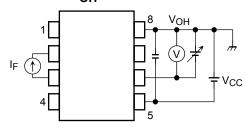
## Test Circuit 1: I<sub>OPH</sub>



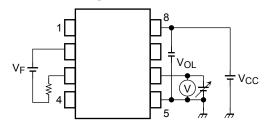
Test Circuit 2: I<sub>OPL</sub>



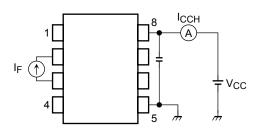
Test Circuit 3: V<sub>OH</sub>



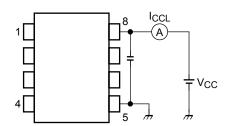
Test Circuit 4: V<sub>OL</sub>



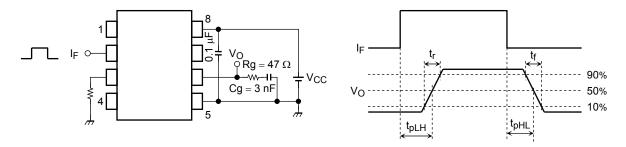
**Test Circuit 5: Icch** 



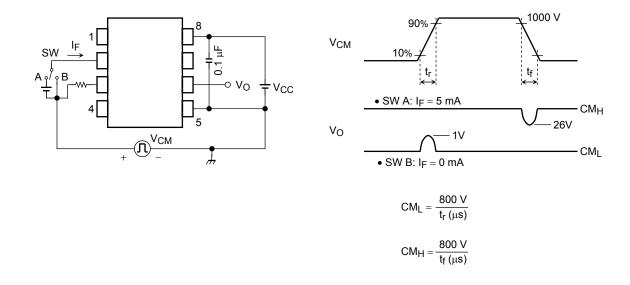
Test Circuit 6: I<sub>CCL</sub>



# Test Circuit 7: $t_{pLH}$ , $t_{pHL}$ , $t_{r}$ , $t_{f}$ , PDD

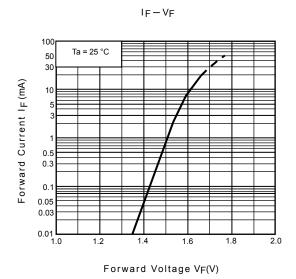


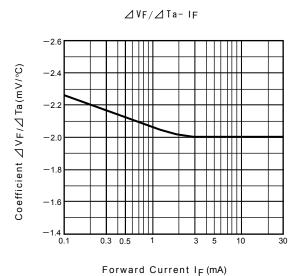
#### Test Circuit 8: CMH, CML

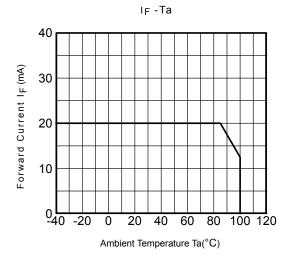


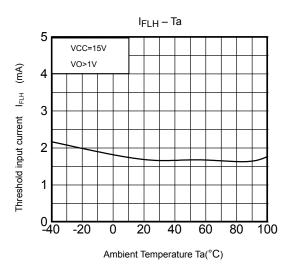
 $\mathrm{CM_L}\left(\mathrm{CM_H}\right)$  is the maximum rate of rise (fall) of the common mode voltage that can be sustained with the output voltage in the low (high) state.

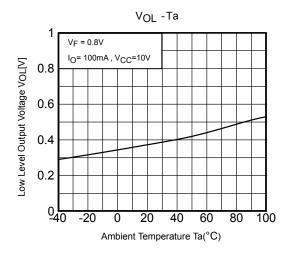
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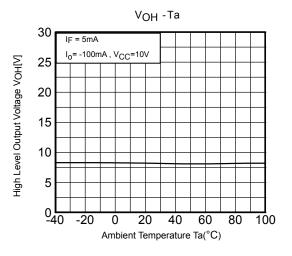




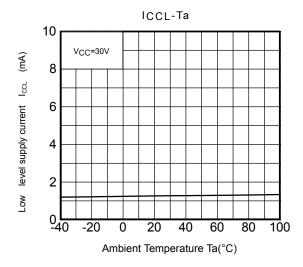


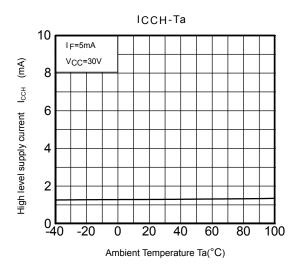


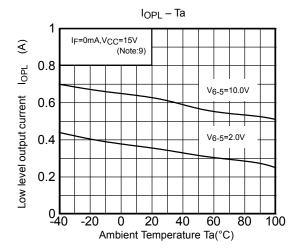


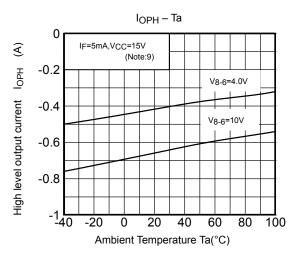


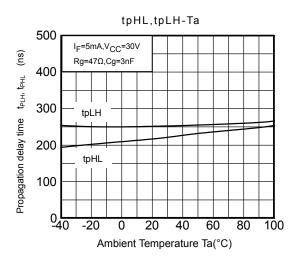
<sup>\*:</sup> The above graphs show typical characteristics.











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