National Semiconductor

April 2, 2008

LM139A/LM139QML
Low Power Low Offset Voltage Quad Comparators

General Description

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic— where the low power drain of the LM139/LM139A is a distinct advantage over standard comparators.

Features

- Available with Radiation Guarantee
  - — Total Ionizing Dose 100 krad(Si)
  - — ELDRS Free 100 krad(Si)
- Wide supply voltage range
- LM139/139A Series 2 to 36 V_{DC} or ±1 to ±18 V_{DC}
- Very low supply current drain (0.8 mA) — independent of supply voltage
- Low input biasing current: 25 nA
- Low input offset current: ±5 nA
- Offset voltage: ±1 mV
- Input common-mode voltage range includes GND
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage: 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

Advantages

- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

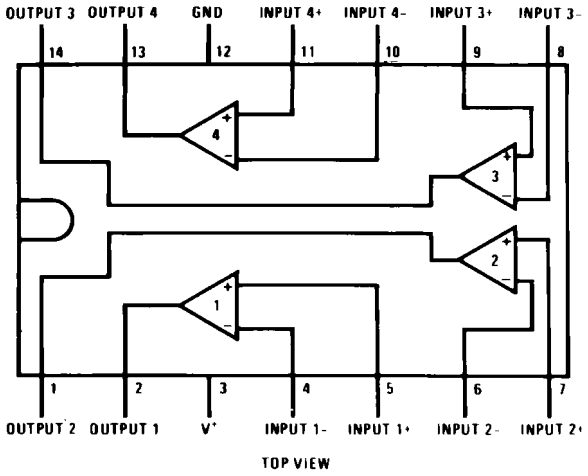
Ordering Information

NS Part Number	SMD Part Number	NS Package Number	Package Description
LM139E/883		E20A	20 terminal Leadless Chip Carrier
LM139J/883		J14A	14LD CERDIP
LM139W/883		W14B	14LD CERPACK
LM139WG/883		WG14A	14LD Ceramic SOIC
LM139AE-SMD	5962–87739012A	E20A	20 terminal Leadless Chip Carrier
LM139AJ-SMD	5962–8773901CA	J14A	14LD CERDIP
LM139AW-SMD	5962–8773901DA	W14B	14LD CERPACK
LM139AWG-SMD	5962–8773901XA	WG14A	14LD Ceramic SOIC
LM139AE/883		E20A	20 terminal Leadless Chip Carrier
LM139AJ-QMLV	5962–9673801VCA	J14A	14LD CERDIP
LM139AJ/883		J14A	14LD CERDIP
LM139AJLQMLV (Note 10)	5962L9673801VCA 50 krad(Si)	J14A	14LD CERDIP
LM139AJRQMLV (Note 10)	5962R9673801VCA 100 krad(Si)	J14A	14LD CERDIP

NS Part Number	SMD Part Number	NS Package Number	Package Description
LM139AJRLQMLV (Note 14) ELDRS Free	5962R9673802VCA 100 krad(Si)	J14A	14LD CERDIP
LM139AW-QMLV	5962–9673801VDA	W14B	14LD CERPACK
LM139AW/883		W14B	14LD CERPACK
LM139AWG-QMLV	5962–9673801VXA	WG14A	14LD Ceramic SOIC
LM139AWG/883		WG14A	14LD Ceramic SOIC
LM139AWGLQMLV (Note 10)	5962L9673801VXA 50 krad(Si)	WG14A	14LD Ceramic SOIC
LM139AWGRQMLV (Note 10)	5962R9673801VXA 100 krad(Si)	WG14A	14LD Ceramic SOIC
LM139AWGRLQMLV (Note 14) ELDRS Free	5962R9673802VXA 100 krad(Si)	WG14A	14LD Ceramic SOIC
LM139AWLQMLV (Note 10)	5962L9673801VDA 50 krad(Si)	W14B	14LD CERPACK
LM139AWRQMLV (Note 10)	5962R9673801VDA 100 krad(Si)	W14B	14LD CERPACK
LM139AWRLQMLV (Note 14) ELDRS Free	5962R9673802VDA 100 krad(Si)	W14B	14LD CERPACK

Connection Diagrams

Dual-In-Line Package



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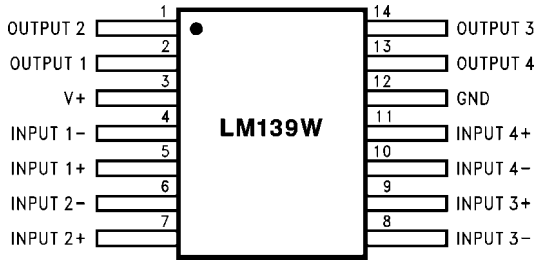
See NS Package NumberJ14A



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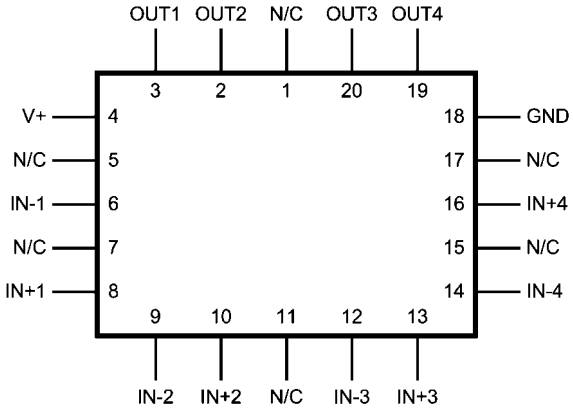
See NS Package Number W14B, WG14A



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See NS Package Number E20A

Absolute Maximum Ratings (Note 1)

	LM139 / LM139A
Supply Voltage, V^+	36 V_{DC} or ±18 V_{DC}
Differential Input Voltage (Note 7)	36 V_{DC}
Input Voltage	−0.3 V_{DC} to +36 V_{DC}
Input Current (V_{IN} < −0.3 V_{DC}) (Note 3)	50 mA
Power Dissipation (Notes 4, 13)	
LCC	1250 mW
CERDIP	1200 mW
CERPACK	680 mW
SOIC	680 mW
Sink Current (approx) (Note 11)	20mA
Output Short-Circuit to GND, (Note 2)	Continuous
Storage Temperature Range	−65°C ≤ T_A ≤ +150°C
Maximum Junction Temperature (T_J)	+150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Operating Temperature Range	−55°C ≤ T_A ≤ +125°C
Thermal Resistance	
θ_{JA}	
LCC (Still Air)	100°C/W
LCC (500LF / Min Air flow)	73°C/W
CERDIP (Still Air)	103°C/W
CERDIP (500LF / Min Air flow)	65°C/W
CERPACK (Still Air)	183°C/W
CERPACK (500LF / Min Air flow)	120°C/W
SOIC (Still Air)	183°C/W
SOIC (500LF / Min Air flow)	120°C/W
θ_{JC}	
LCC	28°C/W
CERDIP	23°C/W
CERPACK	23°C/W
SOIC	23°C/W
Package Weight (typical)	
LCC	470mg
CERDIP	2,190mg
CERPACK	460mg
SOIC	410mg
ESD rating (Note 12)	600V

Recommended Operating Conditions

Supply Voltage	5.0 V_{DC} to +30 V_{DC}
Ambient Operating Temperature Range	−55°C ≤ T_A ≤ +125°C

Quality Conformance Inspection

Mil-Std-883, Method 5005 — Group A

Subgroup	Description	Temp (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55

LM139 883 Electrical Characteristics

DC Parameters

The following conditions apply, unless otherwise specified. +V = 5V, V_{CM} = 0V

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{CC}	Supply Current	R_L = Infinity			2.0	mA	1, 2, 3
	Supply Current	+V = 30V, R_L = Infinity			2.0	mA	1, 2, 3
V_{IO}	Input Offset Voltage	+V = 30V		-5.0	5.0	mV	1
				-9.0	9.0	mV	2, 3
		+V = 30V, V_{CM} = 28.5V		-5.0	5.0	mV	1
		+V = 30V, V_{CM} = 28.0V		-9.0	9.0	mV	2, 3
				-5.0	5.0	mV	1
				-9.0	9.0	mV	2, 3
CMRR	Common Mode Rejection Ratio	+V = 30V, V_{CM} = 0V to 28.5V		60		dB	1
PSRR	Power Supply Rejection Ratio	+V = 5V to 30V		60		dB	1
± I_{Bias}	Input Bias Current	V_O = 1.5V	(Note 5)	-100	-1.0	nA	1
			(Note 5)	-300	-1.0	nA	2, 3
I_{IO}	Input Offset Current	V_O = 1.5V		-25	25	nA	1
				-100	100	nA	2, 3
I_{CEX}	Output Leakage Current	+V = 30V, V_O = 30V			1.0	µA	1, 2, 3
I_{Sink}	Output Sink Current	V_O = 1.5V		6.0		mA	1
V_{Sat}	Saturation Voltage	I_{Sink} = 4mA			400	mV	1
					700	mV	2, 3
A_V	Voltage Gain	+V = 15V, R_L ≥ 15ΩK, V_I = 1V to 11V		50		V/mV	1
V_{CM}	Common Mode Voltage Range	+V = 30V	(Note 8)	0	V+ - (1.5)	V	1
			(Note 8)	0	V+ - (2.0)	V	2, 3
V_{Diff}	Differential Input Voltage	+V = 30V, -V = 0V, $+V_I$ = 36V, $-V_I$ = 0V	(Note 9)		500	nA	1, 2, 3
		+V = 30V, -V = 0V, $+V_I$ = 0V, $-V_I$ = 36V	(Note 9)		500	nA	1, 2, 3

AC Parameters

The following conditions apply, unless otherwise specified. +V = 5V

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
t_{RLH}	Response Time	V_{OD} = 5mV			5.0	µS	9
		V_{OD} = 50mV			0.8	µS	9
t_{RHL}	Response Time	V_{OD} = 5mV			2.5	µS	9
		V_{OD} = 50mV			0.8	µS	9

LM139A SMD 5962–8773901 Electrical Characteristics

DC Parameters

The following conditions apply, unless otherwise specified. +V = 5V, V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{CC}	Supply Current	+V = 30V, R_L = Infinity			3.0	mA	1, 2, 3
		R_L = Infinity			3.0	mA	1, 2, 3
I_{CEX}	Output Leakage Current	+V = 30V, $-V_I$ = 0V, $+V_I \geq$ 1V, V_O = 30V			0.5	µA	1
					1.0	µA	2, 3
V_{Sat}	Saturation Voltage	$I_{Sink} \leq$ 4mA, $-V_I$ = 1V, $+V_I$ = 0V			400	mV	1
					700	mV	2, 3
I_{Sink}	Output Sink Current	$V_O \geq$ 1.5V, $-V_I$ = 1V, $+V_I$ = 0V		6.0		mA	1
V_{IO}	Input Offset Voltage	R_S = 0Ω		-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
		+V = 30V, R_S = 0Ω		-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
		+V = 30V, V_{CM} = 28V, V_O = 1.4V, R_S = 0Ω		-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
$\pm I_{IB}$	Input Bias Current	V_O = 1.5V	(Note 5)	-100	-1.0	nA	1
			(Note 5)	-300	-1.0	nA	2, 3
I_{IO}	Input Offset Current	V_O = 1.5V		-25	25	nA	1
				-100	100	nA	2, 3
PSRR	Power Supply Rejection Ratio	+V = 5V to 30V		70		dB	1, 2, 3
CMRR	Common Mode Rejection Ratio	+V = 30V, V_{CM} = 0V to 28V, $R_L \geq$ 15KΩ		70		dB	1, 2, 3
A_V	Voltage Gain	+V = 15V, $R_L \geq$ 15KΩ, V_O = 1V to 11V		50		V/mV	4
				25		V/mV	5, 6
V_{CM}	Common Mode Voltage Range	+V = 30V	(Note 8)	0	V+ - (2.0)	V	1, 2, 3
		+V = 5V	(Note 8)	0	V+ - (2.0)	V	1, 2, 3

AC Parameters

The following conditions apply, unless otherwise specified. +V = 5V

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
t_{RLH}	Response Time	V_{OD} = 5mV, R_L = 5.1KΩ			5.0	µS	9
t_{RHL}	Response Time	V_{OD} = 5mV, R_L = 5.1KΩ			2.5	µS	9

LM139A 883, QMLV & RH, SMD 5962–9673801 Electrical Characteristics

DC Parameters (Notes 10, 14)

The following conditions apply, unless otherwise specified. +V = 5V, V_{CM} = 0V

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{CC}	Supply Current	R_L = Infinity			2.0	mA	1, 2, 3
		+V = 30V, R_L = Infinity			2.0	mA	1, 2, 3
I_{CEX}	Output Leakage Current	+V = 30V, V_O = 30V			1.0	µA	1, 2, 3
V_{Sat}	Saturation Voltage	I_{Sink} = 4mA			400	mV	1
					700	mV	2, 3
I_{Sink}	Output Sink Current	V_O = 1.5V		6.0		mA	1
V_{IO}	Input Offset Voltage			-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
		+V = 30V		-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
		+V = 30V, V_{CM} = 28.5V, V_O = 1.5V		-2.0	2.0	mV	1
		+V = 30V, V_{CM} = 28.0V, V_O = 1.5V		-4.0	4.0	mV	2, 3
± I_{Bias}	Input Bias Current	V_O = 1.5V	(Note 5)	-100	-1.0	nA	1
			(Note 5)	-300	-1.0	nA	2, 3
I_{IO}	Input Offset Current	V_O = 1.5V		-25	25	nA	1
				-100	100	nA	2, 3
PSRR	Power Supply Rejection Ratio	+V = 5V to 30V		60		dB	1
CMRR	Common Mode Rejection Ratio	+V = 30V, V_{CM} = 0V to 28.5V		60		dB	1
A_V	Voltage Gain	+V = 15V, $R_L \geq 15K\Omega$, V_O = 1V to 11V		50		V/mV	1
V_{CM}	Common Mode Voltage Range	+V = 30V	(Notes 6, 8)	0	V^+ - (1.5)	V	1
			(Notes 6, 8)	0	V^+ - (2.0)	V	2, 3
V_{Diff}	Differential Input Voltage	+V = 30V, -V =0V, $+V_I$ = 36V, $-V_I$ = 0V	(Note 9)		500	nA	1, 2, 3
		+V = 30V, -V = 0V, $+V_I$ = 0V, $-V_I$ = 36V	(Note 9)		500	nA	1, 2, 3

AC Parameters (Notes 10, 14)

The following conditions apply, unless otherwise specified. +V = 5V

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
t_{RLH}	Response Time	V_{OD} = 5mV			5.0	µS	4
		V_{OD} = 50mV			0.8	µS	4
t_{RHL}	Response Time	V_{OD} = 5mV			2.5	µS	4
		V_{OD} = 50mV			0.8	µS	4

DC Parameters Delta Values

The following conditions apply, unless otherwise specified. +V = 5V, V_{CM} = 0V

Deltas required for S-Level, MLS (as specified on Internal Processing instructions (IPI)), and QMLV product at Group B, Subgroup 5.

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage			-1.0	1.0	mV	1
± I_{Bias}	Input Bias Current	V_O = 1.5V	(Note 5)	-15	15	nA	1
I_{IO}	Input Offset Current	V_O = 1.5V		-10	+10	nA	1

DC/AC Parameters 50K Post Rad Limits +25°C (Note 10)

The following conditions apply, unless otherwise specified.

DC: +V = 5V, V_{CM} = 0V

AC: +V = 5V

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	+V = 5V, V_{CM} = 0		-2.5	2.5	mV	1
		+V = 30V, V_{CM} = 0		-2.5	2.5	mV	1
		+V = 30V, V_{CM} = 28.5V, V_O = 1.5V		-2.5	2.5	mV	1
± I_{Bias}	Input Bias Current	V_O = 1.5V	(Note 5)	-110	-1.0	nA	1
t_{RLH}	Response Time	V_{OD} (Overdrive) = 50mV			0.9	µS	4

DC/AC Parameters 100K Post Rad Limits +25°C (Notes 10, 14)

The following conditions apply, unless otherwise specified.

DC: +V = 5V, V_{CM} = 0V

AC: +V = 5V

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	+V = 5V, V_{CM} = 0		-4.0	4.0	mV	1
		+V = 30V, V_{CM} = 0		-4.0	4.0	mV	1
		+V = 30V, V_{CM} = 28.5V, V_O = 1.5V		-4.0	4.0	mV	1
± I_{Bias}	Input Bias Current	V_O = 1.5V	(Note 5)	-110	-1.0	nA	1
t_{RLH}	Response Time	V_{OD} (Overdrive) = 50mV			1.0	µS	4

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guaranteed specific performance limits. For guaranteed specifications and test conditions, see, the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3\ V_{DC}$ (at 25°)C.

Note 4: The low bias dissipation and the ON-OFF characteristics of the outputs keeps the chip dissipation very small ($P_D \leq 100mW$), provided the output transistors are allowed to saturate.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ -1.5V$ for Subgroup 1, or $V^+ -2.0V$ for Subgroup 2 & 3. Either or both inputs can go to $+30\ V_{DC}$ without damage, independent of the magnitude of V^+.

Note 7: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3\ V_{DC}$ (or $0.3\ V_{DC}$below the magnitude of the negative power supply, if used) (at 25°C).

Note 8: Parameter guaranteed by V_{IO} tests

Note 9: The value for V_{Diff} is not data logged during Read and Record.

Note 10: Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the “Post Radiation Limits” table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in Mil-Std-883, Method 1019, Condition A.

Note 11: SMD 5962–8773901 only

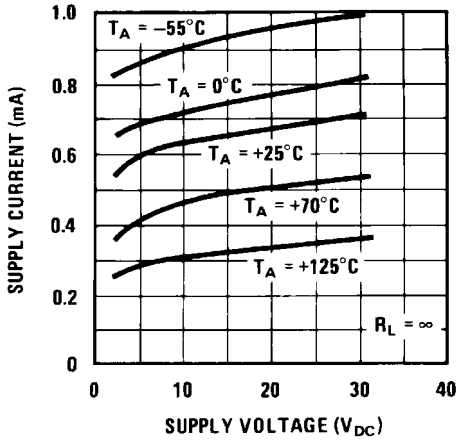
Note 12: Human Body model, 1.5 KΩ in series with 100 pF

Note 13: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (Package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} — T_A) / \theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 14: Low dose rate testing has been performed on a wafer-by-wafer basis, per test method 1019, condition D, MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS) effect. Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics, except as listed in the “Post Radiation Limits” table. Radiation end point limits for the noted parameters are guaranteed for only the conditions as specified in MIL-STD-883, Method 1019, condition D.

Typical Performance Characteristics LM139, LM139A

Supply Current



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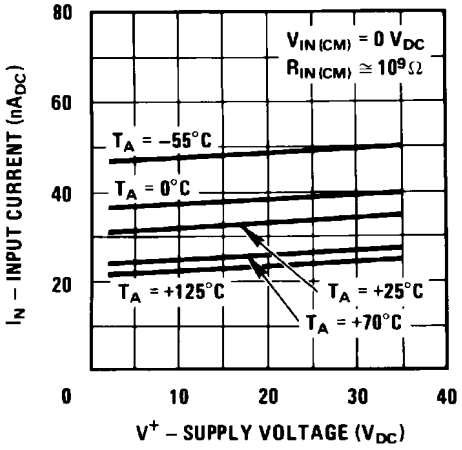
Input Current



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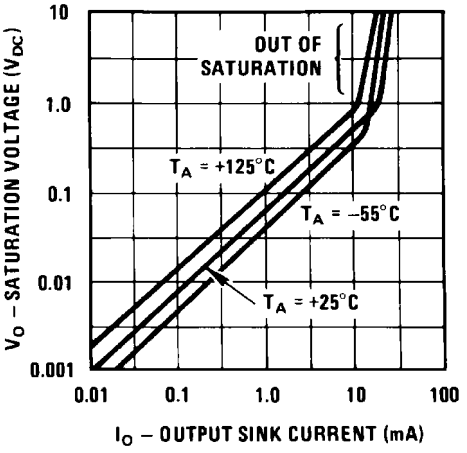
Output Saturation Voltage



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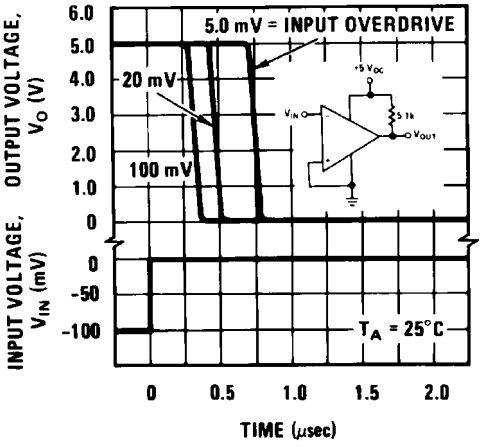
Response Time for Various Input Overdrives —Negative Transition



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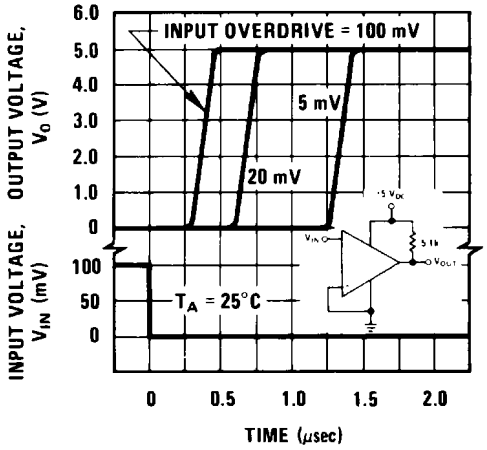
Response Time for Various Input Overdrives —Positive Transition



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Application Hints

The LM139 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing this input resistors to < 10 kΩ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be tied to the negative supply.

The bias network of the LM139 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2 V_{DC} to 30 V_{DC}.

It is usually unnecessary to use a bypass capacitor across the power supply line.

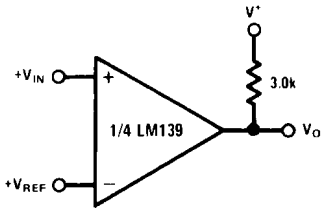
The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than –0.3 V_{DC} (at 25°C). An input clamp diode can be used as shown in the applications section.

The output of the LM139 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM139A package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω R_{SAT} of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp essentially to ground level for small load currents.

Typical Applications

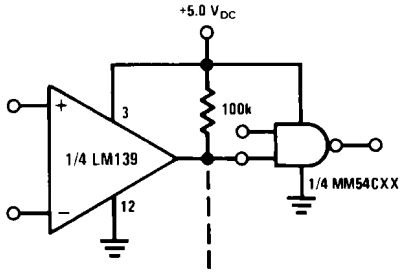
(V^+ = 5.0 V_{DC})

Basic Comparator



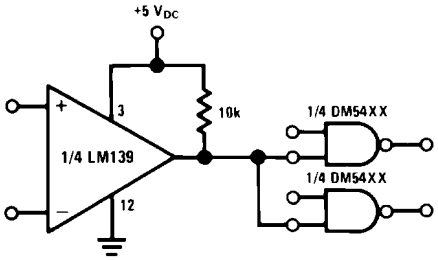
20122103

Driving CMOS



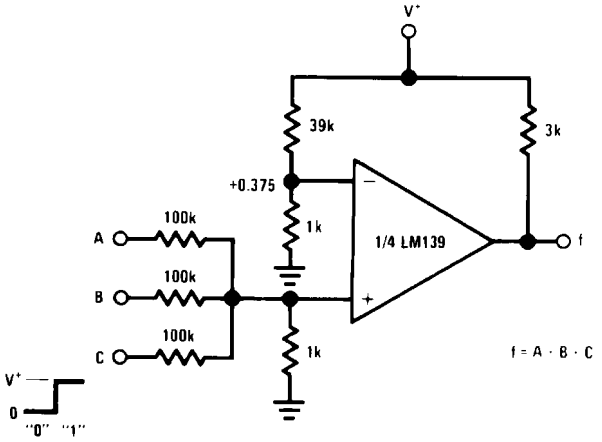
20122104

Driving TTL



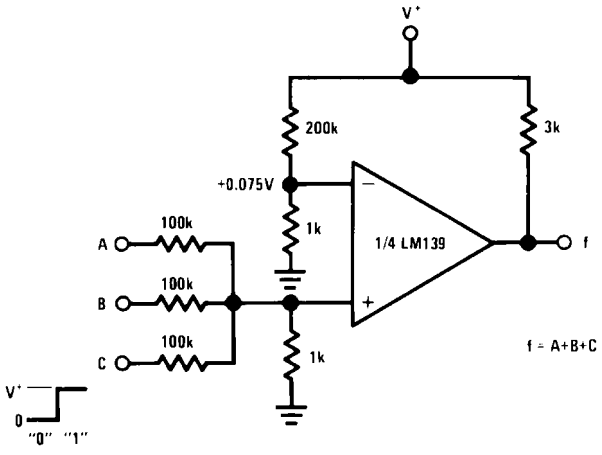
20122105

AND Gate



20122108

OR Gate

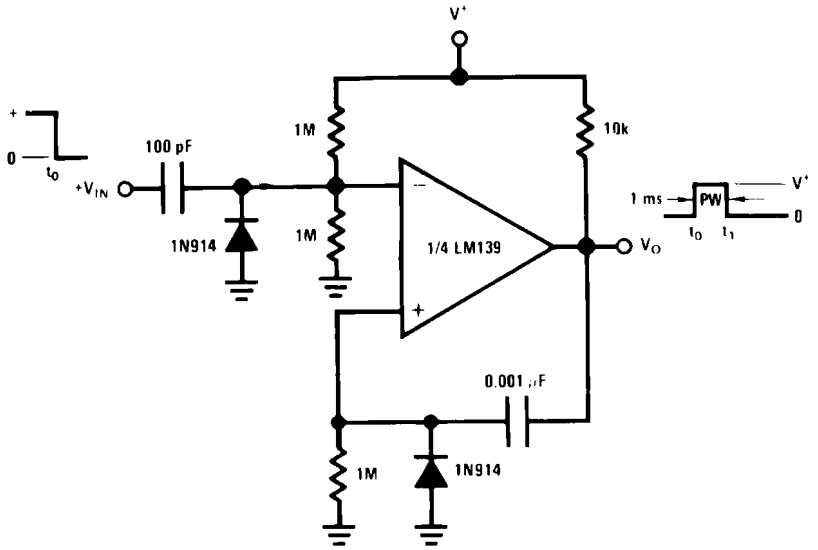


20122109

Typical Applications

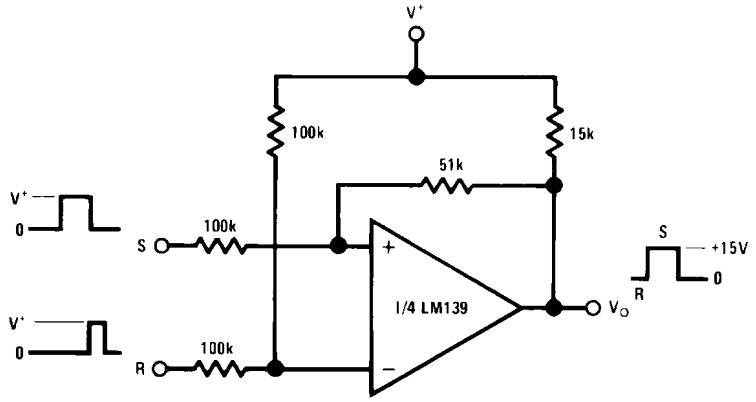
(V^+= 15 V_{DC})

One-Shot Multivibrator



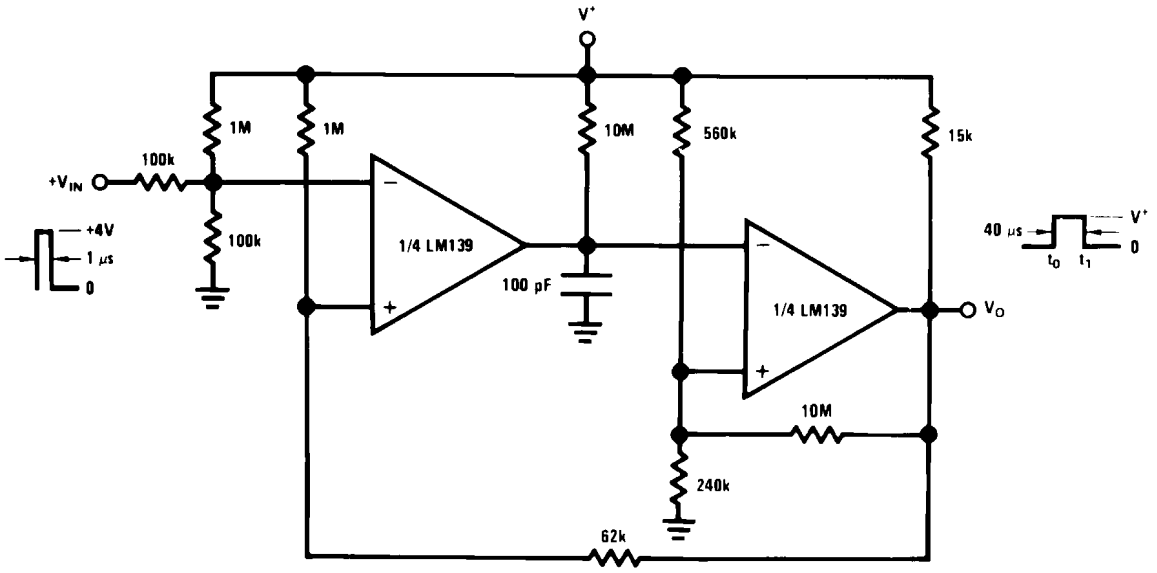
20122110

Bi-Stable Multivibrator



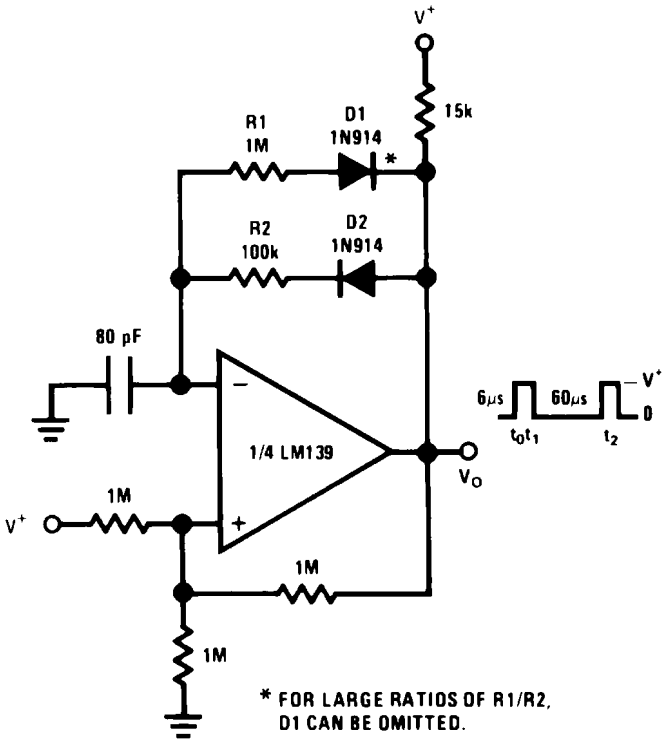
20122111

One-Shot Multivibrator with Input Lock Out



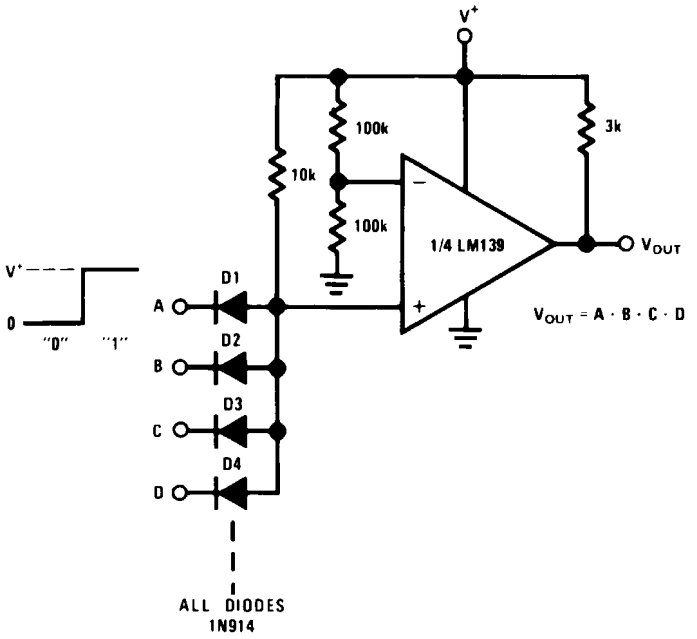
20122112

Pulse Generator



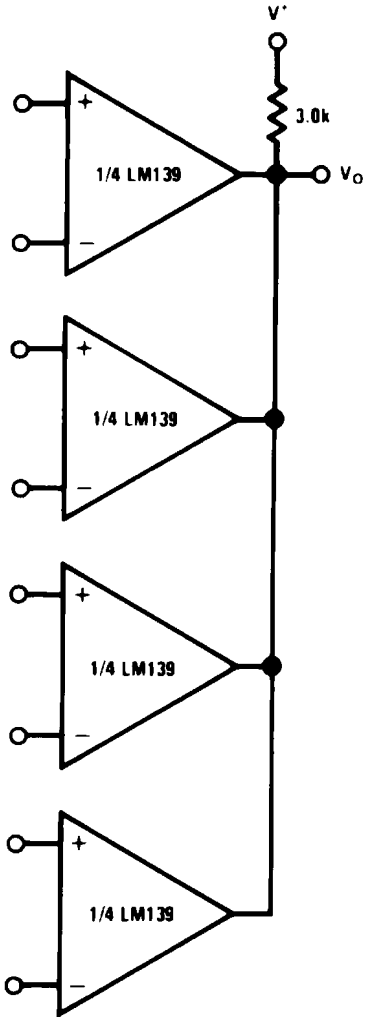
20122117

Large Fan-In AND Gate



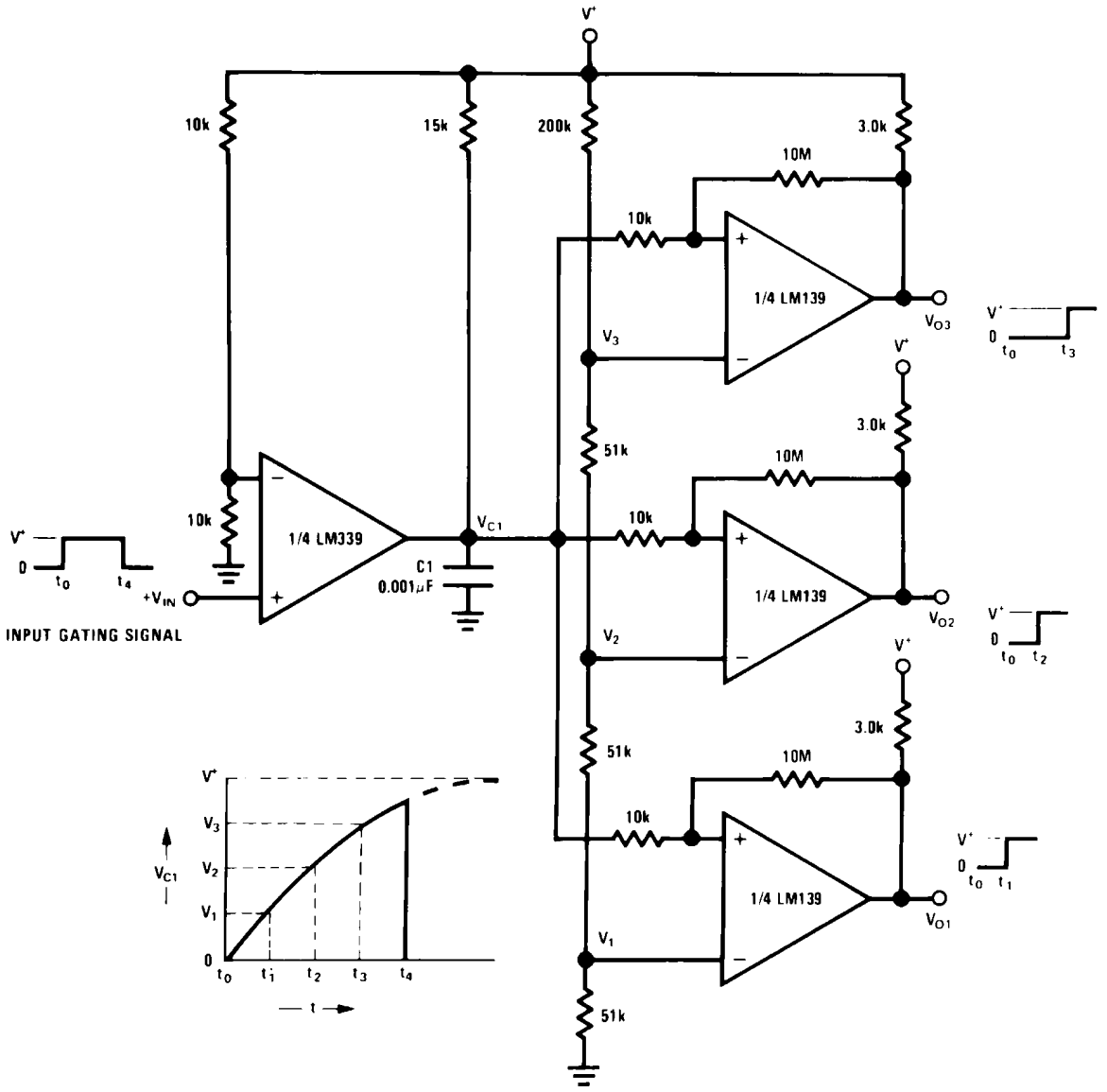
20122113

ORing the Outputs



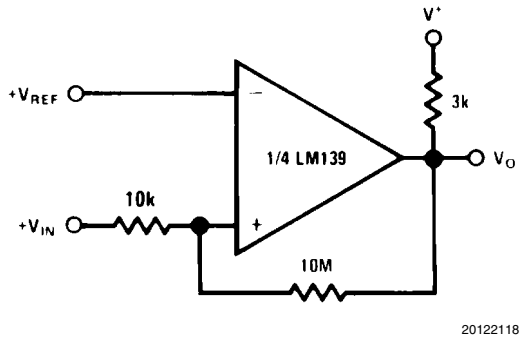
20122115

Time Delay Generator



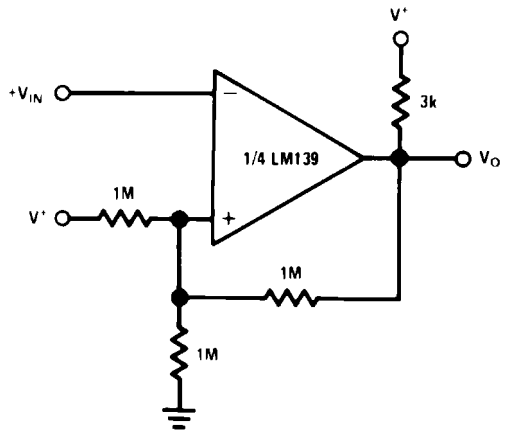
20122114

Non-Inverting Comparator with Hysteresis



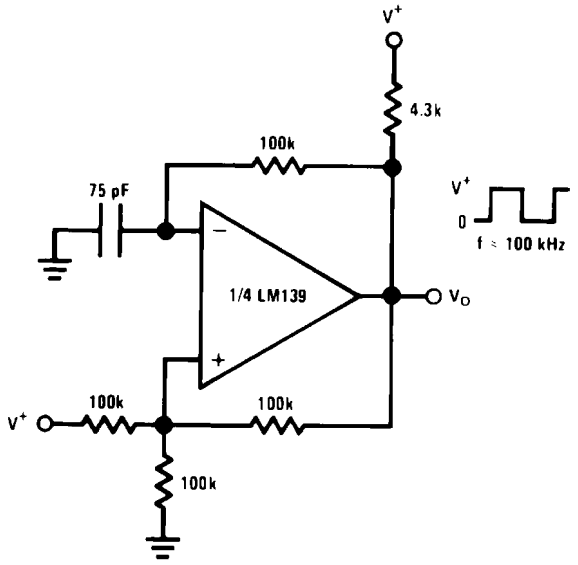
20122118

Inverting Comparator with Hysteresis



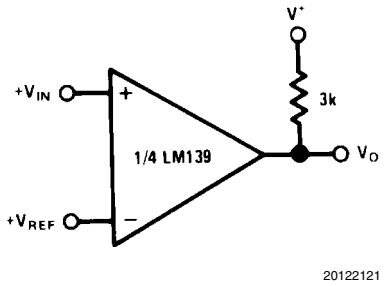
20122119

Squarewave Oscillator



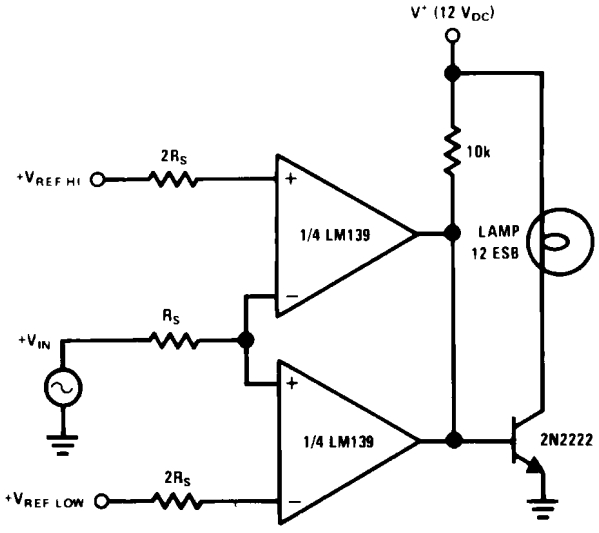
20122116

Basic Comparator



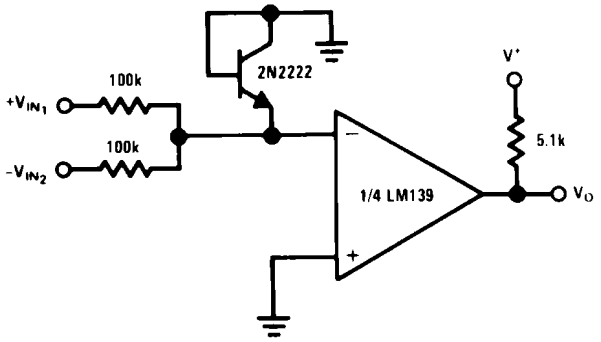
20122121

Limit Comparator



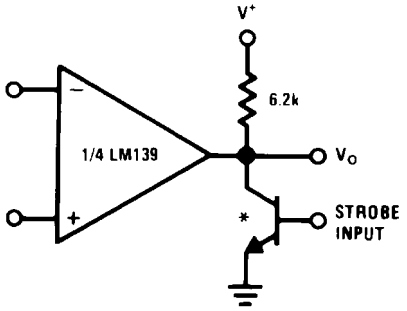
20122124

Comparing Input Voltages of Opposite Polarity



20122120

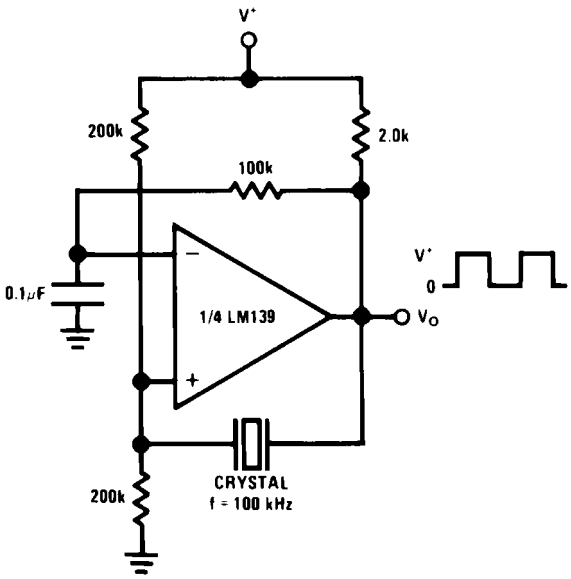
Output Strobing



20122122

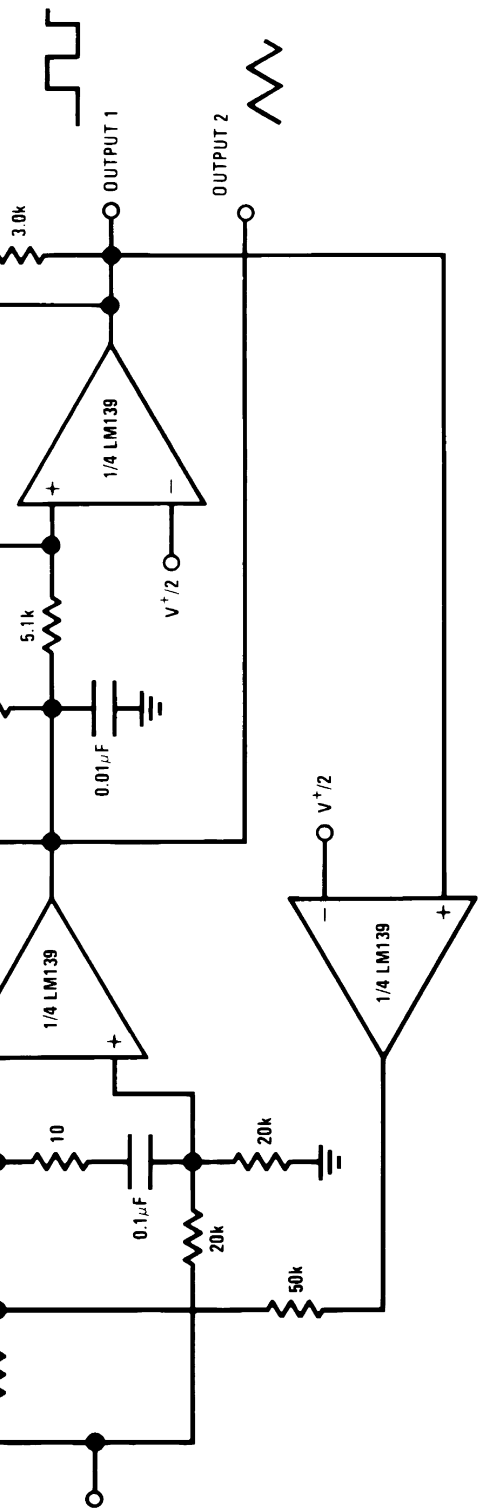
* Or open-collector logic gate without pull-up resistor

Crystal Controlled Oscillator



20122125

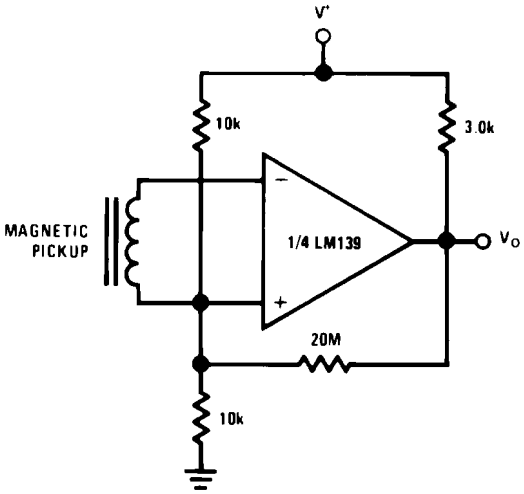
Two-Decade High-Frequency VCO



20122123

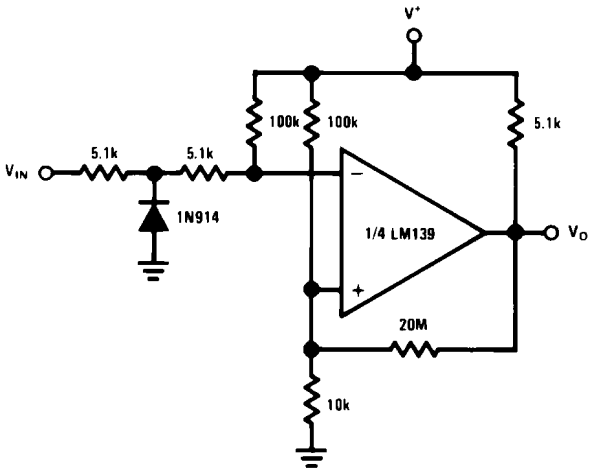
V+ = +30 V_{DC}
250 $mV_{DC} \leq V_C \leq +50\ V_{DC}$
700 Hz $\leq f_O \leq$ 100 kHz

Transducer Amplifier



20122128

Zero Crossing Detector (Single Power Supply)

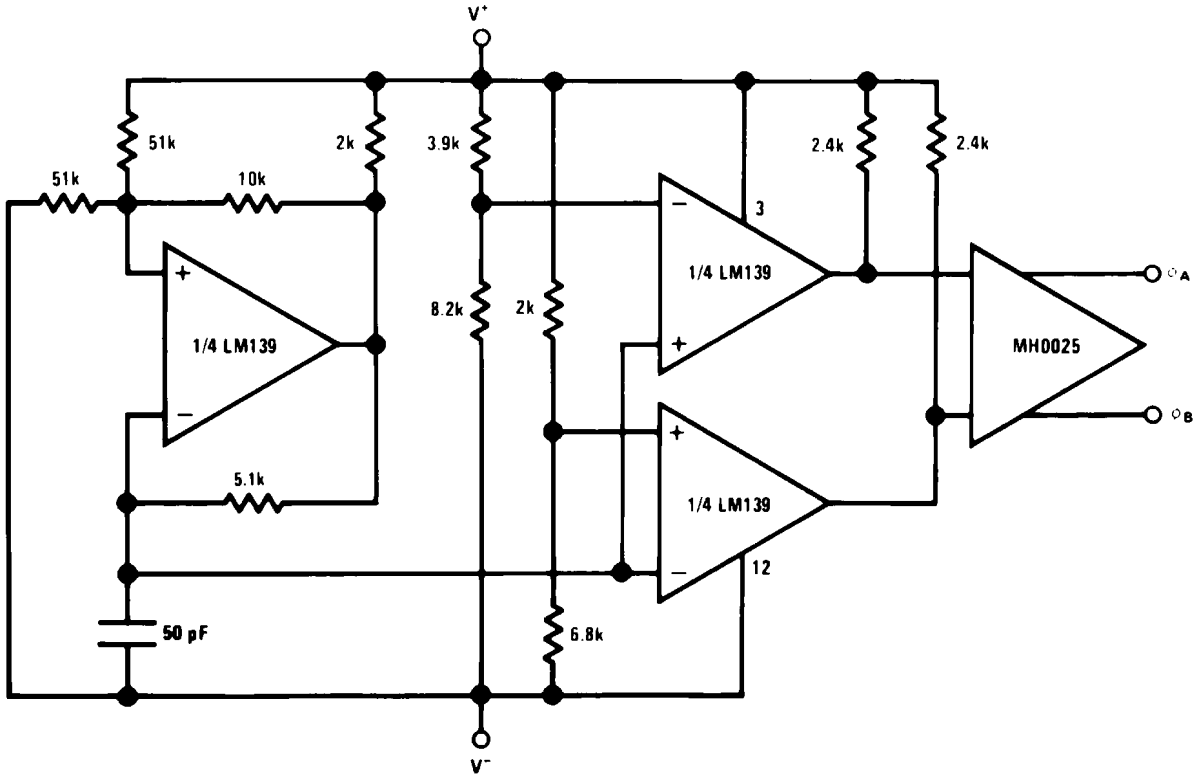


20122130

Split-Supply Applications

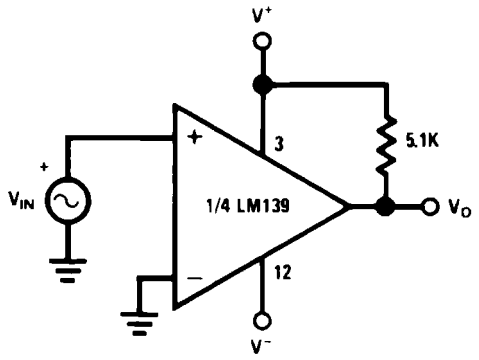
(V^+ = +15 V_{DC} and V^- = −15 V_{DC})

MOS Clock Driver



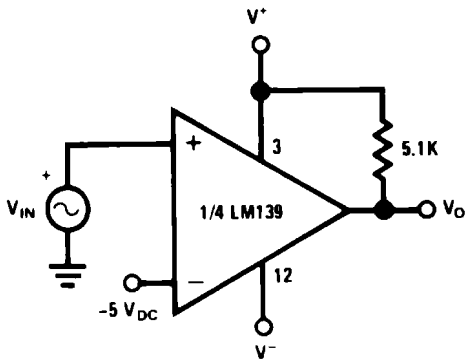
20122131

Zero Crossing Detector



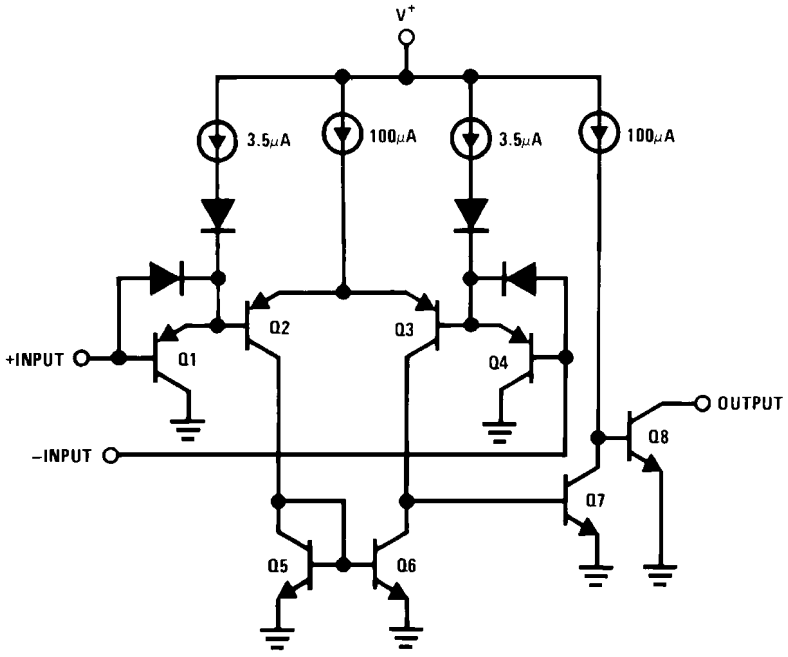
20122132

Comparator With a Negative Reference



20122133

Schematic Diagram

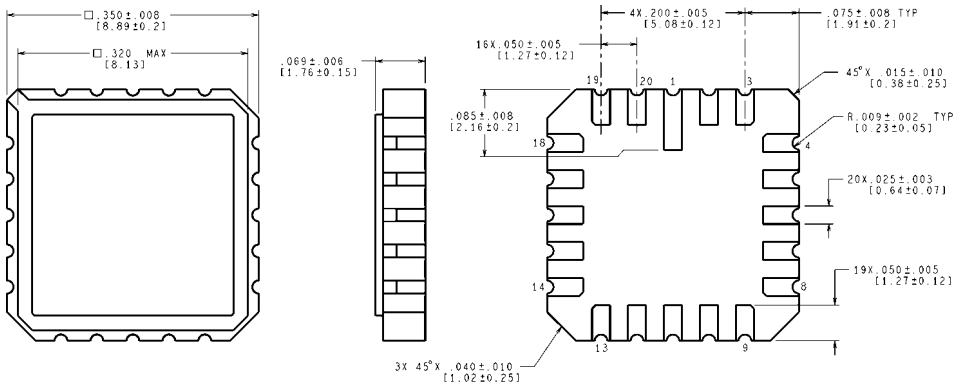


20122101

Revision History

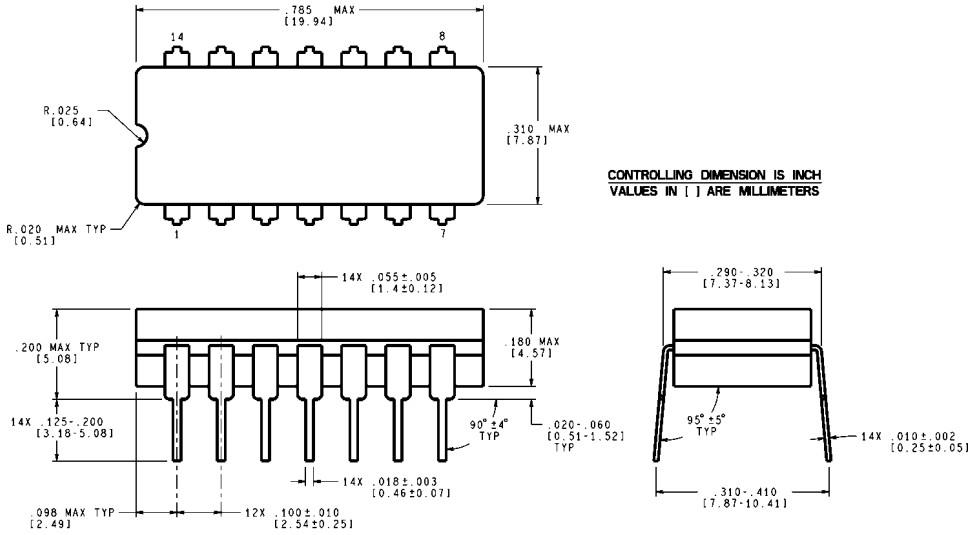
Date Released	Revision	Section	Originator	Changes
02/08/05	A	New Release to corporate format	L. Lytle	3 MDS datasheets converted into one Corp. datasheet format. MNLM139A-X-RH rev 4B0, MDLM139A-X rev 0C1, MNLM139–X rev 1A1. MDS datasheets will be archived.
06/28/06	B	Features, Ordering Information Table, Rad Hard Electrical Section and Notes	R. Malone	Added Available with Radiation Guarantee, Low Dose NSID's to table 5962R9673802VCA LM139AJRLQMLV, 5962R9673802VDA LM139AWRLQMLV, 5962R9673802VXA LM139AWGRLQMLV, and reference to Note 11 and 16. Note 16 to Rad Hard Electrical Heading. Note 16 to Notes. Archive Revision A.
02/13/08	C	Features, Ordering Table, LM139A 883, QMLV & RH, SMD 5962–9673801 Electrical Characteristics, Notes	Larry McGee	Added TID & Eldrs reference, Note 11 - Condition A. Changed VCM parameter - pg 8, Title from Drift Values to Delta Values - pg 9 & Note 16. Revision B will be Archive .

Physical Dimensions inches (millimeters) unless otherwise noted



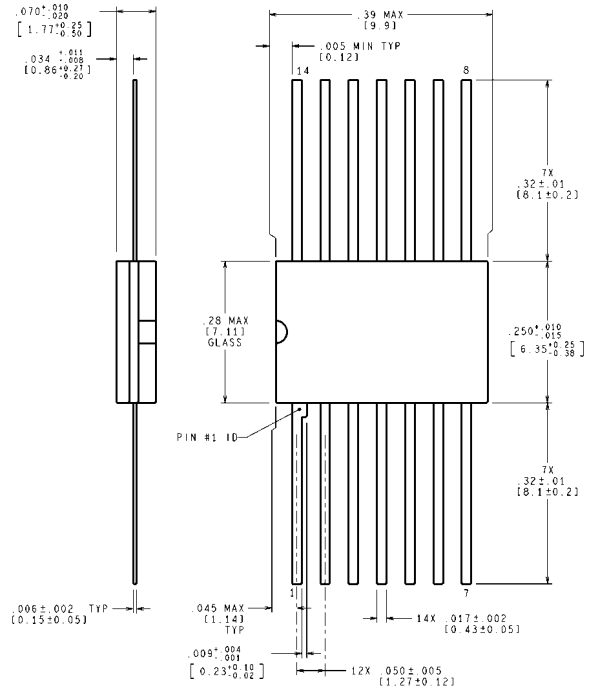
E20A (Rev F)

Leadless Chip Carrier (E))
NS Package Number E20A



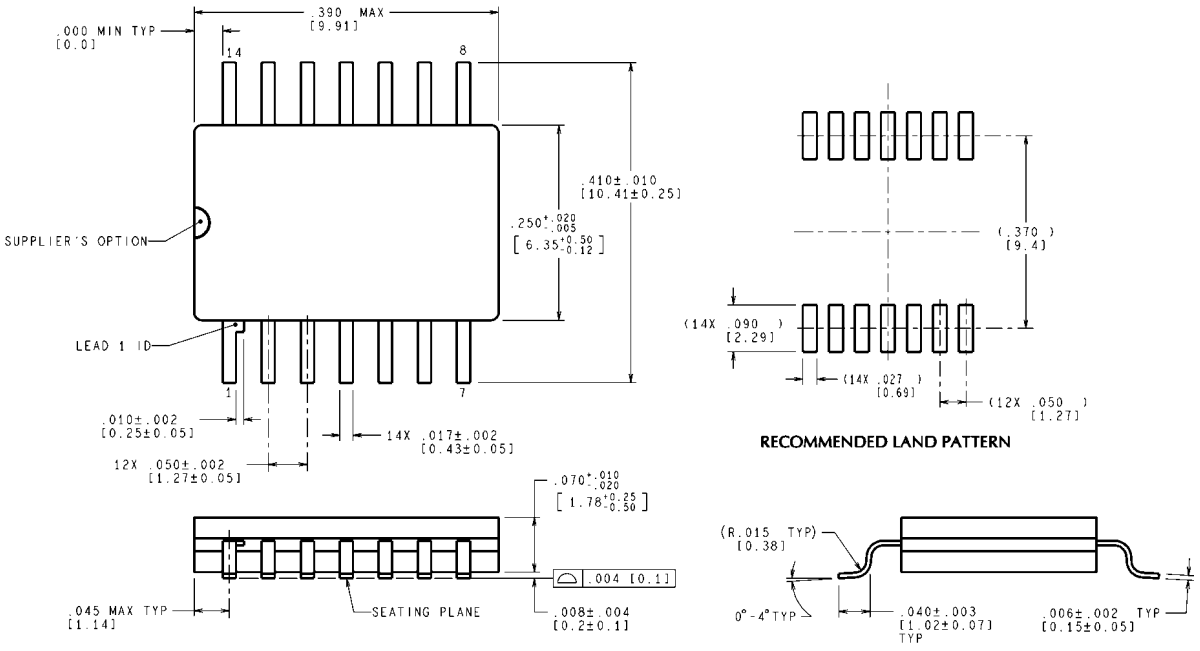
J14A (Rev J)

Ceramic Dual-In-Line Package (J)
NS Package Number J14A



W14B (Rev P)

Ceramic Flat Package (W)
NS Package Number W14B



WG14A (Rev D)

Ceramic SOIC (WG)
NS Package Number WG14A

Notes

Notes

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