S1D13774 WVGA LCD Controller

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The S1D13774 is a low cost, low power LCD Controller providing multiple LCD support for embedded and mobile products requiring up to WVGA resolution. The Video Input interface and optional TV-Out support, via an external NTSC/PAL encoder, enhance the capabilities of the S1D13774 to meet a wide variety of applications. Supporting up to three display layers, the S1D13774 provides the Host processor with flexibility in handling multiple image sources.

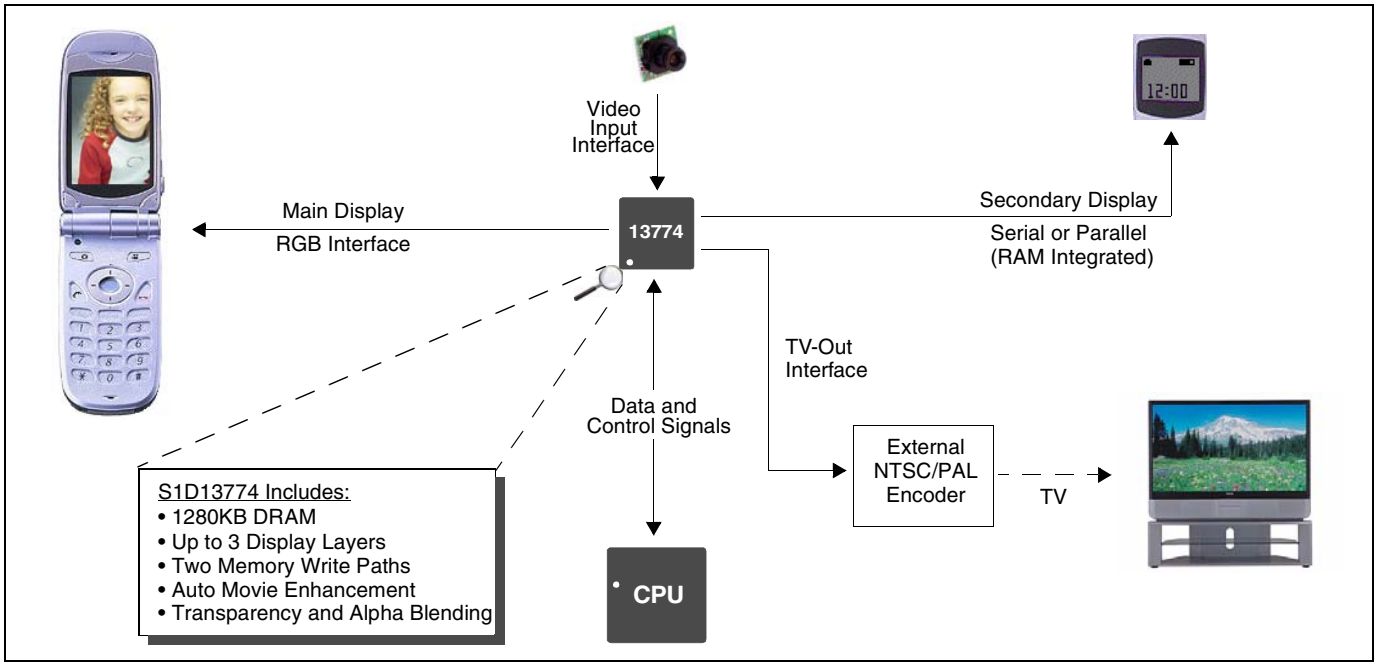
The S1D13774 feature set includes independent resizing of PIP window image data using the bi-cubic scaler, rotation and mirror functions, alpha blending and transparency, image scrolling for each layer, and LCD output manipulation such as gamma control and optional dithering. The Auto Movie Enhancement (AME) feature allows independent chroma, contrast, and gamma adjustments of the image data in a selected PIP window. The combination of these features allows the Host processor to provide image data, but off-loads the image processing requirements from the Host.

The S1D13774 contains 1280K bytes of embedded DRAM which is used to store image data for up to three layers. This feature set provides a low cost, low power single chip solution to meet the demands of embedded markets requiring up to WVGA resolution, such as Mobile Communications devices.

FEATURES

- Embedded 1280K byte DRAM
- MDDI, 18-bit Indirect, or I2C Host Interface
- Supports up to 2 LCD panels (LCD2 must be RAM integrated)
- Support for RGB, Serial, and Parallel I/F panels
- TV-Out support via an external NTSC/PAL encoder
- Video Input Interface
- Support for up to 3 display layers with overlay and alpha blending
  - Main Layer image can be doubled in size
  - PIP1 Layer can be resized from 8x to 1/2x
  - PIP2 Layer can be resized from 8x to 1/2x
- Software Initiated Power Save Mode
- VFBGA 161-pin or PFBGA 181-pin package

SYSTEM BLOCK DIAGRAM



■ DESCRIPTION

Memory

- 1280K bytes of embedded DRAM
- Main and Sub Write Paths:
  - Main Write Path features 90/180/270° Rotation, Mirror, eIC, and double-buffering functions
  - eco Image Codec (eIC) can store 2 WVGA images (480x800@24bpp) within 1280K bytes of memory
  - Sub Write Path supports double-buffering function

CPU Interface

- MDDI Client Type 1 (up to 400Mbps) and I2C Slave
- 18-bit Indirect Host and I2C Slave

Display Support

- Supports up to two panels:
  - LCD1: 18/24-bit RGB interface panel
  - LCD2:
    8/16/18/24-bit Parallel interface (RAM Integrated)
    8/16-bit Serial interface (RAM Integrated)
- TV-Out support using and external NTSC/PAL encoder
  - HSYNC & Field Interface (Interlaced)
  - ITU-R BT656 Interface (Interlaced)
  - Parallel (MPU) Interface (Non-Interlaced)
- Simultaneous output to LCD1 and TV-Out Interface is possible (Main to LCD1, PIP1/PIP2 to TV-Out)

Input Formats

- Host can input image data as:
  - YUV 4:2:2 or YUV 4:2:0
  - RGB 5:6:5, RGB 6:6:6, or RGB 8:8:8

Video Input Interface

- 8-bit YUV or 12-bit RGB Interface
- MVI3-RX (360Mbps/ch x 2 ch) (PFBGA 181-pin only)

Display Features

- Supports up to 3 layers with Overlay and Alpha Blending:
  - Main Layer features:
    - Image can be stored as RGB format
    - Pixel Doubling which doubles the size of the display image (independent horizontal/vertical)
  - PIP1 Layer features:
    - Image can be stored as RGB or YUV format
    - Bi-Cubic Scaler can resize image from 1/2x ~ 8x
    - Edge Enhancement support
  - PIP2 Layer features:
    - Image can be stored as RGB or YUV format
    - Bi-Cubic Scaler can resize image from 1/2x ~ 8x
    - Panorama function allows variable horizontal or vertical scaling
    - Edge Enhancement support
- Auto Movie Enhancement (AME) allows independent chroma, contrast, and gamma adjustments
- Image Scrolling for each Layer (Main, PIP1, PIP2)
- LUT (Look-Up Table) for gamma control of the LCD output
- Optional dithering for the LCD output

Miscellaneous

- Internal PLL or digital clock input (CLKI)
- Software initiated power save mode
- Available General Purpose IO pins
- Voltages:
  - CORE 1.5 volts
  - DRAM 1.5 volts and 2.5 volts
  - IO 1.80 volts or 2.50 volts
- Package:
  - VFBGA 161-pin (no MVI3), 7mm x 7mm x 1mm (S1D13774B01B)
  - VFBGA 161-pin (no MVI3 no MDDI), 7mm x 7mm x 1mm (S1D13774B02B)
  - PFBGA 181-pin (stacked MVI3), 8mm x 8mm x 1.2mm (S1D13774A00B)

CONTACT YOUR SALES REPRESENTATIVE FOR THESE COMPREHENSIVE DESIGN TOOLS

- S1D13774 Technical Documentation
- CPU Independent Software Utilities
- S1D13774 Evaluation Boards
- Royalty Free source level driver code

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