

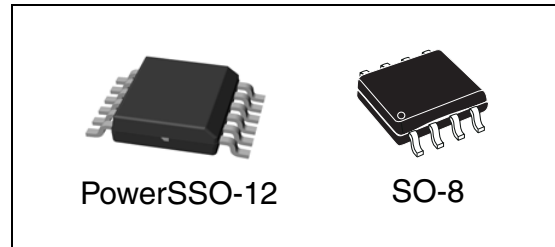
## 5 V low dropout voltage regulator

### Features

Max DC supply voltage	$V_S$	40 V
Max output voltage tolerance	$\Delta V_o$	+/-2%
Max dropout voltage	$V_{dp}$	500 mV
Output current	$I_o$	150 mA
Quiescent current	$I_{qn}$	55 $\mu A^{(1)}$

1. Typical value

- Operating DC supply voltage range 5.6 V to 40 V
- Low dropout voltage
- Low quiescent current consumption
- Precision output voltage 5 V +/- 2%
- Reset circuit sensing the output voltage
- Programmable reset pulse delay with external capacitor
- Adjustable reset threshold
- Early warning
- Very wide stability range with low value output capacitor
- Thermal shutdown and short-circuit protection
- Wide temperature range ( $T_j = -40\text{ }^\circ\text{C}$  to  $150\text{ }^\circ\text{C}$ )



### Description

L5150CJ is a low dropout linear regulator with microprocessor control functions such as power on reset, low voltage reset, early warning.

Typical quiescent current is 55  $\mu A$  at very low output current.

On chip trimming results in high output voltage accuracy (2%). Accuracy is kept over wide temperature range, line and load variation. Early warning circuit monitors the input voltage and compares it to an internal voltage reference.

Output voltage reset threshold can be adjusted down to 3.5 V by means of an external voltage divider.

The maximum input voltage is 40 V. The maximum output current is internally limited. Internal temperature protection disables the voltage regulator output. In addition, only low-value ceramic capacitor on output is required for stability.

**Table 1. Device summary**

Package	Order codes	
	Tube	Tape & reel
PowerSSO-12	L5150CJ	L5150CJTR
SO-8	L5150CS	L5150CSTR

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# 1 Block diagram and pins description

Figure 1. Block diagram

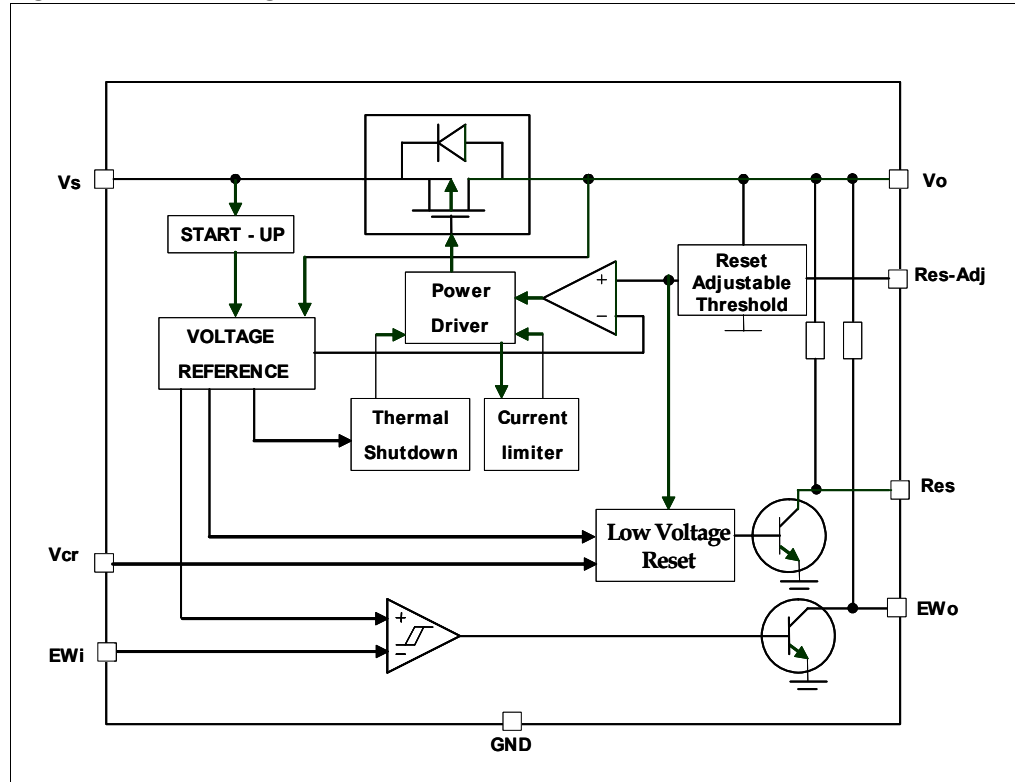


Figure 2. Configuration diagram (top view)

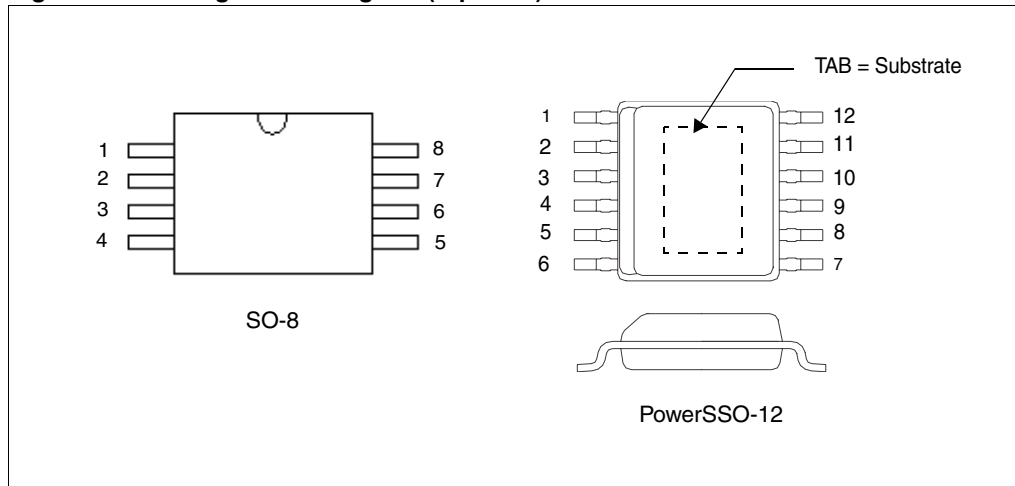


Table 2. Pins description

Pin name	PowerSSO-12 pin #	SO-8 pin #	Function
$R_{es\_Adj}$	1	8	Reset adjustable threshold. Connected to an appropriate external voltage divider, it allows to properly set the reset threshold down to 3.5 V. Connect to GND if not needed.
$R_{es}$	2	1	Reset output. Internally connected to $V_o$ through a 20 K $\Omega$ pull up resistor. This pin is pulled low when $V_o < V_{o\_th}$ . Keep open if not needed.
$V_{cr}$	3	2	Reset delay. Connect an external capacitor between $V_{cr}$ pin and ground to adjust the reset delay time. Keep open if not needed.
GND	4	3	Ground reference.
NC	5, 11, 8, 9	-	Not connected.
$V_o$	6	4	5 V regulated output. Block to GND with a ceramic capacitor ( $C_o \geq 220$ nF for regulator stability).
$V_S$	7	5	Supply voltage, block directly to GND on the IC with a capacitor.
$EW_i$	10	6	Early warning input. This pin monitors the $V_S$ voltage level through a resistor divider. Connect to $V_S$ if not needed.
$EW_o$	12	7	Early warning output. Internally connected to $V_o$ through 20 K $\Omega$ pull up resistor. This pin is pulled low when $EW_i$ is below bandgap reference voltage. Keep open if not needed.
TAB	-	-	TAB is connected to the substrate of the chip: connect to GND or leave open (see <a href="#">Figure 2</a> for PowerSSO-12 only).

## 2 Electrical specifications

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in the [Table 3: Absolute maximum ratings](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality documents.

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V <sub>sdc</sub>	DC supply voltage	-0.3 to 40	V
I <sub>sdc</sub>	Input current	internally limited	
V <sub>odc</sub>	DC output voltage	-0.3 to 6	V
I <sub>odc</sub>	DC output current	internally limited	
V <sub>od Res</sub>	Open drain output voltage R <sub>es</sub>	-0.3 to V <sub>odc</sub> + 0.3	V
I <sub>od Res</sub>	Open drain output current R <sub>es</sub>	internally limited	
V <sub>Res_adj</sub>	V <sub>Res_adj</sub> voltage	-0.3 to V <sub>odc</sub> + 0.3	V
V <sub>od EW<sub>o</sub></sub>	Open drain output voltage EW <sub>o</sub>	-0.3 to V <sub>odc</sub> + 0.3	V
I <sub>od EW<sub>o</sub></sub>	Open drain output current EW <sub>o</sub>	internally limited	
V <sub>cr</sub>	V <sub>cr</sub> voltage	-0.3 to V <sub>o</sub> + 0.3	V
V <sub>EW<sub>i</sub></sub>	Early warning input voltage	-0.3 to 40	V
T <sub>j</sub>	Junction temperature	-40 to 150	°C
V <sub>ESD HBM</sub>	ESD HBM voltage level (HBM-MIL STD 883C)	+/- 2	kV
V <sub>ESD CDM</sub>	ESD CDM voltage level (CDM- )	+/- 750	V

## 2.2 Thermal data

**Table 4. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction to case: PowerSSO-12	20	°K/W
$R_{thj-lead}$	Thermal resistance junction to lead: SO-8	55	°K/W
$R_{thj-amb}^{(1)}$	Thermal resistance junction to ambient: PowerSSO-12	52	°K/W
	SO-8	112	

1. **PowerSSO-12:** The values quoted are for PCB 77 mm x 86 mm x 1.6 mm, FR4, double copper layer with single heatsink layer, copper thickness 70  $\mu$ m, thermal vias, copper area 2 cm<sup>2</sup>.  
**SO-8:** The values quoted are for PCB 48 mm x 48 mm x 2 mm, FR4, double copper layer with single heatsink layer, copper thickness 35  $\mu$ m, copper area 2 cm<sup>2</sup>.

## 2.3 Electrical characteristics

Values specified in this section are for  $V_S = 5.6$  V to 31 V,  $T_j = -40$  °C to +150 °C unless otherwise stated.

**Table 5. General**

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_o$	$V_{o\_ref}$	Output voltage	$V_S = 8$ V to 18 V $I_o = 8$ mA to 150 mA	4.9	5.0	5.1	V
$V_o$	$V_{o\_ref}$	Output voltage	$V_S = 5.6$ V to 31 V $I_o = 8$ mA to 150 mA	4.85	5.0	5.15	V
$V_o$	$V_{o\_ref}$	Output voltage	$V_S = 5.6$ V to 31 V $I_o = 0.1$ mA to 8 mA	4.75	5.0	5.25	V
$V_o$	$I_{short}$	Short-circuit current	$V_S = 13.5$ V	0.65	0.95	1.25	A
$V_o$	$I_{lim}$	Output current capability <sup>(1)</sup>	$V_S = 13.5$ V	280	470	660	mA
$V_S, V_o$	$V_{line}$	Line regulation voltage	$V_S = 6$ V to 28 V $I_o = 30$ mA			40	mV
$V_o$	$V_{load}$	Load regulation voltage	$V_S = 8$ V to 18 V, $I_o = 8$ mA to 150 mA			55	mV
			$V_S = 13.5$ V, $T_j = 25$ °C $I_o = 8$ mA to 150 mA			40	
$V_S, V_o$	$V_{dp}$	Drop voltage <sup>(2)</sup>	$I_o = 150$ mA			500	mV
$V_S, V_o$	SVR	Ripple rejection	$f_r = 100$ Hz <sup>(3)</sup>		60		dB
$V_o$	$I_{o\_th\_H}$	Normal consumption mode output current	$V_S = 8$ V to 18 V	8			mA



**Table 5. General (continued)**

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V <sub>o</sub>	I <sub>o<sub>th_L</sub></sub>	Very low consumption mode output current	V <sub>S</sub> = 8 V to 18 V			1.1	mA
V <sub>o</sub>	I <sub>o<sub>th_Hyst</sub></sub>	Output current switching threshold hysteresis	V <sub>S</sub> = 13.5 V T <sub>j</sub> = 25 °C		0.8		mA
V <sub>S</sub> , V <sub>o</sub>	I <sub>qn_1</sub>	Current consumption I <sub>qn_1</sub> = I <sub>V<sub>S</sub></sub> - I <sub>o</sub>	V <sub>S</sub> = 13.5 V, I <sub>o</sub> = 0.1 mA to 1 mA, T <sub>j</sub> = 25 °C		55	80	μA
			V <sub>S</sub> = 13.5 V, I <sub>o</sub> = 0.1 mA to 1 mA,			95	
V <sub>S</sub> , V <sub>o</sub>	I <sub>qn_150</sub>	Current consumption I <sub>qn_150</sub> = I <sub>V<sub>S</sub></sub> - I <sub>o</sub>	V <sub>S</sub> = 13.5 V I <sub>o</sub> = 150 mA		3	4.2	mA
	T <sub>w</sub>	Thermal protection temperature		150		190	°C
	T <sub>w_hy</sub>	Thermal protection temperature hysteresis			10		°C

1. Measured Output Current when the output voltage has dropped 100 mV from its nominal Value obtained at 13.5 V and I<sub>o</sub> = 75 mA.
2. V<sub>S</sub> - V<sub>o</sub> Measured Dropout when the output voltage has dropped 100 mV from its nominal Value obtained at 13.5 V and I<sub>o</sub> = 75 mA.
3. Guaranteed by design.

**Table 6. Reset**

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R <sub>es</sub>	V <sub>res_l</sub>	Reset output low voltage	R <sub>ext</sub> = 5 kΩ V <sub>o</sub> > 1 V			0.4	V
R <sub>es</sub>	I <sub>Res_lkg</sub>	Reset output high leakage current	V <sub>Res</sub> = 5 V			1	μA
R <sub>es</sub>	R <sub>Res</sub>	Pull up internal resistance	Versus V <sub>o</sub>	10	20	40	kΩ
R <sub>es</sub>	V <sub>o_th</sub>	V <sub>o</sub> out of regulation threshold	V <sub>res_adj</sub> < 0.2 V, V <sub>o</sub> decreasing	6	8	10	% Below V <sub>o_ref</sub>
R <sub>es_adj</sub>	V <sub>res_adj</sub>	Reset adjustable switching threshold		2.35	2.5	2.65	V
R <sub>es_adj</sub>	V <sub>Res_adjl</sub>	Reset adjustable low voltage		0.4	0.9	1.3	V
R <sub>es_adj</sub>	I <sub>Res_adj_lkg</sub>	Reset adjustable leakage current	V <sub>res_adj</sub> = 2.5 V	-1		1	μA
V <sub>cr</sub>	V <sub>Rlth</sub>	Reset timing low threshold	V <sub>S</sub> = 13.5 V	15	18	22	% V <sub>o_ref</sub>
V <sub>cr</sub>	V <sub>Rhth</sub>	Reset timing high threshold	V <sub>S</sub> = 13.5 V	47	50	53	% V <sub>o_ref</sub>

**Table 6. Reset (continued)**

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V <sub>cr</sub>	I <sub>cr</sub>	Charge current	V <sub>S</sub> = 13.5 V	10	20	30	μA
V <sub>cr</sub>	I <sub>dr</sub>	Discharge current	V <sub>S</sub> = 13.5 V	10	20	30	μA
R <sub>es</sub>	T <sub>rr</sub>	Reset reaction time				2	μs
R <sub>es</sub>	T <sub>rd</sub>	Reset delay time	V <sub>S</sub> = 13.5 V, C <sub>tr</sub> = 1000 pF	2	4	6	ms

**Table 7. Early warning**

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
EW <sub>i</sub>	V <sub>EWi_thl</sub>	EW input low threshold voltage		2.35	2.50	2.65	V
EW <sub>i</sub>	V <sub>EWi_thh</sub>	EW input high threshold voltage		2.42	2.57	2.72	V
EW <sub>i</sub>	V <sub>EWi_thhyst</sub>	EW input threshold hysteresis			70		mV
EW <sub>i</sub>	I <sub>EWi_lkg</sub>	EW input leakage current	V <sub>EWi</sub> = 2.5 V, V <sub>S</sub> > 4 V	-1		1	μA
EW <sub>o</sub>	R <sub>EWo</sub>	Pull up internal resistance	Versus V <sub>o</sub>	10	20	40	kΩ
EW <sub>o</sub>	V <sub>EWo_lv</sub>	EW output low voltage (with external pull up)	V <sub>EWi</sub> < 2.35 V, V <sub>S</sub> > 4 V, R <sub>ext</sub> = 5 kΩ			0.4	V
EW <sub>o</sub>	I <sub>EWo_lkg</sub>	EW output leakage current	V <sub>EWo</sub> = 5 V			1	μA

## 2.4 Electrical characteristics curves

Figure 3. Output voltage vs.  $T_j$

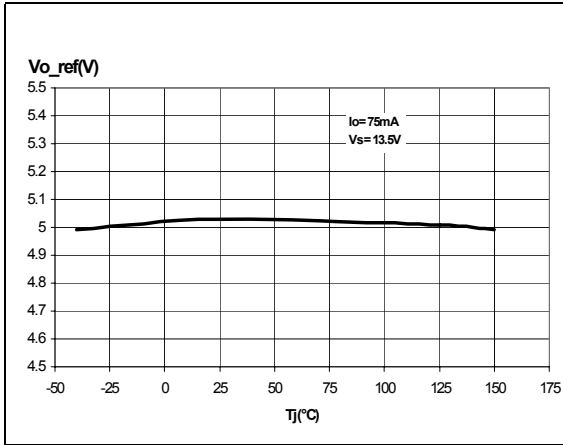


Figure 4. Output voltage vs.  $V_s$

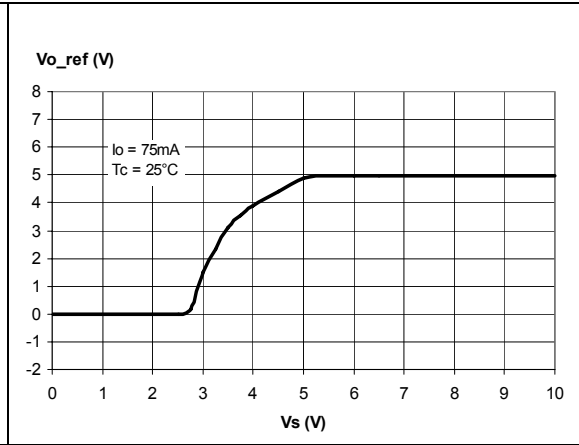


Figure 5. Drop voltage vs. output current

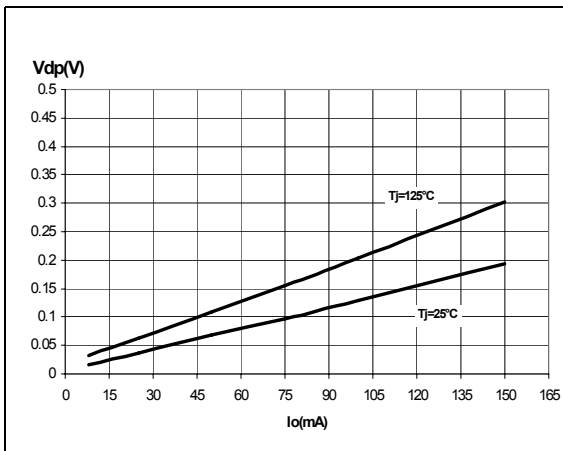


Figure 6. Current consumption vs. output current

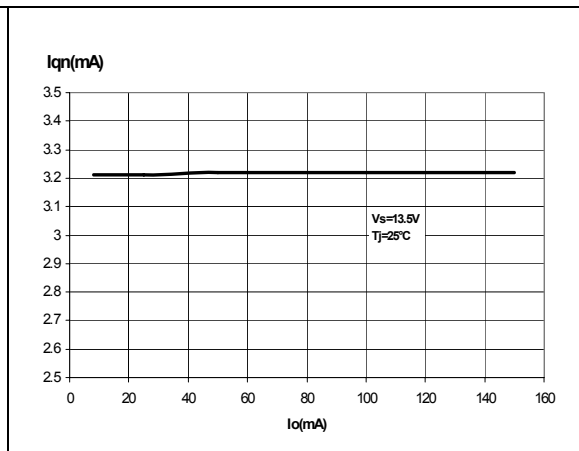


Figure 7. Current consumption vs. output current (at light load condition)

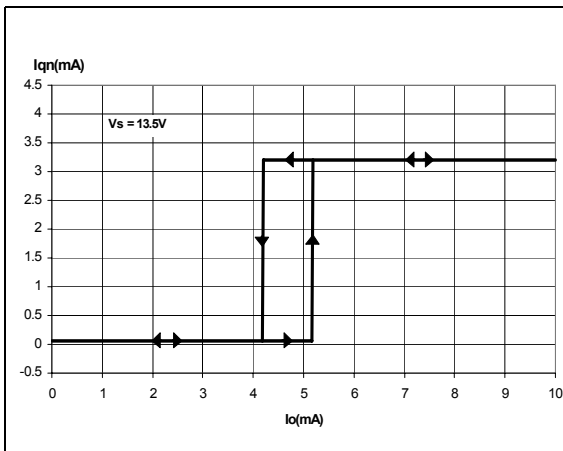


Figure 8. Current consumption vs. input voltage ( $I_o = 0.1 \text{ mA}$ )

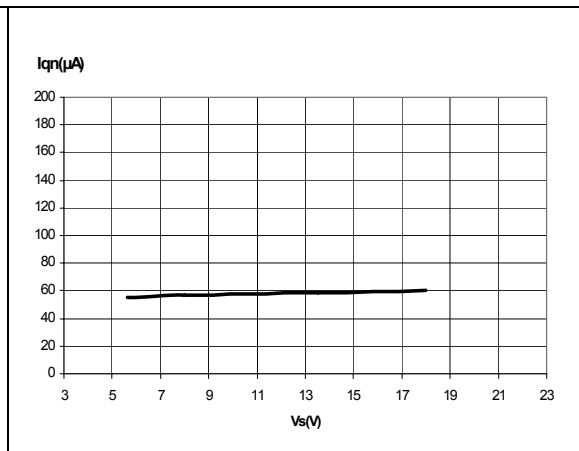


Figure 9. Current consumption vs. input voltage ( $I_o = 75\text{ mA}$ )

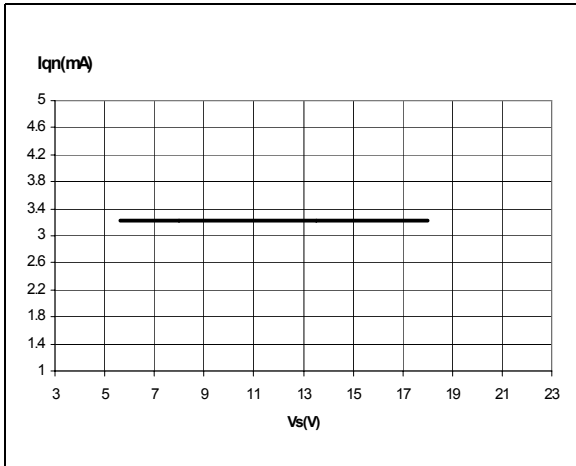


Figure 10. Current limitation vs.  $T_j$

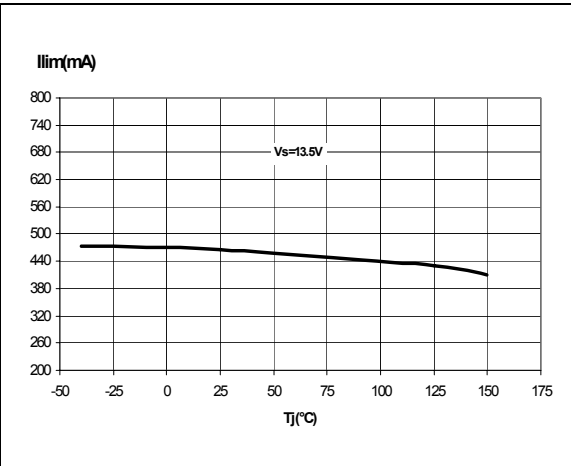


Figure 11. Current limitation vs. input voltage

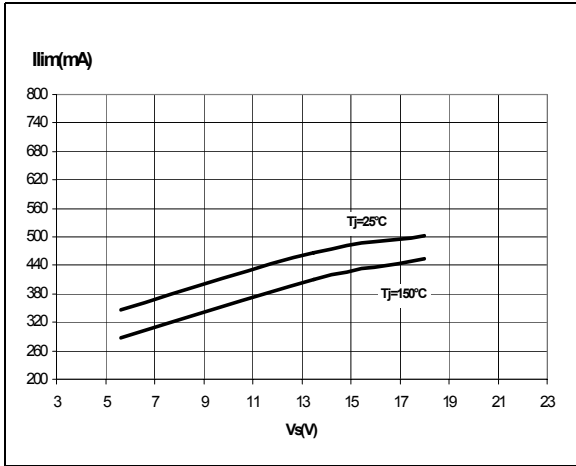


Figure 12. Short-circuit current vs.  $T_j$

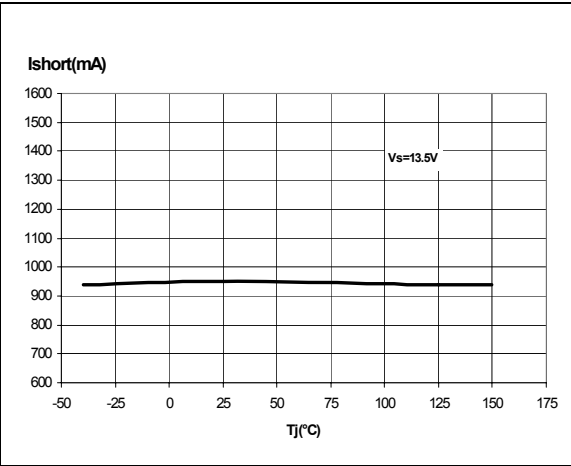


Figure 13. Short-circuit current vs. input voltage

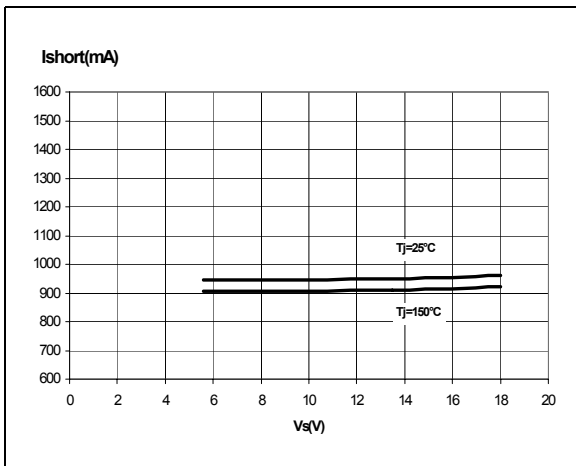


Figure 14.  $V_{Rhth}$  vs.  $T_j$

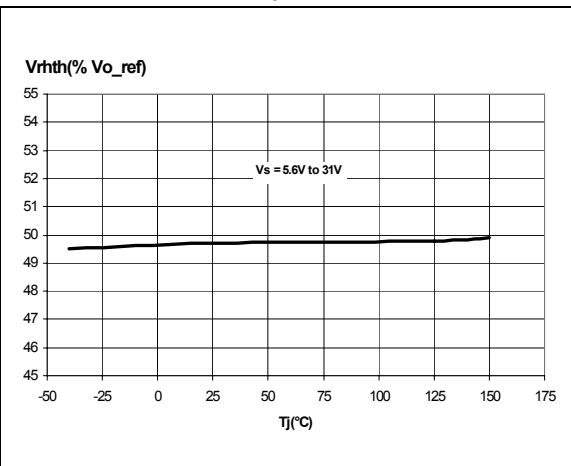


Figure 15.  $V_{Rlth}$  vs.  $T_j$

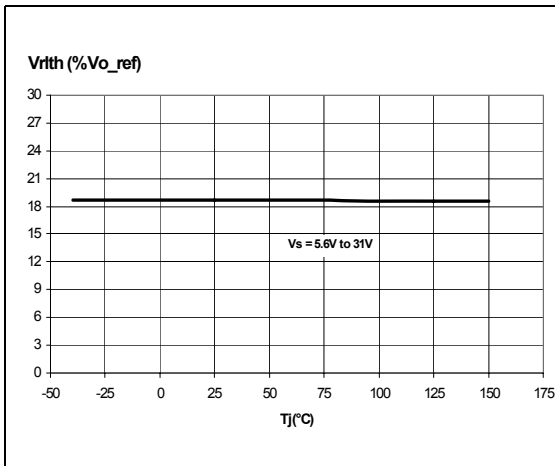


Figure 16.  $V_{EWi\_thh}$  vs.  $T_j$

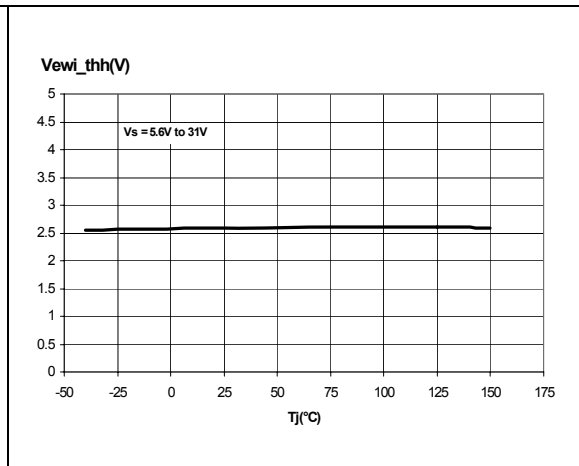


Figure 17.  $V_{EWi\_thl}$  vs.  $T_j$

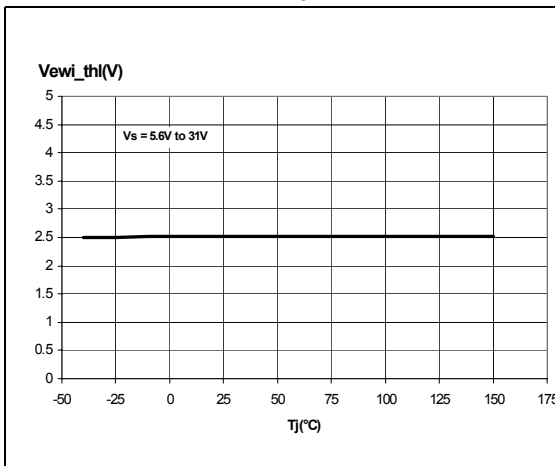


Figure 18.  $I_{cr}$  vs.  $T_j$

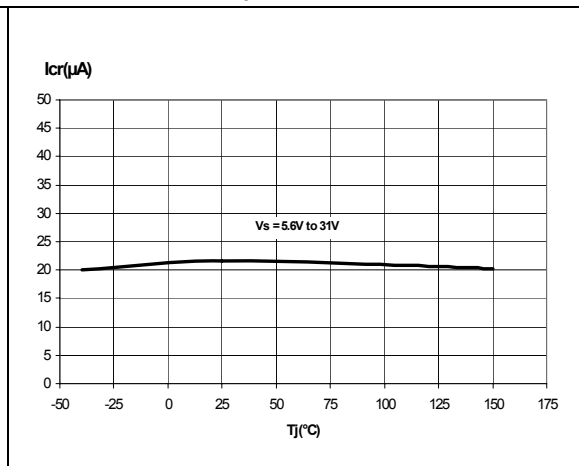


Figure 19.  $I_{dr}$  vs.  $T_j$

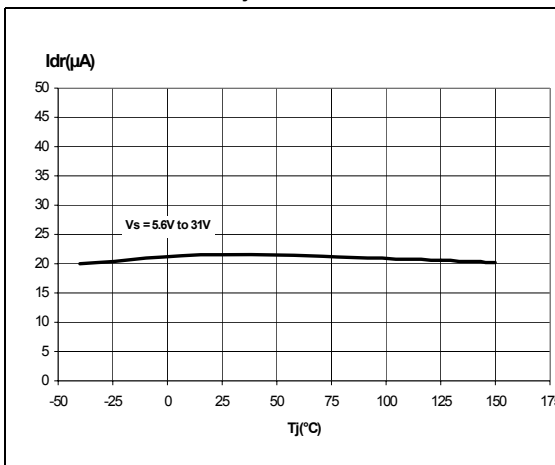
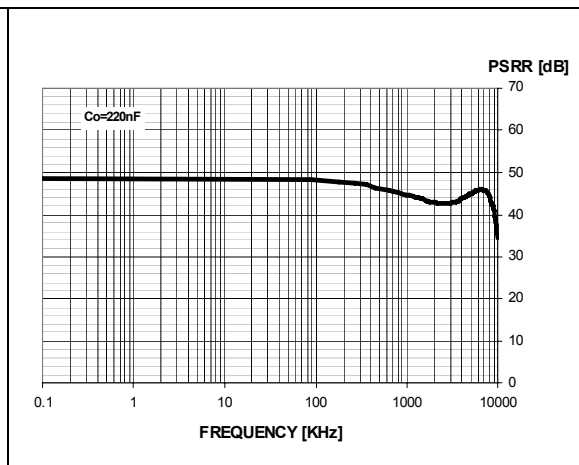


Figure 20. PSRR

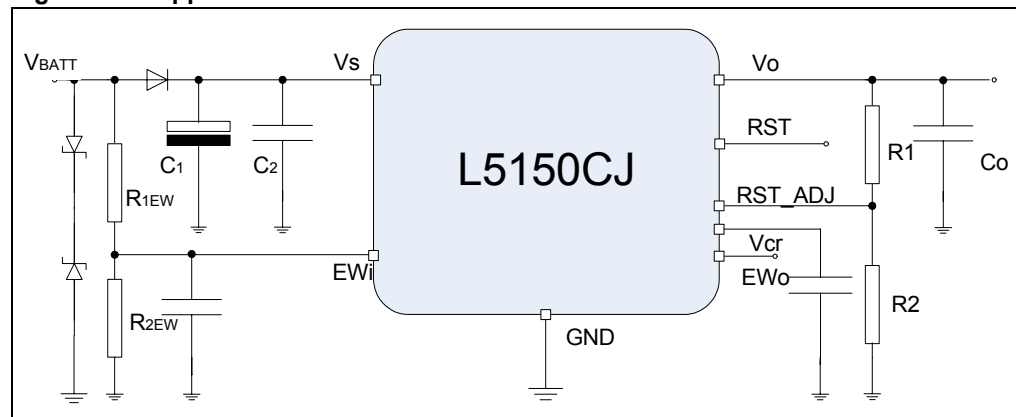


### 3 Application information

#### 3.1 Voltage regulator

The voltage regulator uses a p-channel mos transistor as a regulating element. With this structure a very low dropout voltage at current up to 150 mA is obtained. The output voltage is regulated up to input supply voltage of 40 V. The high-precision of the output voltage (2%) is obtained with a pre-trimmed reference voltage. The voltage regulator automatically adapts its own quiescent current to the output current level. In light load conditions the quiescent current goes to 55  $\mu$ A only (low consumption mode). This procedure features a certain hysteresis on the output current (see [Figure 7](#)). Short-circuit protection to GND and a thermal shutdown are provided.

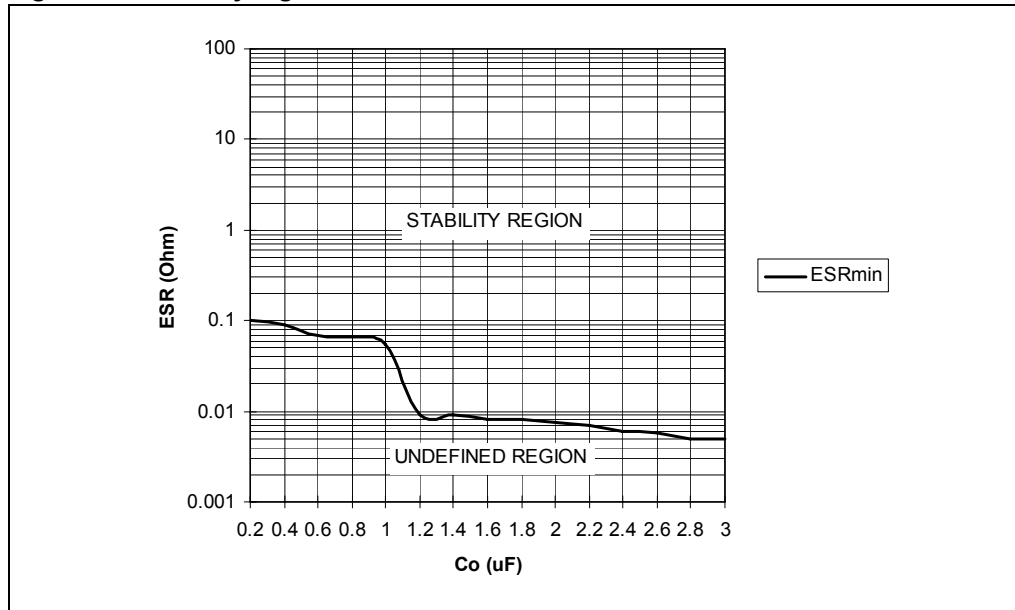
**Figure 21. Application schematic**



The input capacitor  $C_1 \geq 100 \mu\text{F}$  is necessary as backup supply for negative pulses which may occur on the line. The second input capacitor  $C_2 \geq 220 \text{ nF}$  is needed when the  $C_1$  is too distant from the  $V_S$  pin and it compensates smooth line disturbances. The  $C_0$  ceramic capacitor, connected to the output pin, is for bypassing to GND the high-frequency noise and it guarantees stability even during sudden line and load variations. Suggested value is  $C_0 = 220 \text{ nF}$  with  $\text{ESR} \geq 100 \text{ m}\Omega$ .

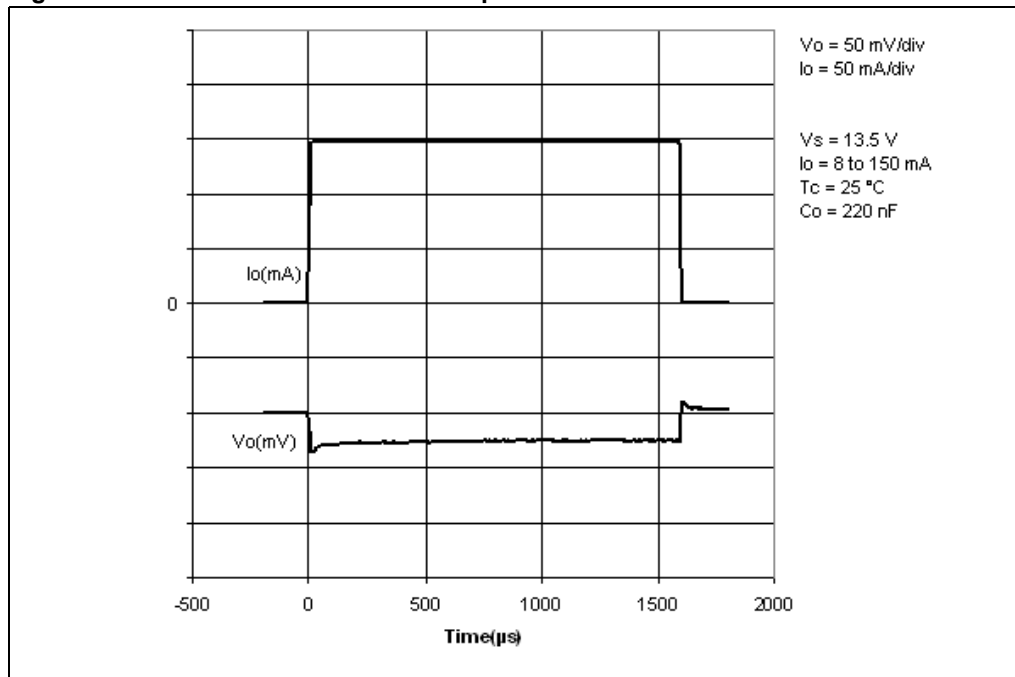
Stability region is reported in [Figure 22](#).

Figure 22. Stability region<sup>(1)</sup>



1. The curve which describes the minimum ESR is derived from characterization data on the regulator with connected ceramic capacitors which feature low ESR values (at 100 kHz). Any capacitor with further lower ESR than the given plot value must be evaluated in each and every case.

Figure 23. Maximum load variation response



## 3.2 Reset

The reset circuit monitors the output voltage  $V_o$ . If the output voltage becomes lower than  $V_{o\_th}$  then  $R_{es}$  goes low with a delay time ( $t_{rr}$ ). When the output voltage becomes higher than  $V_{o\_th}$  then  $R_{es}$  goes high with a delay time  $t_{rd}$ . This delay is obtained by 32 periods of oscillator. The oscillator period is given by:

### Equation 1

$$T_{osc} = [(V_{Rhth} - V_{Rlth}) \times C_{tr}] / I_{cr} + [(V_{Rhth} - V_{Rlth}) \times C_{tr}] / I_{dr}$$

where:

$I_{cr} = 20 \mu A$  is an internally generated charge current,

$I_{dr} = 20 \mu A$  is an internally generated discharge current,

$V_{Rhth} = 2.5 V$  (typ) and  $V_{Rlth} = 0.9 V$  (typ) are two voltage thresholds,

$C_{tr}$  is an external capacitor put between  $V_{cr}$  pin and GND.



Reset pulse delay  $T_{rd}$  is given by:

**Equation 2**

$$t_{rd} = 32 \times T_{osc}$$

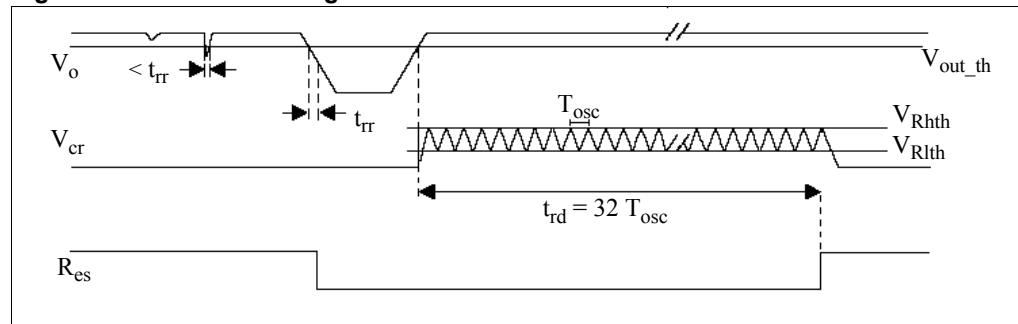
The Output Voltage Reset threshold can be adjusted via an external voltage divider  $R_1 + R_2$  ( $R_1$  connected between  $R_{es\_Adj}$  and  $V_0$ ,  $R_2$  connected between  $R_{es\_Adj}$  and GND) according to the following formula:

**Equation 3**

$$V_{thre} = [(R_1 + R_2) / R_2] \times V_{Res\_adj}$$

The Output Voltage Reset threshold can be decreased down to 3.5 V. If it is needed to maintain it to its default value (8% below  $V_{0\_ref}$  typical), it is enough to connect the  $R_{es\_Adj}$  pin directly to GND.

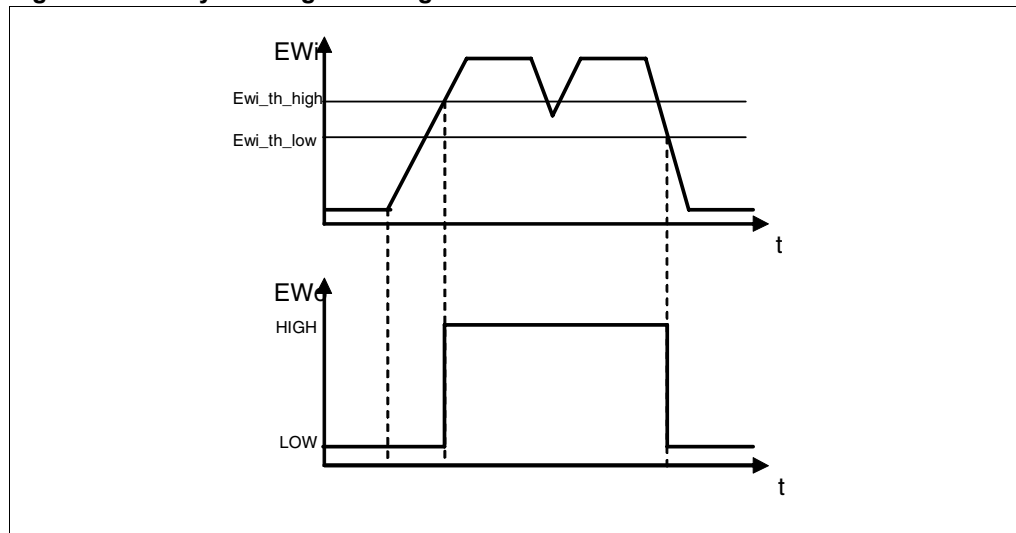
**Figure 24. Reset time diagram**



### 3.3 Early warning

This circuit compares the  $EW_i$  input signal with the internal voltage reference (typically 2.5 V). The use of an external voltage divider makes the comparator very flexible in the application. This function can be used to supervise the supply input voltage either before or after the protection diode and to give additional information to the microprocessor such as low voltage warnings.

Figure 25. Early warning time diagram



## 4 Package and PCB thermal data

### 4.1 PowerSSO-12 thermal data

Figure 26. PowerSSO-12 PC board<sup>(1)</sup>



1. Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB: double layer, thermal vias, FR4 area = 77 mm x 86 mm, PCB thickness = 1.6 mm, Cu thickness = 70  $\mu$ m (front and back side), thermal vias separation 1.2 mm, thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 25  $\mu$ m, footprint dimension 4.1 mm x 6.5 mm).

Figure 27.  $R_{thj-amb}$  Vs. PCB copper area in open box free air condition

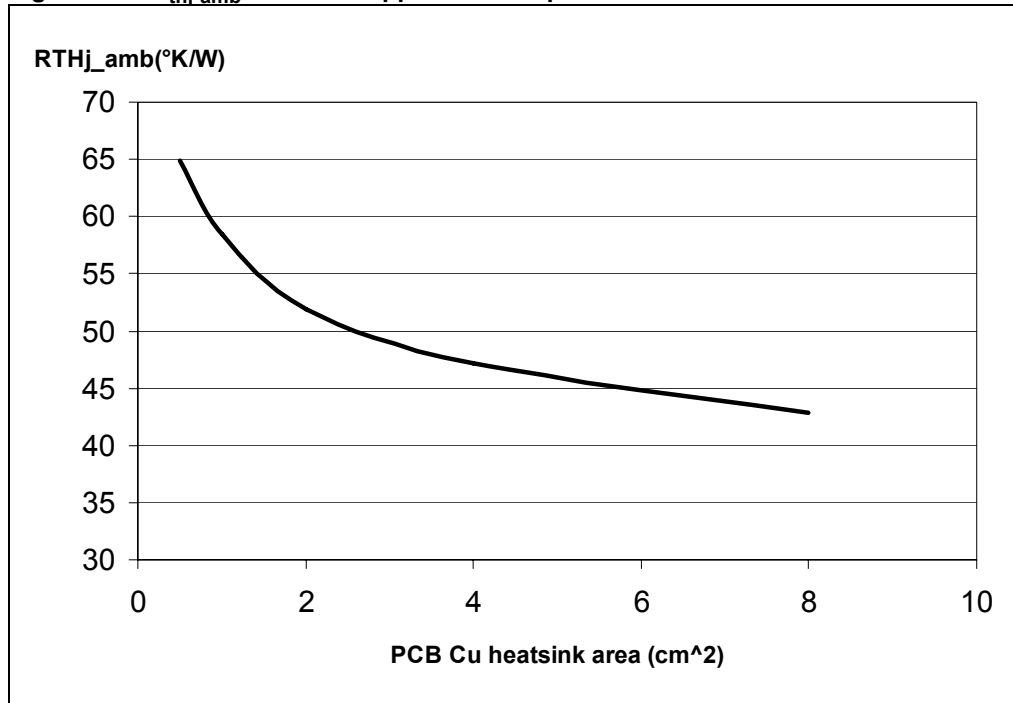
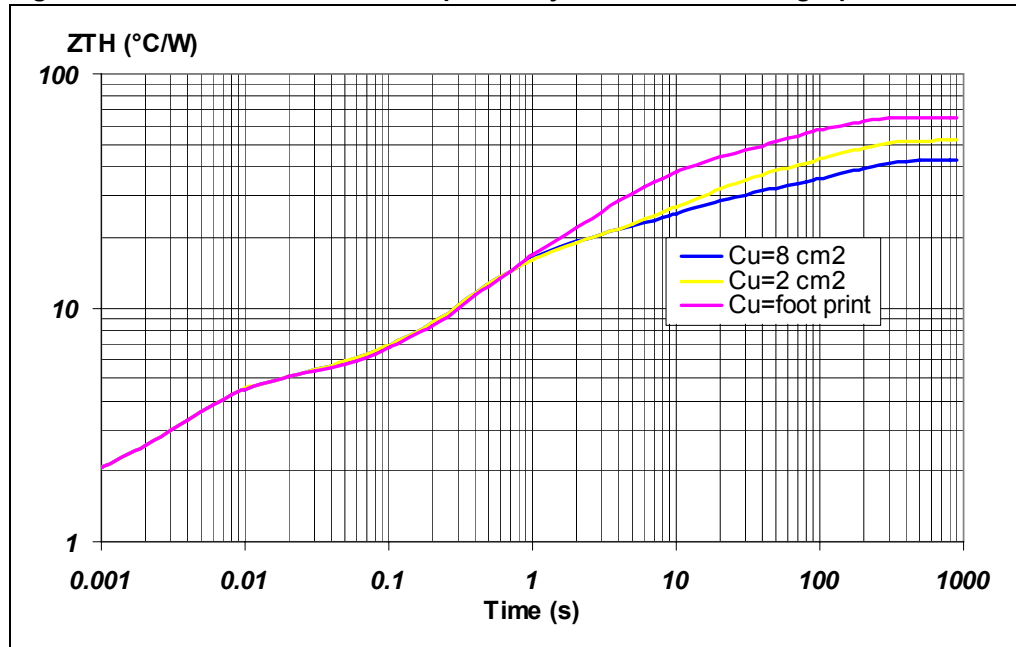


Figure 28. PowerSSO-12 thermal impedance junction ambient single pulse

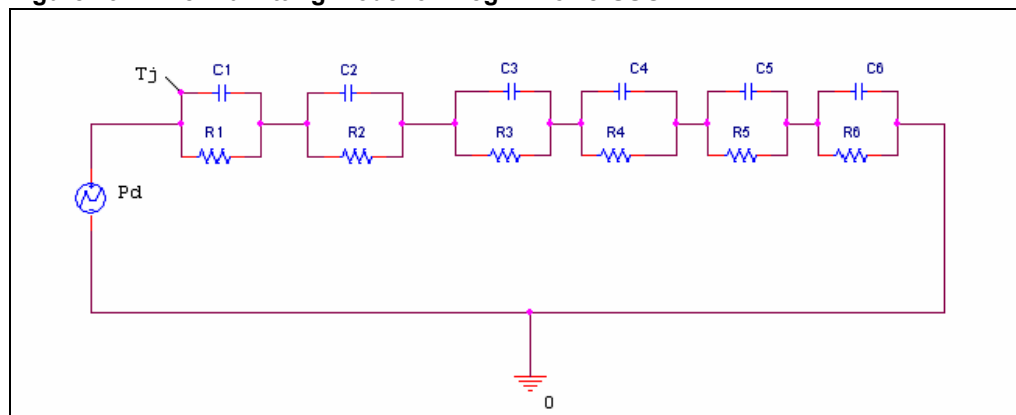


Equation 4: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Figure 29. Thermal fitting model of Vreg in PowerSSO-12

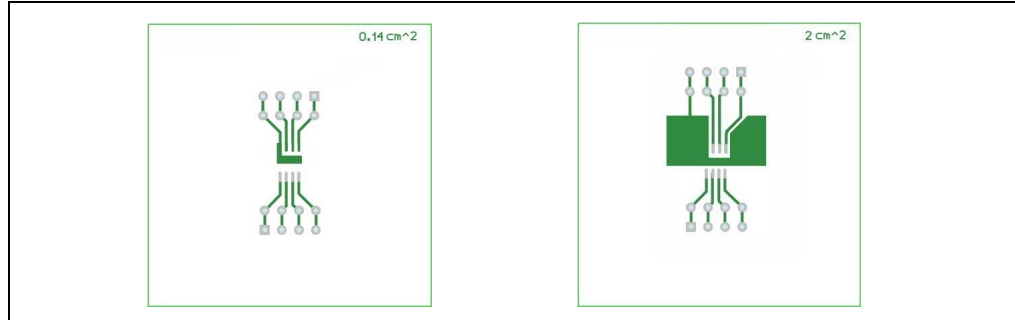


**Table 8. PowerSSO-12 thermal parameter**

Area (cm <sup>2</sup> )	Footprint	2	8
R1 (°K/W)	1.53		
R2 (°K/W)	3.21		
R3 (°K/W)	5.2		
R4 (°K/W)	7	7	8
R5 (°K/W)	22	15	10
R6 (°K/W)	26	20	15
C1 (W.s/°K)	0.00004		
C2 (W.s/°K)	0.0016		
C3 (W.s/°K)	0.08		
C4 (W.s/°K)	0.2	0.1	0.1
C5 (W.s/°K)	0.27	0.8	1
C6 (W.s/°K)	3	6	9

## 4.2 SO-8 thermal data

Figure 30. SO-8 PC board<sup>(1)</sup>



1. Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB: double layer, thermal vias, FR4 area = 48 mm x 48 mm, PCB thickness = 2 mm, Cu thickness = 35  $\mu$ m (front and back side), Cu thickness on vias 25  $\mu$ m, Footprint dimension 4.1 mm x 6.5 mm ).

Figure 31.  $R_{thj-amb}$  Vs. PCB copper area in open box free air condition

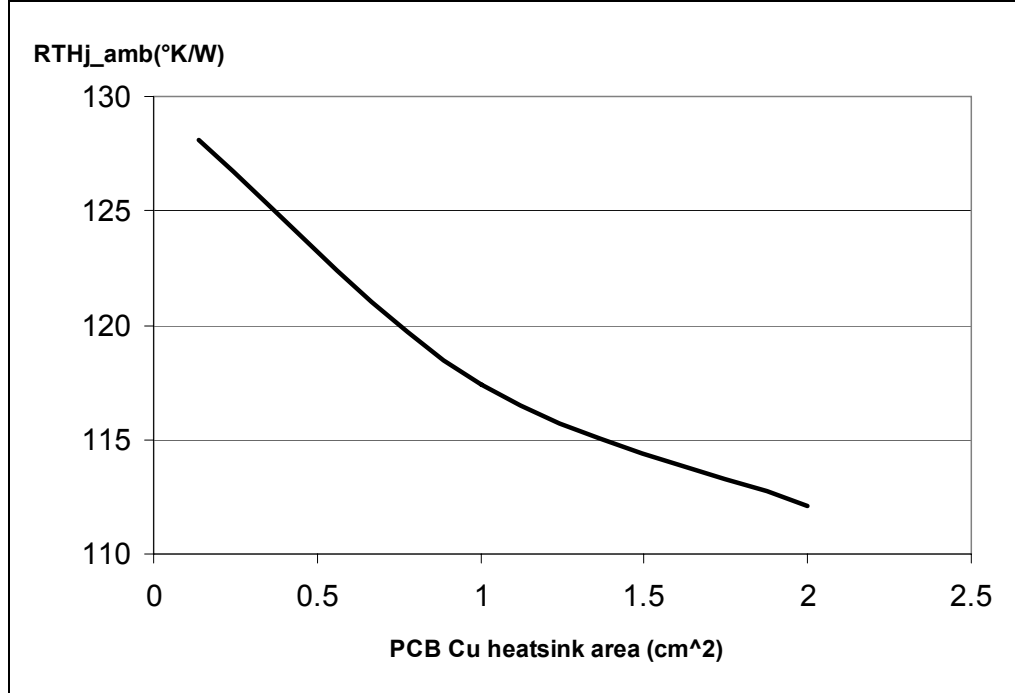
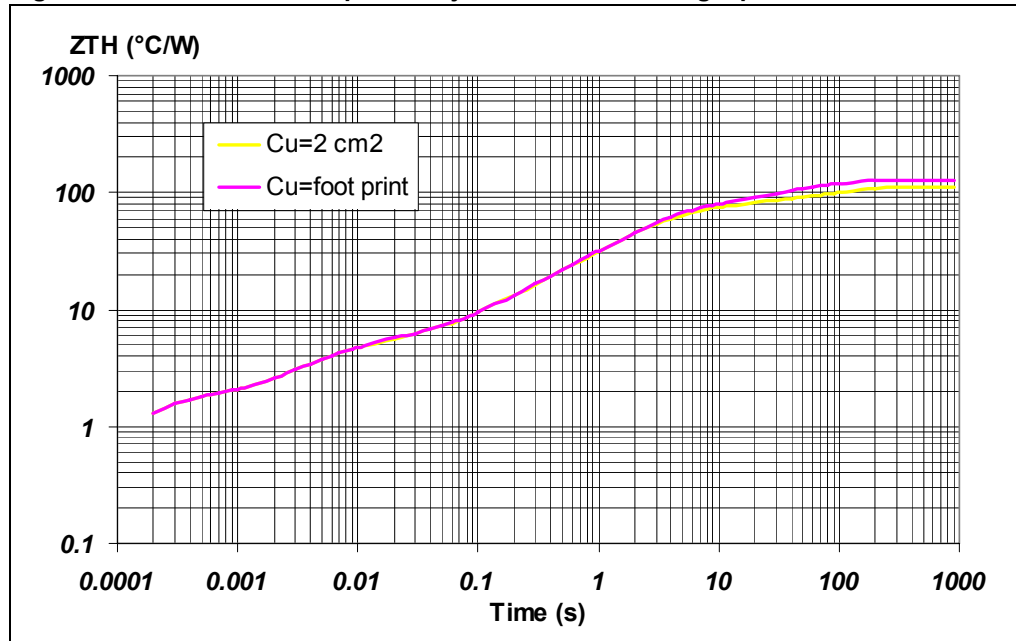


Figure 32. SO-8 thermal impedance junction ambient single pulse

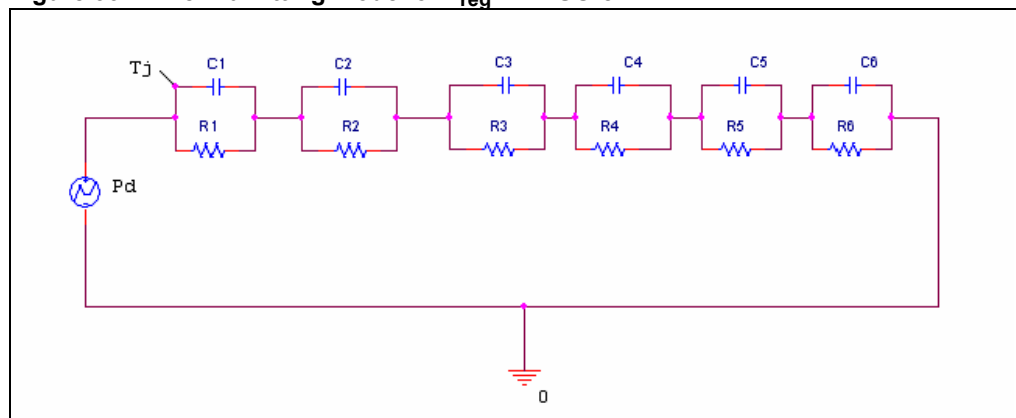


Equation 5: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Figure 33. Thermal fitting model of  $V_{reg}$  in in SO-8



**Table 9. SO-8 thermal parameter**

Area (cm <sup>2</sup> )	Footprint	2
R1 (°K/W)	1.53	
R2 (°K/W)	3.21	
R3 (°K/W)	5.4	
R4 (°K/W)	32	
R5 (°K/W)	34	
R6 (°K/W)	52	36
C1 (W.s/°K)	0.00004	
C2 (W.s/°K)	0.0016	
C3 (W.s/°K)	0.04	
C4 (W.s/°K)	0.05	
C5 (W.s/°K)	0.15	
C6 (W.s/°K)	1	2.5



## 5 Package and packing information

### 5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 5.2 PowerSSO-12 mechanical data

Figure 34. PowerSSO-12 package dimensions

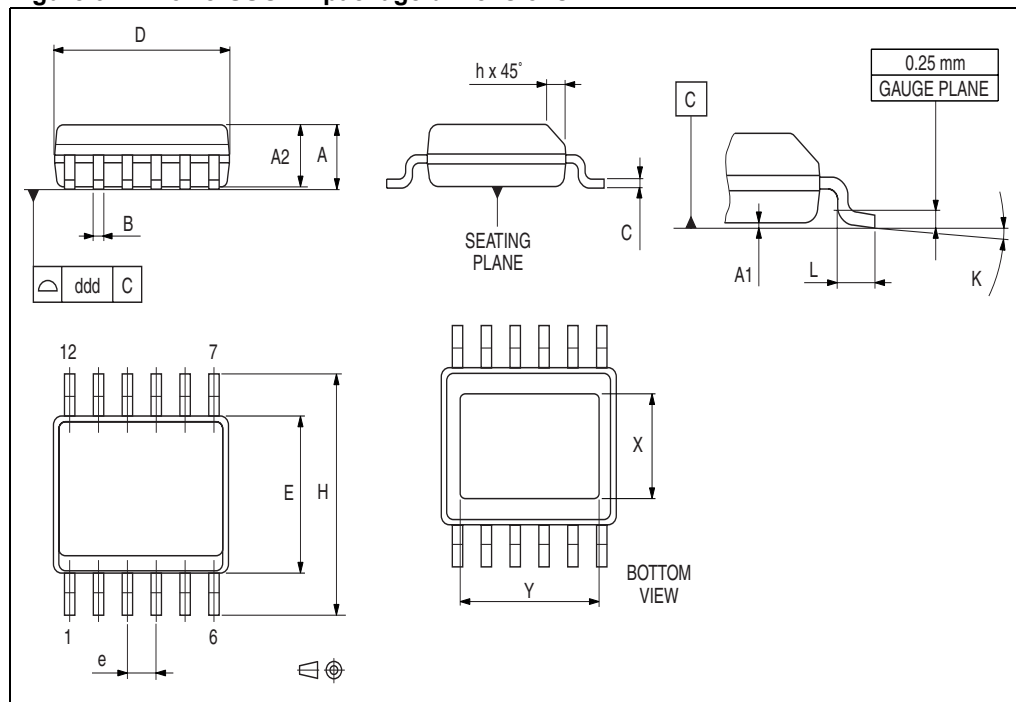


Table 10. PowerSSO-12 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	1.250		1.620
A1	0.000		0.100
A2	1.100		1.650
B	0.230		0.410
C	0.190		0.250
D	4.800		5.000
E	3.800		4.000
e		0.800	
H	5.800		6.200
h	0.250		0.500
L	0.400		1.270
k	0°		8°
X	1.900		2.500
Y	3.600		4.200
ddd			0.100

### 5.3 SO-8 package information

Figure 35. SO-8 package dimensions

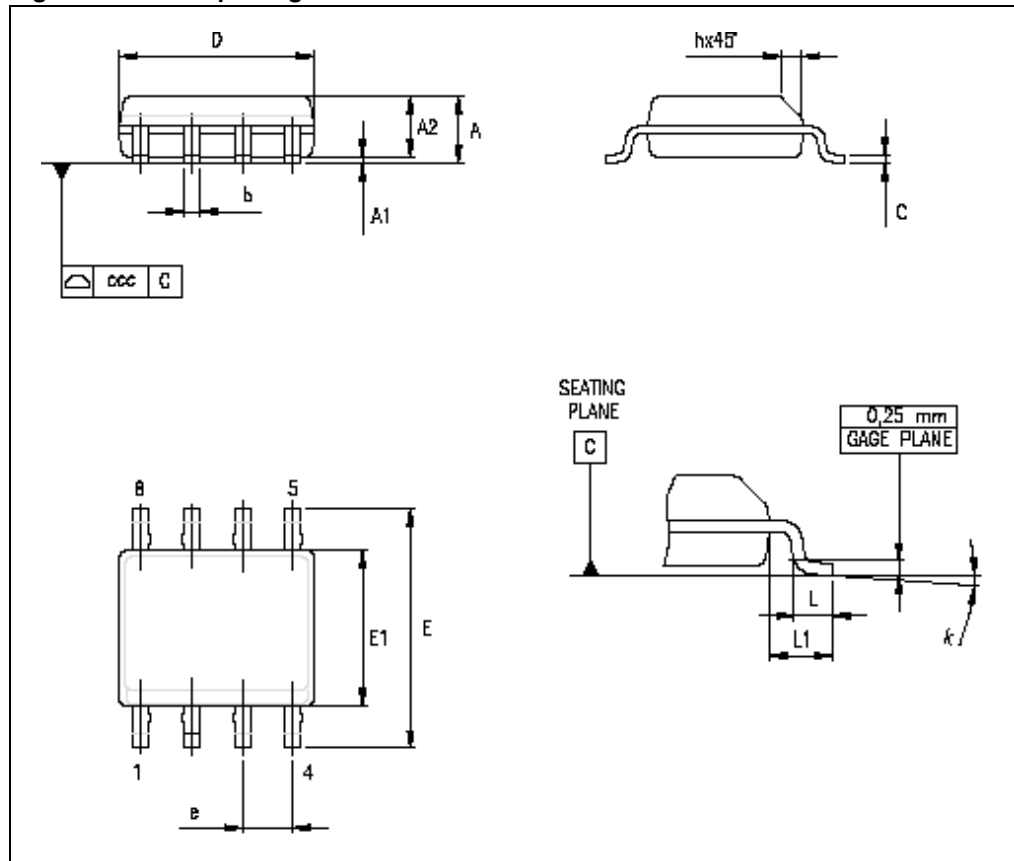


Table 11. SO-8 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D <sup>(1)</sup>	4.80	4.90	5.00
E	5.80	6.00	6.20
E1 <sup>(2)</sup>	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both side).
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

### 5.4 PowerSSO-12 packing information

Figure 36. PowerSSO-12 tube shipment (no suffix)

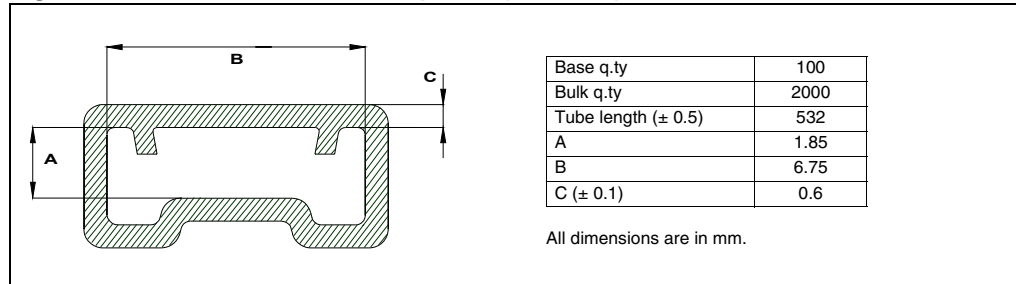
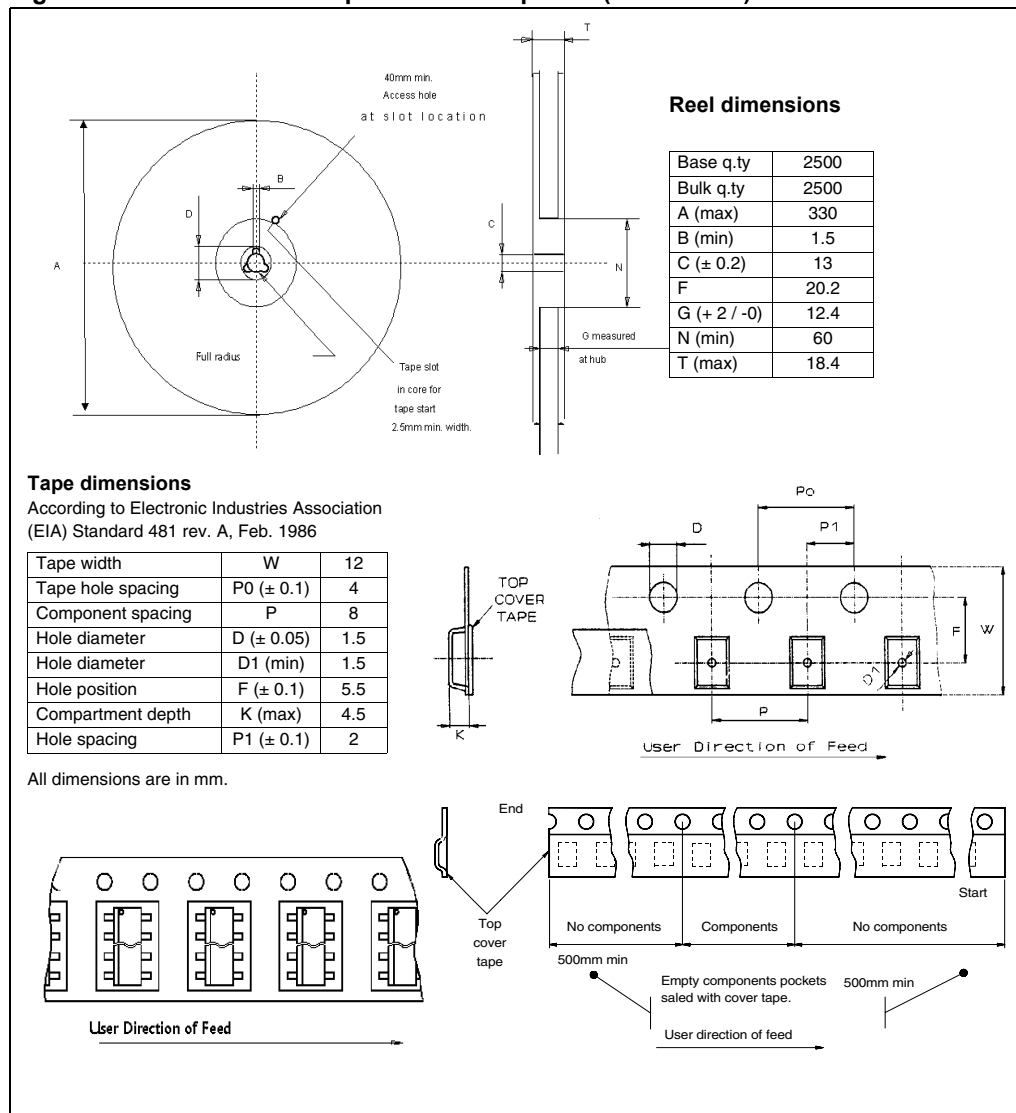


Figure 37. PowerSSO-12 tape and reel shipment (suffix "TR")



### 5.5 SO-8 packing information

Figure 38. SO-8 tube shipment (no suffix)

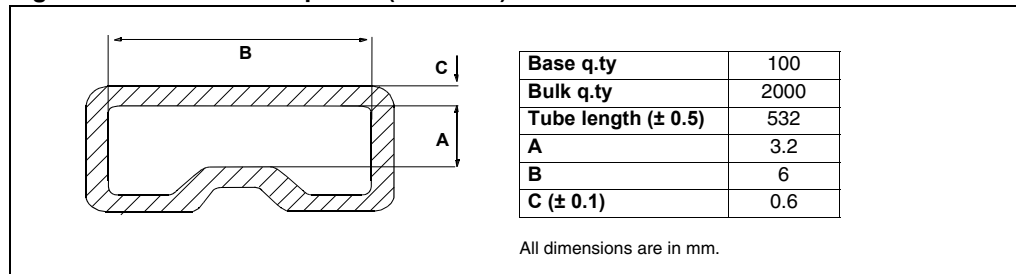
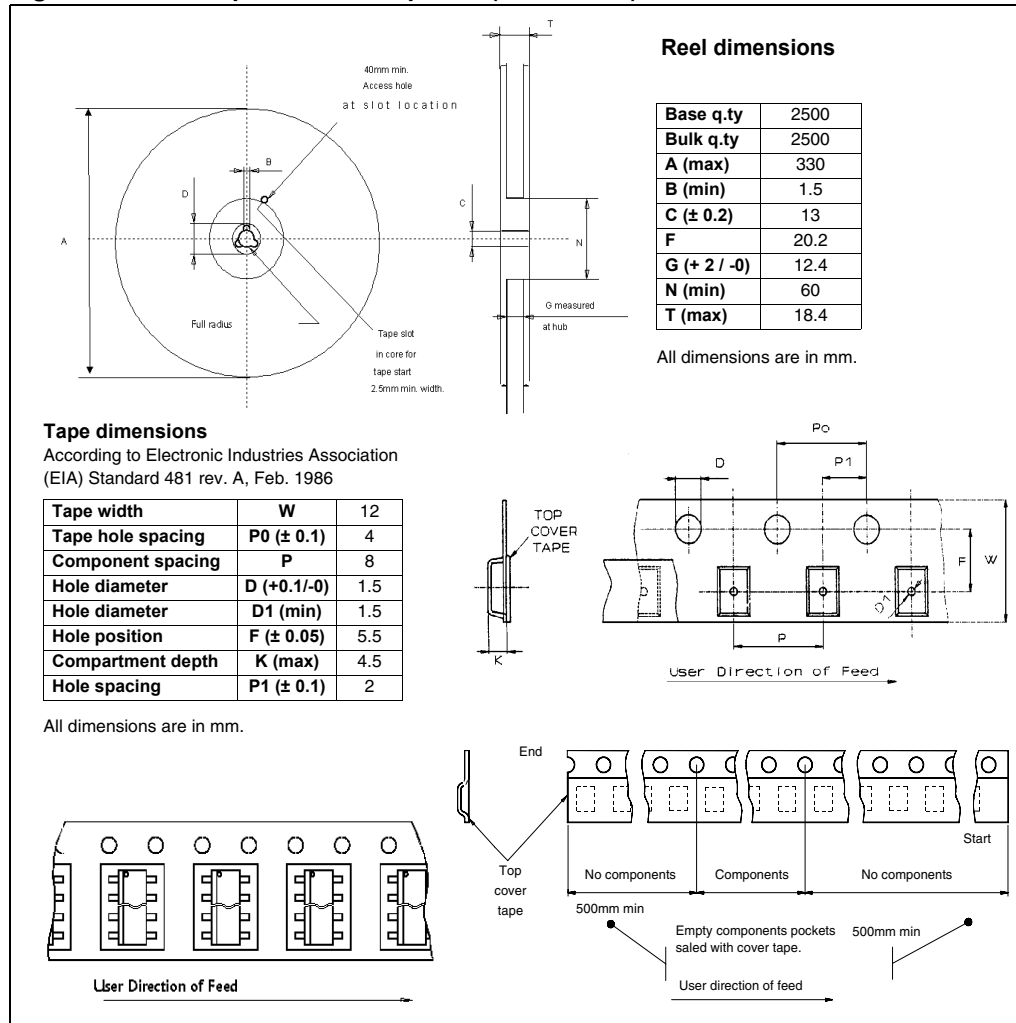


Figure 39. SO-8 tape and reel shipment (suffix "TR")



## 6 Revision history

Table 12. Document revision history

Date	Revision	Changes
09-Aug-2007	1	Initial release.
06-Mar-2008	2	<p>Updated <a href="#">Table 5.: General</a>:</p> <ul style="list-style-type: none"> <li>– changed <math>V_{o\_ref}</math>, <math>V_{line}</math>, <math>V_{load}</math> test conditions</li> <li>– added notes to <math>I_{lim}</math> and <math>V_{dp}</math> parameters</li> <li>– added <math>I_{oth\_H}</math>, <math>I_{oth\_L}</math>, <math>I_{oth}</math> parameters.</li> </ul> <p>Updated <a href="#">Table 6.: Reset</a>:</p> <ul style="list-style-type: none"> <li>– added <math>V_{res\_adj}</math> parameter</li> <li>– changed <math>V_{Rlth}</math> values (min./ typ./ max.) from 17/20/23 to 20/23/26 (% <math>V_{o\_ref}</math>).</li> </ul> <p>Modified <a href="#">Section 3.2: Reset</a>.</p>
09-May-2008	3	<p>Updated <a href="#">Table 5.: General</a> :</p> <ul style="list-style-type: none"> <li>– changed <math>I_{lim}</math> values (Min./Typ./Max.) from 0.7/1/1.30 A to 280/470/660 mA</li> <li>– <math>V_{o\_ref}</math> parameter : updated <math>I_o</math> test condition Old -&gt; <math>I_o = 0.1</math> mA to 10 mA New -&gt; <math>I_o = 0.1</math> mA to 8 mA.</li> </ul>
13-Oct-2008	4	<p>Updated <a href="#">Table 5.: General</a> :</p> <ul style="list-style-type: none"> <li>– <math>V_{load}</math> parameter : updated <math>I_o</math> test condition Old -&gt; <math>I_o = 5</math> mA to 150 mA New -&gt; <math>I_o = 8</math> mA to 150 mA.</li> </ul>
23-Oct-2008	5	Added S0-8 package option.

Table 12. Document revision history (continued)

Date	Revision	Changes
16-Apr-2009	6	<p>Updated corporate template from V2 to V3</p> <p>Updated <a href="#">Figure 2: Configuration diagram (top view)</a></p> <p><a href="#">Table 2: Pins description</a></p> <ul style="list-style-type: none"> <li>– Added new row</li> </ul> <p><a href="#">Table 3: Absolute maximum ratings</a></p> <ul style="list-style-type: none"> <li>– <math>V_{En}</math>: deleted row</li> </ul> <p><a href="#">Table 4: Thermal data</a></p> <ul style="list-style-type: none"> <li>– <math>R_{thj-amb}</math>: changed value</li> <li>– Added new row</li> <li>– Updated TableFootnote</li> </ul> <p><a href="#">Table 5: General</a></p> <ul style="list-style-type: none"> <li>– <math>V_{load}</math>: changed max value for <math>V_S = 8\text{ V}</math> to <math>18\text{ V}</math>, added new row</li> <li>– <math>I_{qn\_1}</math>: changed Test conditions (added <math>T_j = 25\text{ °C}</math>), added new row</li> </ul> <p><a href="#">Table 6: Reset</a></p> <ul style="list-style-type: none"> <li>– <math>V_{Rlth}</math>: changed min/typ/max value</li> <li>– <math>V_{Res\_adjl}</math>: replaced with <math>V_{Rlth}</math>, changed Parameter</li> </ul> <p><a href="#">Table 7: Early warning</a></p> <ul style="list-style-type: none"> <li>– Updated symbols</li> </ul> <p>Added <a href="#">Figure 3: Output voltage vs. <math>T_j</math></a></p> <p>Added <a href="#">Figure 4: Output voltage vs. <math>V_S</math></a></p> <p>Added <a href="#">Figure 5: Drop voltage vs. output current</a></p> <p>Added <a href="#">Figure 6: Current consumption vs. output current</a></p> <p>Added <a href="#">Figure 7: Current consumption vs. output current (at light load condition)</a></p> <p>Added <a href="#">Figure 8: Current consumption vs. input voltage (<math>I_o = 0.1\text{ mA}</math>)</a></p> <p>Added <a href="#">Figure 9: Current consumption vs. input voltage (<math>I_o = 75\text{ mA}</math>)</a></p> <p>Added <a href="#">Figure 10: Current limitation vs. <math>T_j</math></a></p> <p>Added <a href="#">Figure 11: Current limitation vs. input voltage</a></p> <p>Added <a href="#">Figure 12: Short-circuit current vs. <math>T_j</math></a></p> <p>Added <a href="#">Figure 13: Short-circuit current vs. input voltage</a></p> <p>Added <a href="#">Figure 14: <math>V_{Rhth}</math> vs. <math>T_j</math></a></p> <p>Added <a href="#">Figure 15: <math>V_{Rlth}</math> vs. <math>T_j</math></a></p> <p>Added <a href="#">Figure 16: <math>V_{EWi\_thh}</math> vs. <math>T_j</math></a></p> <p>Added <a href="#">Figure 17: <math>V_{EWi\_thl}</math> vs. <math>T_j</math></a></p> <p>Added <a href="#">Figure 18: <math>I_{cr}</math> vs. <math>T_j</math></a></p> <p>Added <a href="#">Figure 19: <math>I_{dr}</math> vs. <math>T_j</math></a></p> <p>Added <a href="#">Figure 20: PSRR</a></p> <p><a href="#">Section 3.1: Voltage regulator</a></p> <ul style="list-style-type: none"> <li>– Updated text</li> <li>– Added <a href="#">Figure 21: Application schematic</a></li> <li>– Added <a href="#">Figure 23: Maximum load variation response</a></li> </ul> <p><a href="#">Section 3.2: Reset</a></p> <ul style="list-style-type: none"> <li>– <math>V_{Rlth}</math>: changed value from <math>1.15\text{ V}</math> to <math>0.9\text{ V}</math> in <a href="#">Equation 1</a></li> </ul> <p>Added <a href="#">Section 4: Package and PCB thermal data</a></p> <p>Changed <a href="#">Section 5.1: ECOPACK®</a></p>



**Table 12. Document revision history (continued)**

Date	Revision	Changes
09-Jun-2009	7	Changed document title <i>Table 5: General</i> – $I_{\text{oth\_H}}$ , $I_{\text{oth\_L}}$ : added test condition Updated <i>Figure 4: Output voltage vs. <math>V_S</math></i> <i>Section 3.3: Early warning</i> – changed internal voltage reference typical value from 1.23 V to 2.5 V Updated <i>Figure 28: PowerSSO-12 thermal impedance junction ambient single pulse</i> Updated <i>Figure 32: SO-8 thermal impedance junction ambient single pulse</i>
04-Dec-2009	8	Updated features list. Updated <i>Table 2: Pins description</i> . Updated <i>Section 3.1: Voltage regulator</i> . Corrected <i>Equation 3</i> on <i>Section 3.2: Reset</i> .
26-Mar-2010	9	Updated <i>Table 5: General</i> : – $I_{\text{qn\_1}}$ , $I_{\text{qn\_150}}$ : removed test condition $E_n = \text{high}$ .
12-Apr-2010	10	<i>Table 4: Thermal data</i> : – $R_{\text{thj-amb}}$ : updated PowerSSO-12 value

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