



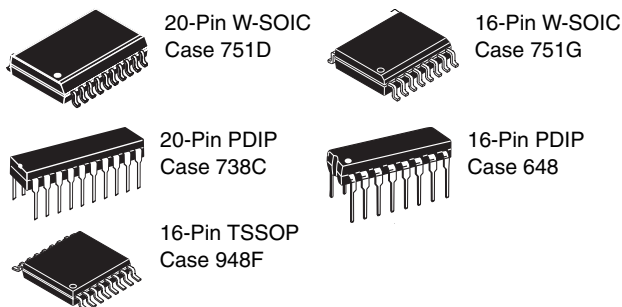
MC9RS08KA8

MC9RS08KA8 Series

Covers: **MC9RS08KA8**
MC9RS08KA4

Features:

- 8-Bit RS08 Central Processor Unit (CPU)
 - Up to 20 MHz CPU at 1.8 V to 5.5 V across temperature range of -40°C to 85°C
 - Subset of HC08 instruction set with added BGND instruction
- On-Chip Memory
 - 8 KB flash read/program/erase over full operating voltage and temperature; KA4 has 4 KB flash
 - 254 byte random-access memory (RAM); KA4 has 126 byte RAM
 - Security circuitry to prevent unauthorized access to RAM and flash contents
- Power-Saving Modes
 - Wait and stop
 - Wakeup from power-saving modes using real-time interrupt (RTI), KBI, or ACMP
- Clock Source Options
 - Oscillator (XOSC) — Loop-Control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 39.0625 kHz or 1 MHz to 5 MHz
 - Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supports bus frequencies up to 10 MHz
- System Protection
 - Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock
 - Low-Voltage detection with reset or interrupt
 - Illegal opcode detection with reset
 - Illegal address detection with reset
 - Flash block protection
- Development Support
 - Single-Wire background debug interface
 - Breakpoint capability to allow single breakpoint setting during in-circuit debugging
- Peripherals
 - **ADC** — 12-channel, 10-bit resolution; 2.5 μs conversion time; automatic compare function; operation in stop; fully functional from 2.7 V to 5.5 V (8-channels available on 16-pin package)
 - **TPM** — One 2-channel; selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel
 - **IIC** — Inter-Integrated circuit bus module capable of operation up to 100 kbps with maximum bus loading; capable of higher baudrates with reduced loading
 - **MTIM1 and MTIM2** — Two 8-bit modulo timers
 - **KBI** — Keyboard interrupts with rising or falling edge detect; eight KBI ports in 16-pin and 20-pin packages
 - **ACMP** — Analog comparator: full rail-to-rail supply operation; option to compare to fixed internal bandgap reference voltage; can operate in stop mode
- Input/Output
 - 14/18 GPIOs including one output only pin and one input only pin
 - Hysteresis and configurable pullup device on all input pins; configurable slew rate and drive strength on all output pins
- Package Options
 - 16-pin SOIC, PDIP or TSSOP
 - 20-pin SOIC or PDIP



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Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

<http://freescale.com/>

The following revision history table summarizes changes contained in this document.

| Revision | Date | Description of Changes |
|----------|-----------|---|
| 1 | 1/22/2008 | Initial public release |
| 2 | 10/7/2008 | Updated Figure 4 and Figure 10 . Updated "How to Reach Us" information. Added 16-pin TSSOP package information. |
| 3 | 11/4/2008 | Updated operating voltage in Table 7 . |
| 4 | 6/11/2009 | Added output voltage of high drive at 5 V, $I_{load} = 10$ mA in the Table 7 . |

Related Documentation

Find the most current versions of all documents at: <http://www.freescale.com>

Reference Manual (MC9RS08KA8RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

1 MCU Block Diagram

The block diagram, [Figure 1](#), shows the structure of the MC9RS08KA8 MCU.

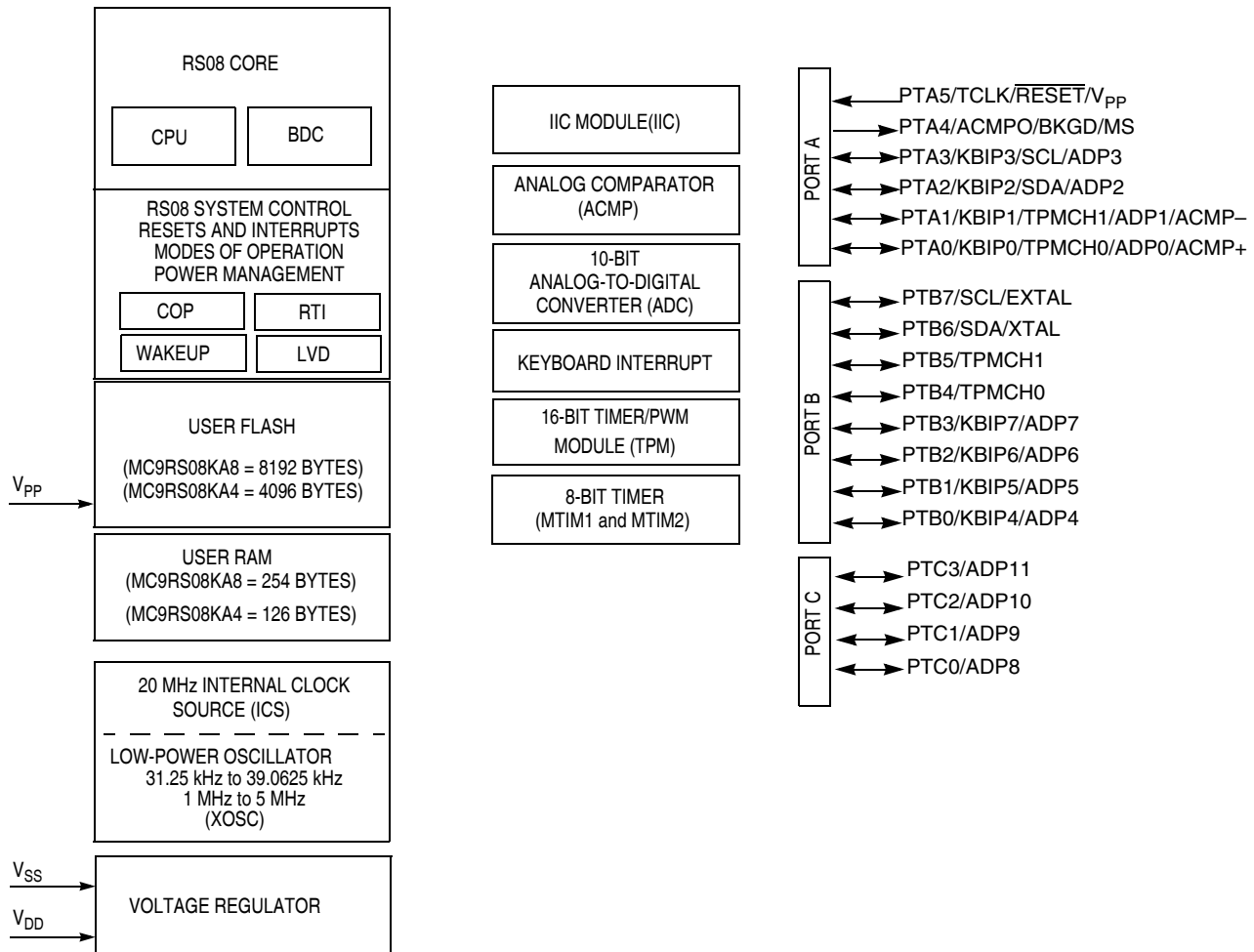


Figure 1. MC9RS08KA8 Series Block Diagram

2 Pin Assignments

This section shows the pin assignments in the packages available for the MC9RS08KA8 series.

Table 1. Pin Availability by Package Pin-Count

| Pin Number | | <-- Lowest Priority --> Highest | | | | |
|------------|----|---------------------------------|---------------------|---------------------|---------------------------|-----------------|
| 20 | 16 | Port Pin | Alt 1 | Alt 2 | Alt 3 | Alt 4 |
| 1 | 1 | PTA5 | | TCLK | $\overline{\text{RESET}}$ | V _{PP} |
| 2 | 2 | PTA4 | ACMPO | BKGD | MS | |
| 3 | 3 | | | | | V _{DD} |
| 4 | 4 | | | | | V _{SS} |
| 5 | 5 | PTB7 | SCL ¹ | | | EXTAL |
| 6 | 6 | PTB6 | SDA ¹ | | | XTAL |
| 7 | 7 | PTB5 | TPMCH1 ² | | | |
| 8 | 8 | PTB4 | TPMCH0 ² | | | |
| 9 | — | PTC3 | | | ADP11 | |
| 10 | — | PTC2 | | | ADP10 | |
| 11 | — | PTC1 | | | ADP9 | |
| 12 | — | PTC0 | | | ADP8 | |
| 13 | 9 | PTB3 | KBIP7 | | ADP7 | |
| 14 | 10 | PTB2 | KBIP6 | | ADP6 | |
| 15 | 11 | PTB1 | KBIP5 | | ADP5 | |
| 16 | 12 | PTB0 | KBIP4 | | ADP4 | |
| 17 | 13 | PTA3 | KBIP3 | SCL ¹ | ADP3 | |
| 18 | 14 | PTA2 | KBIP2 | SDA ¹ | ADP2 | |
| 19 | 15 | PTA1 | KBIP1 | TPMCH1 ² | ADP1 | ACMP- |
| 20 | 16 | PTA0 | KBIP0 | TPMCH0 ² | ADP0 | ACMP+ |

¹ IIC pins can be remapped to PTA3 and PTA2

² TPM pins can be remapped to PTA0 and PTA1

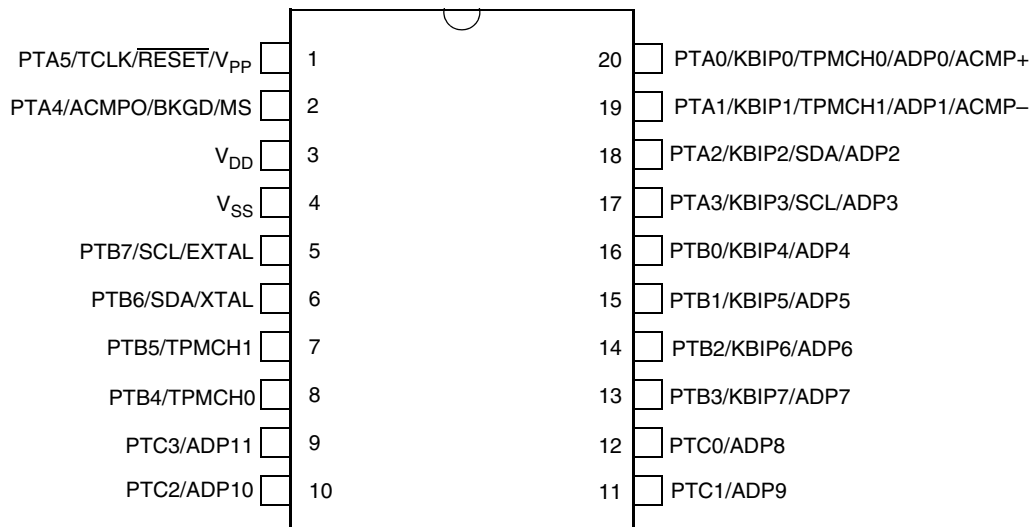


Figure 2. MC9RS08KA8 Series in 20-Pin PDIP/SOIC Package

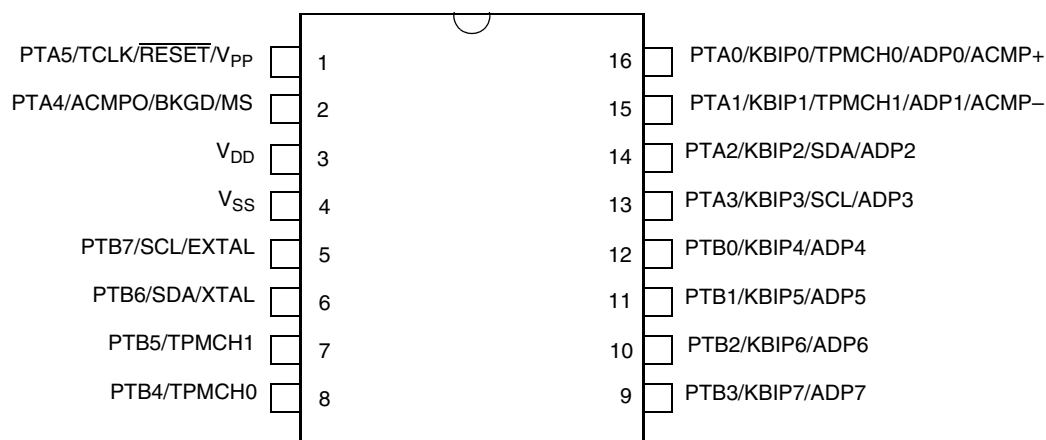


Figure 3. MC9RS08KA8 Series in 16-Pin PDIP/SOIC/TSSOP Package

3 Electrical Characteristics

3.1 Introduction

This chapter contains electrical and timing specifications for the MC9RS08KA8 series of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

| | |
|----------|--|
| P | Those parameters are guaranteed during production testing on each individual device. |
| C | Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations. |
| T | Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category. |
| D | Those parameters are derived mainly from simulations. |

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 3 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this chapter.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 3. Absolute Maximum Ratings

| Rating | Symbol | Value | Unit |
|---|-----------|------------------------|------|
| Supply voltage | V_{DD} | -0.3 to 5.8 | V |
| Maximum current into V_{DD} | I_{DD} | 120 | mA |
| Digital input voltage | V_{In} | -0.3 to $V_{DD} + 0.3$ | V |
| Instantaneous maximum current Single pin limit (applies to all port pins) ^{1, 2, 3} | I_D | ± 25 | mA |
| Storage temperature range | T_{stg} | -55 to 150 | °C |

¹ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

² All functional non-supply pins are internally clamped to V_{SS} and V_{DD} except the \overline{RESET}/V_{PP} pin which is internally clamped to V_{SS} only.

³ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 4. Thermal Characteristics

| Rating | Symbol | Value | Unit |
|--|---------------|-----------------------------|------|
| Operating temperature range (packaged) | T_A | T_L to T_H -40 to 85 | °C |
| Maximum junction temperature | T_{JMAX} | 105 | °C |
| Thermal resistance 16-pin PDIP | θ_{JA} | 80 | °C/W |
| Thermal resistance 16-pin SOIC | θ_{JA} | 112 | °C/W |

Table 4. Thermal Characteristics (continued)

| Rating | Symbol | Value | Unit |
|---------------------------------|---------------|-------|------|
| Thermal resistance 16-pin TSSOP | θ_{JA} | 75 | °C/W |
| Thermal resistance 20-pin PDIP | θ_{JA} | 75 | °C/W |
| Thermal resistance 20-pin SOIC | θ_{JA} | 96 | °C/W |

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \text{Eqn. 1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C /W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts chip internal power

$P_{I/O}$ = Power dissipation on input and output pins user determined

For most applications, $P_{I/O} \ll P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273^\circ\text{C}) \quad \text{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273^\circ\text{C}) + \theta_{JA} \times (P_D)^2 \quad \text{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving equations 1 and 2 iteratively for any value of T_A .

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions must be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 5. ESD and Latch-up Test Conditions

| Model | Description | Symbol | Value | Unit |
|------------|-----------------------------|--------|-------|----------|
| Human Body | Series resistance | R1 | 1500 | Ω |
| | Storage capacitance | C | 100 | pF |
| | Number of pulses per pin | — | 3 | — |
| Machine | Series resistance | R1 | 0 | Ω |
| | Storage capacitance | C | 200 | pF |
| | Number of pulses per pin | — | 3 | — |
| Latch-up | Minimum input voltage limit | — | -2.5 | V |
| | Maximum input voltage limit | — | 7.5 | V |

Table 6. ESD and Latch-Up Protection Characteristics

| No. | Rating ¹ | Symbol | Min | Max | Unit |
|-----|--|-----------|-------------|-----|------|
| 1 | Human body model (HBM) | V_{HBM} | ± 2000 | — | V |
| 2 | Machine model (MM) | V_{MM} | ± 200 | — | V |
| 3 | Charge device model (CDM) | V_{CDM} | ± 500 | — | V |
| 4 | Latch-up current at $T_A = 85^\circ\text{C}$ (applies to all pins except pin 9 PTC3/ADP11) | I_{LAT} | $\pm 100^2$ | — | mA |
| | Latch-up current at $T_A = 85^\circ\text{C}$ (applies to pin 9 PTC3/ADP11) | I_{LAT} | $\pm 75^3$ | — | mA |

¹ Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

² These pins meet JESD78A Class II (section 1.2) Level A (section 1.3) requirement of $\pm 100\text{mA}$.

³ This pin meets JESD78A Class II (section 1.2) Level B (section 1.3) characterization to $\pm 75\text{mA}$. This pin is only present on 20 pin package types.

3.6 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 7. DC Characteristics (Temperature Range = -40 to 85°C Ambient)

| Parameter | Symbol | Min | Typical | Max | Unit |
|---|-------------|--------------|--------------|--------------|------|
| Supply voltage (run, wait and stop modes.) $0 < f_{Bus} < 10\text{MHz}$ V_{DD} rising V_{DD} falling | V_{DD} | 2.0 1.8 | — | 5.5 | V |
| Minimum RAM retention supply voltage applied to V_{DD} | V_{RAM} | 0.8^1 | — | — | V |
| Low-voltage Detection threshold (V_{DD} falling) (V_{DD} rising) | V_{LVD} | 1.80 1.88 | 1.86 1.94 | 1.95 2.03 | V |
| Power on RESET (POR) voltage | V_{POR}^1 | 0.9 | — | 1.7 | V |

Table 7. DC Characteristics (Temperature Range = –40 to 85°C Ambient) (continued)

| Parameter | Symbol | Min | Typical | Max | Unit |
|---|-------------|----------------------|---------|----------------------|-----------|
| Input high voltage ($V_{DD} > 2.3V$) (all digital inputs) | V_{IH} | $0.70 \times V_{DD}$ | — | — | V |
| Input high voltage ($1.8 V \leq V_{DD} \leq 2.3 V$) (all digital inputs) | V_{IH} | $0.85 \times V_{DD}$ | — | — | V |
| Input low voltage ($V_{DD} > 2.3 V$) (all digital inputs) | V_{IL} | — | — | $0.30 \times V_{DD}$ | V |
| Input low voltage ($1.8 V \leq V_{DD} \leq 2.3 V$) (all digital inputs) | V_{IL} | — | — | $0.30 \times V_{DD}$ | V |
| Input hysteresis (all digital inputs) | V_{hys}^1 | $0.06 \times V_{DD}$ | — | — | V |
| Input leakage current (per pin) $V_{In} = V_{DD}$ or V_{SS} , all input only pins | I_{InI} | — | 0.025 | 1.0 | μA |
| High impedance (off-state) leakage current (per pin) $V_{In} = V_{DD}$ or V_{SS} , all input/output | I_{IoZ} | — | 0.025 | 1.0 | μA |
| Internal pullup resistors ² (all port pins) | R_{PU} | 20 | 45 | 65 | $k\Omega$ |
| Internal pulldown resistors ² (all port pins except PTA5) | R_{PD} | 20 | 45 | 65 | $k\Omega$ |
| PTA5 Internal pulldown resistor | — | 45 | — | 95 | $k\Omega$ |
| Output high voltage — Low Drive (PTxDSn = 0) 5 V, $I_{Load} = 2$ mA 3 V, $I_{Load} = 1$ mA 1.8 V, $I_{Load} = 0.5$ mA | V_{OH} | $V_{DD} - 0.8$ | — | — | V |
| Output high voltage — High Drive (PTxDSn = 1) 5 V, $I_{Load} = 10$ mA 5 V, $I_{Load} = 5$ mA 3 V, $I_{Load} = 3$ mA 1.8 V, $I_{Load} = 2$ mA | | $V_{DD} - 0.8$ | — | — | |
| Maximum total I_{OH} for all port pins | I_{OHT} | — | — | 40 | mA |
| Output low voltage — Low Drive (PTxDSn = 0) 5 V, $I_{Load} = 2$ mA 3 V, $I_{Load} = 1$ mA 1.8 V, $I_{Load} = 0.5$ mA | V_{OL} | — | — | 0.8 | V |
| Output low voltage — High Drive (PTxDSn = 1) 5 V, $I_{Load} = 10$ mA 5 V, $I_{Load} = 5$ mA 3 V, $I_{Load} = 3$ mA 1.8 V, $I_{Load} = 2$ mA | | — | — | 0.8 | |
| Maximum total I_{OL} for all port pins | I_{OLT} | — | — | 40 | mA |
| DC injection current ^{3, 4, 5, 6} $V_{In} < V_{SS}$, $V_{In} > V_{DD}$ Single pin limit Total MCU limit, includes sum of all stressed pins | | — | — | 0.2 0.8 | mA |
| Input capacitance (all non-supply pins) | C_{In} | — | — | 7 | pF |

¹ This parameter is characterized and not tested on each device.

² Measurement condition for pull resistors: $V_{In} = V_{SS}$ for pullup and $V_{In} = V_{DD}$ for pulldown.

³ All functional non-supply pins are internally clamped to V_{SS} and V_{DD} except the \overline{RESET}/V_{PP} which is internally clamped to V_{SS} only.

⁴ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

⁵ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

⁶ This parameter is characterized and not tested on each device.

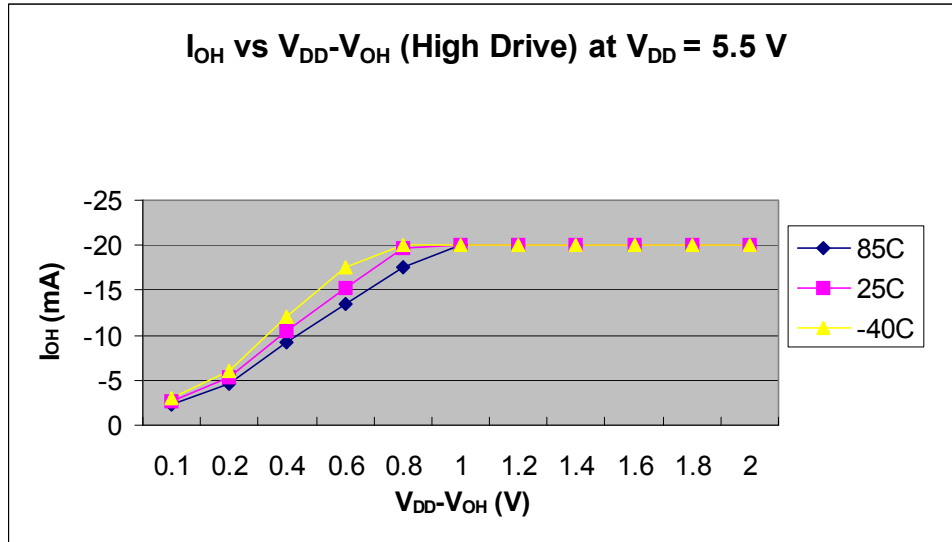


Figure 4. Typical IOH vs. VDD-VOH
VDD = 5.5 V (High Drive)

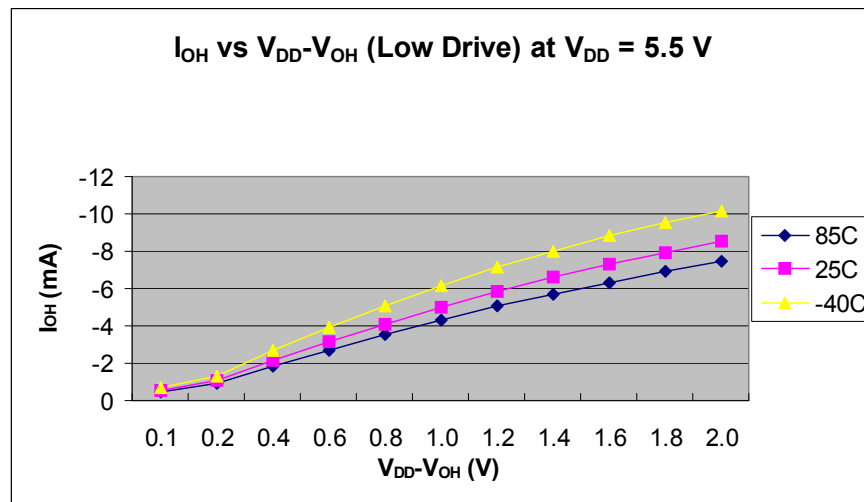


Figure 5. Typical IOH vs. VDD-VOH
VDD = 5.5 V (Low Drive)

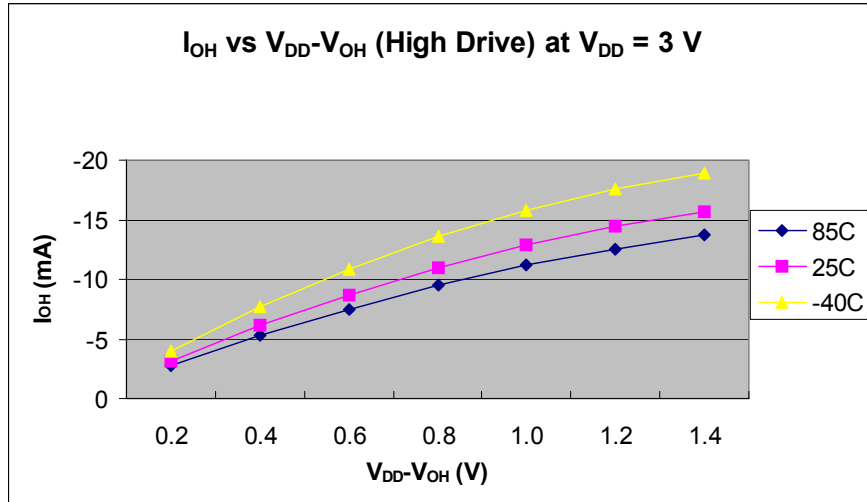


Figure 6. Typical I_{OH} vs. $V_{DD}-V_{OH}$
 $V_{DD} = 3\text{ V}$ (High Drive)

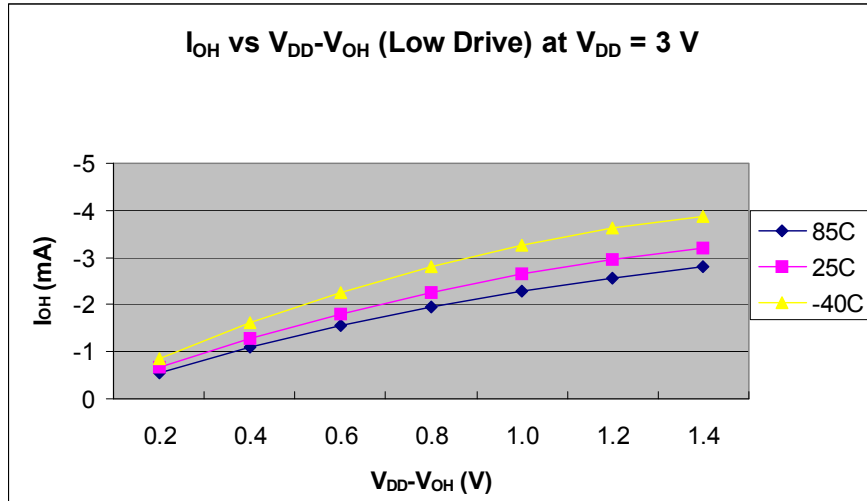


Figure 7. Typical I_{OH} vs. $V_{DD}-V_{OH}$
 $V_{DD} = 3\text{ V}$ (Low Drive)

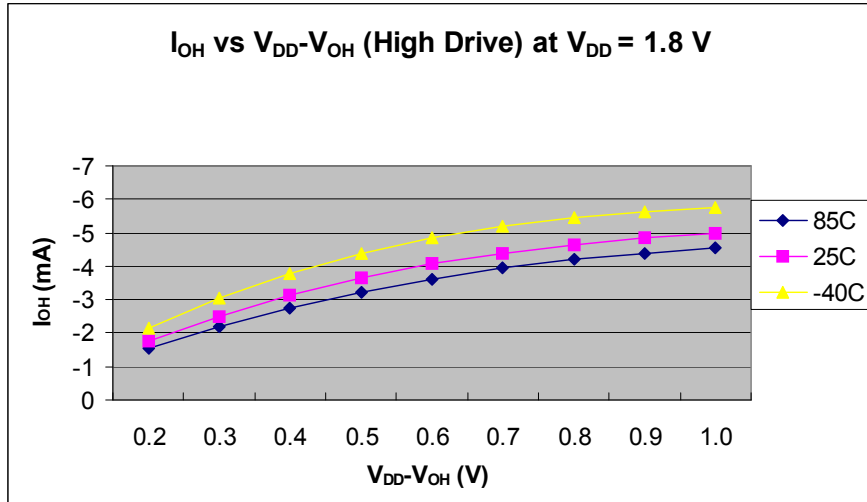


Figure 8. Typical I_{OH} vs. $V_{DD}-V_{OH}$
 $V_{DD} = 1.8$ V (High Drive)

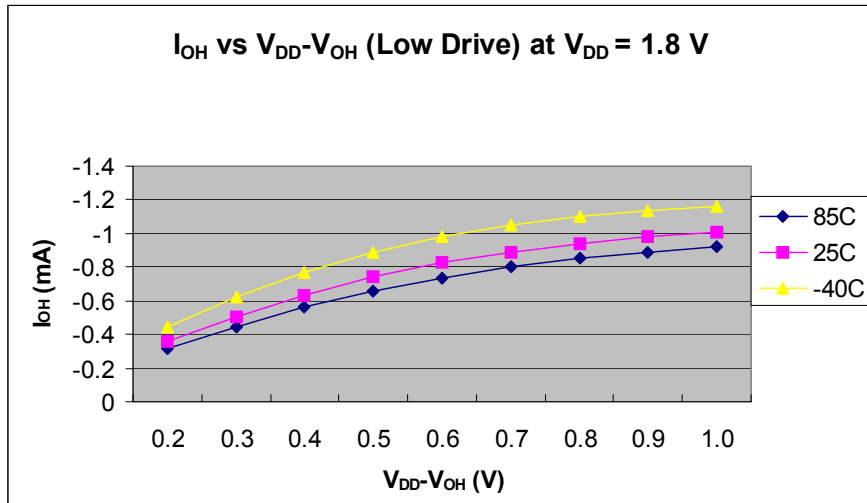


Figure 9. Typical I_{OH} vs. $V_{DD}-V_{OH}$
 $V_{DD} = 1.8$ V (Low Drive)

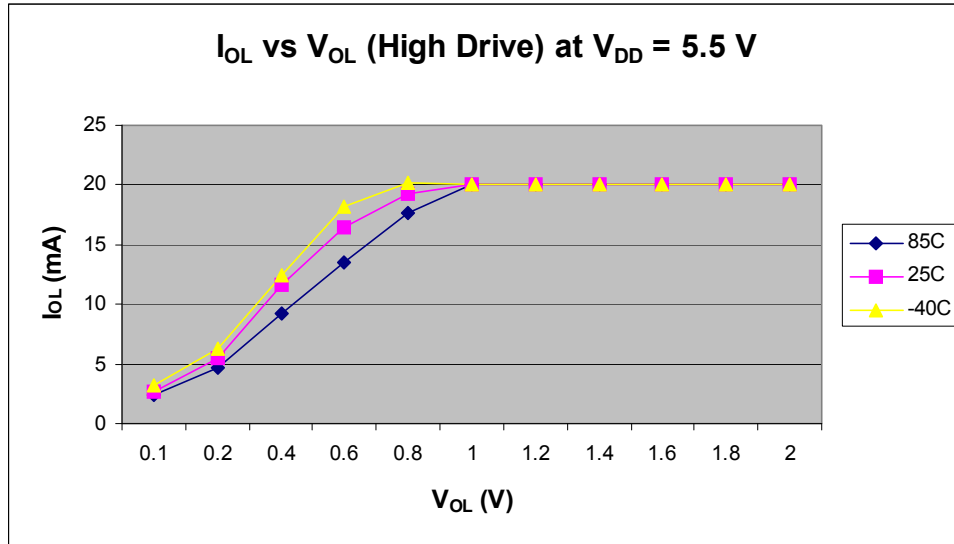


Figure 10. Typical I_{OL} vs. V_{DD}-V_{OL}
V_{DD} = 5.5 V (High Drive)

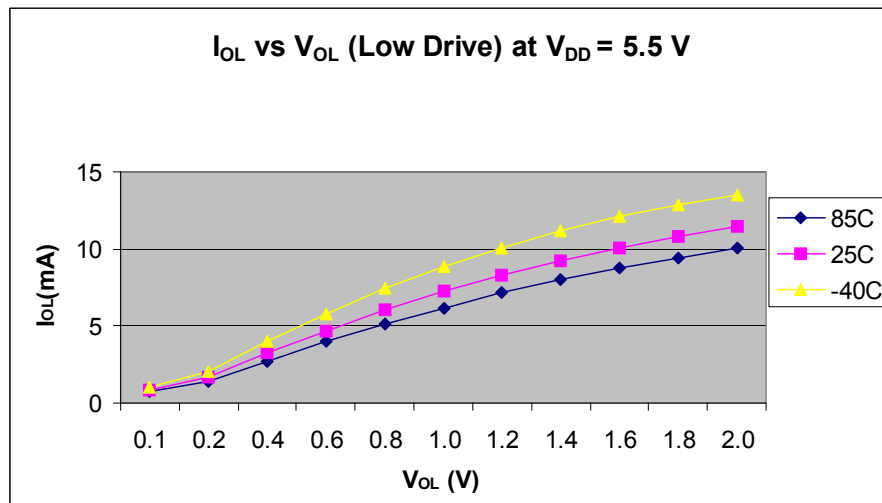


Figure 11. Typical I_{OL} vs. V_{DD}-V_{OL}
V_{DD} = 5.5 V (Low Drive)

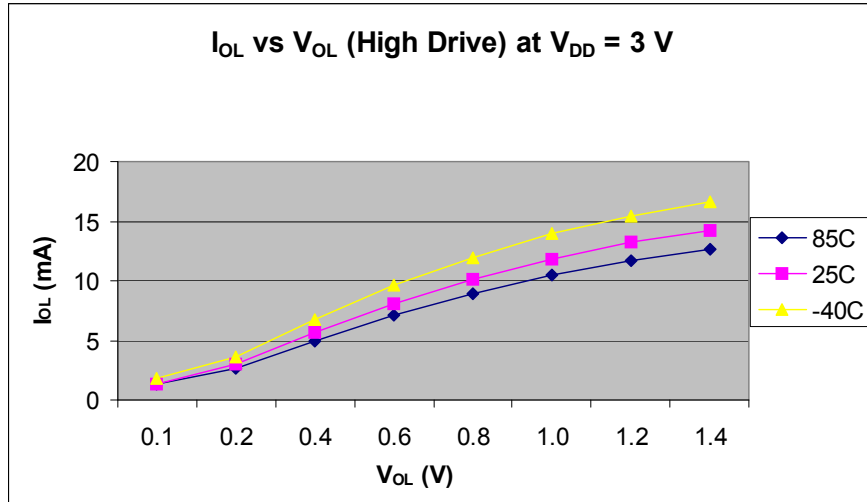


Figure 12. Typical I_{OL} vs. V_{DD}-V_{OL}
V_{DD} = 3 V (High Drive)

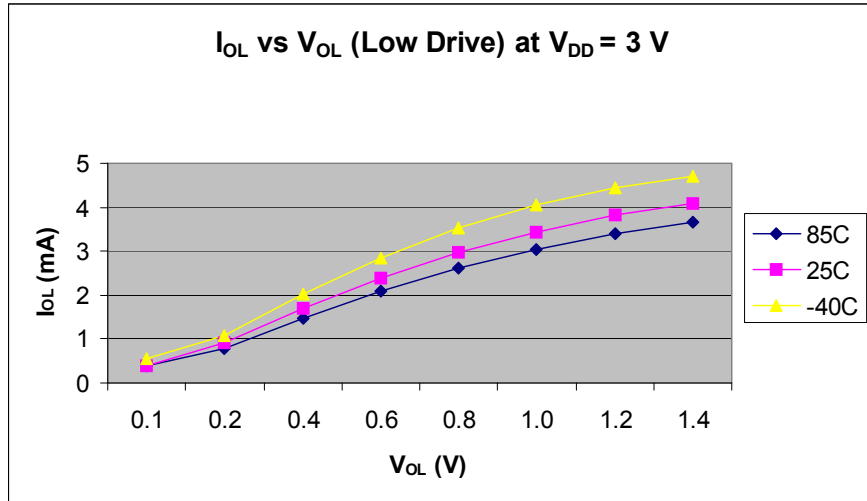


Figure 13. Typical I_{OL} vs. V_{DD}-V_{OL}
V_{DD} = 3 V (Low Drive)

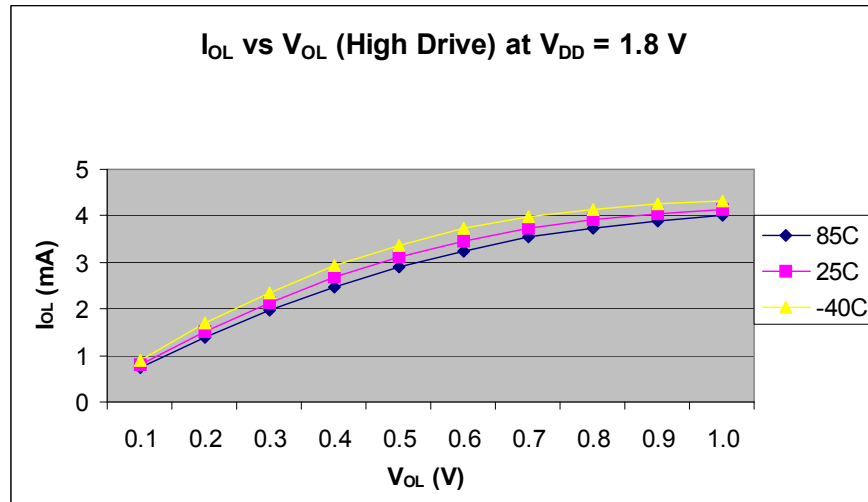


Figure 14. Typical I_{OL} vs. $V_{DD}-V_{OL}$
 $V_{DD} = 1.8$ V (High Drive)

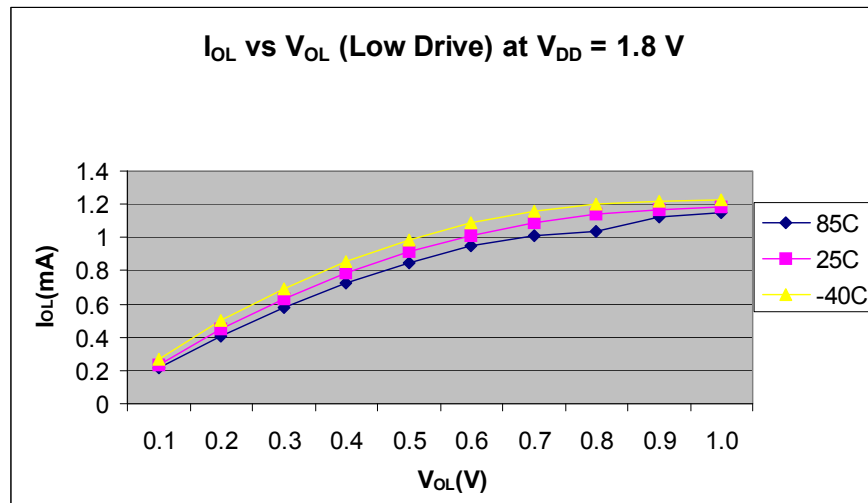


Figure 15. Typical I_{OL} vs. $V_{DD}-V_{OL}$
 $V_{DD} = 1.8$ V (Low Drive)

3.7 Supply Current Characteristics

Table 8. Supply Current Characteristics

| Parameter | Symbol | V_{DD} (V) | Typical ¹ | Max ² | Temp. (°C) |
|--|-------------|--------------|----------------------|------------------|------------|
| Run supply current ³ measured at ($f_{Bus} = 10$ MHz) | R_{IDD10} | 5 | 2.4 mA | 5 mA | 25 85 |
| | | 3 | 2.4 mA | — | 25 85 |
| | | 1.80 | 1.7 mA | — | 25 85 |

Table 8. Supply Current Characteristics (continued)

| Parameter | Symbol | V _{DD} (V) | Typical ¹ | Max ² | Temp. (°C) |
|--|-------------------|---------------------|----------------------|------------------|------------|
| Run supply current ³ measured at (f _{Bus} = 1.25 MHz) | R _{IDD1} | 5 | 0.42 mA | 2 mA | 25 85 |
| | | 3 | 0.42 mA | — | 25 85 |
| | | 1.80 | 0.3 mA | — | 25 85 |
| Stop mode supply current | S _{IDD} | 5 | 2.4 μA | 5 μA 8 μA | 25 85 |
| | | 3 | 2 μA | — | 25 85 |
| | | 1.80 | 1.5 μA | — | 25 85 |
| ADC adder from stop ⁴ | — | 5 | 128 μA | 150 μA 165 μA | 25 85 |
| | | 3 | 121 μA | — | 25 85 |
| | | 1.80 | 79 μA | — | 25 85 |
| ACMP adder from stop (ACME = 1) | — | 5 | 21 μA | 22 μA | 25 85 |
| | | 3 | 18.5 μA | — | 25 85 |
| | | 1.80 | 17.5 μA | — | 25 85 |
| RTI adder from stop with 1 kHz clock source enabled ⁵ | — | 5 | 2.4 μA | 2 μA | 25 85 |
| | | 3 | 1.9 μA | — | 25 85 |
| | | 1.80 | 1.5 μA | — | 25 85 |
| RTI adder from stop with 1 MHz external clock source reference enabled | — | 5 | 2.1 μA | 2 μA | 25 85 |
| | | 3 | 1.6 μA | — | 25 85 |
| | | 1.80 | 1.2 μA | — | 25 85 |
| LVI adder from stop (LVDE=1 and LVDSE=1) | — | 5 | 70 μA | 80 μA | 25 85 |
| | | 3 | 65 μA | — | 25 85 |
| | | 1.80 | 60 μA | — | 25 85 |

¹ Typicals are measured at 25°C.

² Maximum value is measured at the nominal V_{DD} voltage times 10% tolerance. Values given here are preliminary estimates prior to completing characterization.

³ Not include any DC loads on port pins.

⁴ Required asynchronous ADC clock and LVD to be enabled.

⁵ Most customers are expected to find that auto-wakeup from stop can be used instead of the higher current wait mode. Wait mode typical is 1.3 mA at 3 V and 1 mA at 2 V with $f_{Bus} = 1$ MHz.

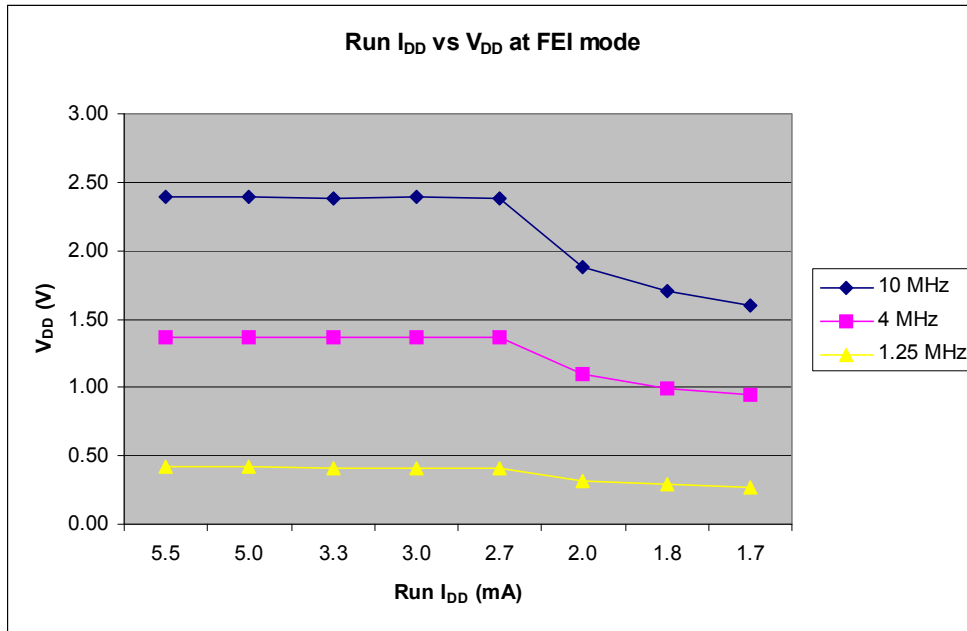


Figure 16. Typical Run I_{DD} vs. V_{DD} for FEI Mode

3.8 External Oscillator (XOSC) Characteristics

Table 9. Oscillator Electrical Specifications (Temperature Range = -40 to 125°C Ambient)

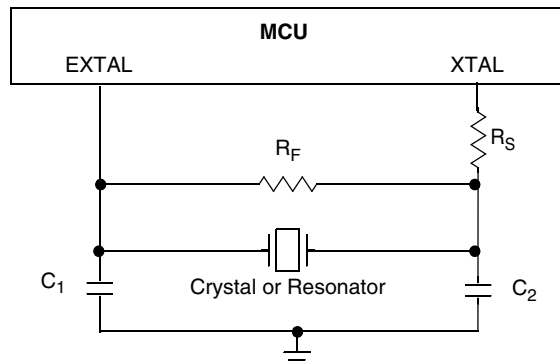
| Num | C | Rating | Symbol | Min | Typical ¹ | Max | Unit |
|-----|---|--|----------------|---|----------------------|------|------------|
| 1 | C | Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) | | | | | |
| | | Low range (RANGE = 0) | f_{lo} | 32 | — | 38.4 | kHz |
| | | High range (RANGE = 1) FEE or FBE mode ² | f_{hi} | 1 | — | 5 | MHz |
| | | High range (RANGE = 1, HGO = 1) FBELP mode | f_{hi-hgo} | 1 | — | 16 | MHz |
| | | High range (RANGE = 1, HGO = 0) FBELP mode | f_{hi-lp} | 1 | — | 8 | MHz |
| 2 | D | Load capacitors | C_1, C_2 | See crystal or resonator manufacturer's recommendation. | | | |
| 3 | D | Feedback resistor | R_F | | | | M Ω |
| | | Low range (32 kHz to 100 kHz) | | — | 10 | — | |
| | | High range (1 MHz to 16 MHz) | | — | 1 | — | |
| 4 | D | Series resistor | R_S | | | | k Ω |
| | | Low range, low gain (RANGE = 0, HGO = 0) | | — | 0 | — | |
| | | Low range, high gain (RANGE = 0, HGO = 1) | | — | 100 | — | |
| | | High range, low gain (RANGE = 1, HGO = 0) | | — | 0 | — | |
| | | High range, high gain (RANGE = 1, HGO = 1) | | — | 0 | — | |
| | | ≥ 8 MHz | — | 0 | 0 | | |
| | | 4 MHz | — | 0 | 10 | | |
| | | 1 MHz | — | 0 | 20 | | |
| 5 | C | Crystal start-up time ³ | | | | | ms |
| | | Low range, low gain (RANGE = 0, HGO = 0) | $t_{CSTL-LP}$ | — | 200 | — | |
| | | Low range, high gain (RANGE = 0, HGO = 1) | $t_{CSTL-HGO}$ | — | 400 | — | |
| | | High range, low gain (RANGE = 1, HGO = 0) ⁴ | $t_{CSTH-LP}$ | — | 5 | — | |
| | | High range, high gain (RANGE = 1, HGO = 1) ⁴ | $t_{CSTH-HGO}$ | — | 20 | — | |
| 6 | D | Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) | f_{extal} | | | | MHz |
| | | FEE or FBE mode ² | | 0.03125 | — | 5 | |
| | | FBELP mode | | 0 | — | 40 | |

¹ Typical data was characterized at 5.0 V, 25 °C or is recommended value.

² The input clock source must be divided using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

³ This parameter is characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications.

⁴ 4 MHz crystal.



3.9 AC Characteristics

This section describes AC timing characteristics for each peripheral system.

3.9.1 Control Timing

Table 10. Control Timing

| Num | C | Parameter | Symbol | Min | Typical | Max | Unit |
|-----|---|--|----------------------|---------------|---------|------|---------|
| 1 | D | Bus frequency ($t_{cyc} = 1/f_{Bus}$) | f_{Bus} | 0 | — | 10 | MHz |
| 2 | D | Real time interrupt internal oscillator period | t_{RTI} | 700 | 1000 | 1300 | μs |
| 3 | D | External \overline{RESET} pulse width ¹ | t_{extrst} | 150 | — | — | ns |
| 4 | D | KBI pulse width ² | t_{KBIPW} | $1.5 t_{cyc}$ | — | — | ns |
| 5 | D | KBI pulse width in stop ¹ | t_{KBIPWS} | 100 | — | — | ns |
| 6 | D | Port rise and fall time (load = 50 pF) ³ | t_{Rise}, t_{Fall} | — | 11 | — | ns |
| | | Slew rate control disabled (PTxSE = 0) | | — | 35 | — | |
| | | Slew rate control enabled (PTxSE = 1) | | | | | |

¹ This is the shortest pulse guaranteed to pass through the pin input filter circuitry. Shorter pulses may or may not be recognized.

² This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

³ Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range $-40^{\circ}C$ to $85^{\circ}C$.

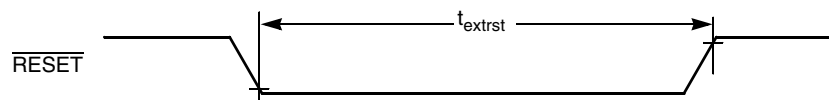


Figure 17. Reset Timing

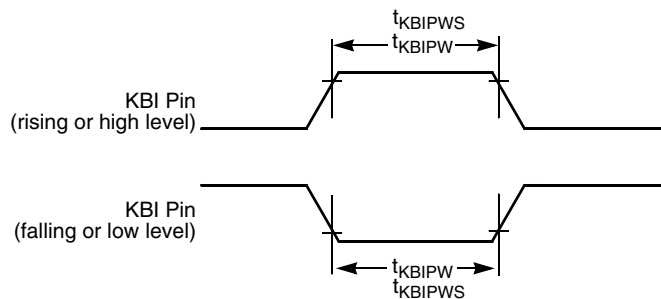


Figure 18. KBI Pulse Width

3.9.2 TPM/MTIM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 11. TPM Input Timing

| Num | C | Rating | Symbol | Min | Max | Unit |
|-----|---|---------------------------|--------------|-----|-------------|-----------|
| 1 | D | External clock frequency | f_{TPMext} | DC | $f_{Bus}/4$ | MHz |
| 2 | D | External clock period | t_{TPMext} | 4 | — | t_{cyc} |
| 3 | D | External clock high time | t_{clkh} | 1.5 | — | t_{cyc} |
| 4 | D | External clock low time | t_{clkl} | 1.5 | — | t_{cyc} |
| 5 | D | Input capture pulse width | t_{ICPW} | 1.5 | — | t_{cyc} |

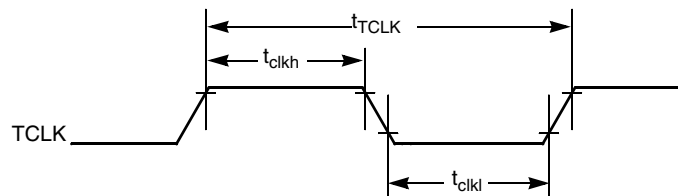


Figure 19. Timer External Clock

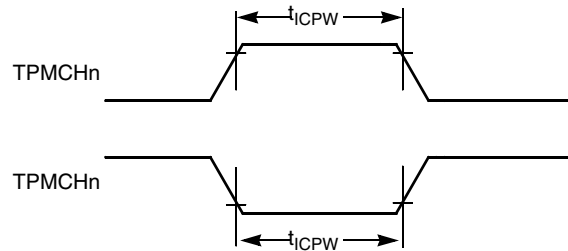


Figure 20. Timer Input Capture Pulse

3.10 Analog Comparator (ACMP) Electrical

Table 12. Analog Comparator Electrical Specifications

| Num | C | Characteristic | Symbol | Min | Typical | Max | Unit |
|-----|---|---|-------------|----------------|---------|----------|-----------|
| 1 | D | Supply voltage | V_{DD} | 1.80 | — | 5.5 | V |
| 2 | P | Supply current (active) | I_{DDAC} | — | 20 | 35 | μA |
| 3 | D | Analog input voltage ¹ | V_{AIN} | $V_{SS} - 0.3$ | — | V_{DD} | V |
| 4 | P | Analog input offset voltage ¹ | V_{AIO} | — | 20 | 40 | mV |
| 5 | C | Analog Comparator hysteresis ¹ | V_H | 3.0 | 9.0 | 15.0 | mV |
| 6 | C | Analog source impedance ¹ | R_{AS} | — | — | 10 | $k\Omega$ |
| 7 | P | Analog input leakage current | I_{ALKG} | — | — | 1.0 | μA |
| 8 | C | Analog Comparator initialization delay | t_{AINIT} | — | — | 1.0 | μs |

Table 12. Analog Comparator Electrical Specifications (continued)

| Num | C | Characteristic | Symbol | Min | Typical | Max | Unit |
|-----|---|---|----------|-----|---------|-----|------|
| 9 | P | Analog Comparator bandgap reference voltage | V_{BG} | 1.1 | 1.208 | 1.3 | V |

¹ These data are characterized but not production tested.

3.11 Internal Clock Source Characteristics

Table 13. Internal Clock Source Specifications

| Num | C | Characteristic | Symbol | Min | Typical ¹ | Max | Unit |
|-----|---|--|--------------------------|-------|----------------------|---------|-------------|
| 1 | C | Average internal reference frequency — untrimmed | f_{int_ut} | 25 | 31.25 | 41.66 | kHz |
| 2 | P | Average internal reference frequency — trimmed | f_{int_t} | 31.25 | 39.06 | 39.0625 | kHz |
| 3 | C | DCO output frequency range — untrimmed | f_{dco_ut} | 12.8 | 16 | 21.33 | MHz |
| 4 | P | DCO output frequency range — trimmed | f_{dco_t} | 16 | 20 | 20 | MHz |
| 5 | C | Resolution of trimmed DCO output frequency at fixed voltage and temperature | $\Delta f_{dco_res_t}$ | — | — | 0.2 | % f_{dco} |
| 6 | C | Total deviation of trimmed DCO output frequency over voltage and temperature | Δf_{dco_t} | — | — | 2 | % f_{dco} |
| 7 | C | FLL acquisition time ^{2,3} | $t_{acquire}$ | — | — | 1 | ms |
| 8 | C | Stop recovery time (FLL wakeup to previous acquired frequency) IREFSTEN = 0 IREFSTEN = 1 | t_{wakeup} | — | 100 86 | — | μ s |

¹ Data in typical column was characterized at 3.0 V and 5.0 V, 25 °C or is typical recommended value.

² This parameter is characterized and not tested on each device.

³ This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBILP) to FLL enabled (FEI, FBI).

3.12 ADC Characteristics

Table 14. 5 Volt 10-bit ADC Operating Conditions

| C | Characteristic | Conditions | Symb | Min. | Typical | Max. | Unit |
|---|--|---|------------|----------|---------|----------|------------|
| D | Input voltage | — | V_{ADIN} | V_{SS} | — | V_{DD} | V |
| C | Accuracy | $V_{DD} = 2$ V | — | — | 8 bit | — | — |
| C | Input capacitance | — | C_{ADIN} | — | 4.5 | 5.5 | pF |
| C | Input resistance | — | R_{ADIN} | — | 3 | 5 | k Ω |
| C | Analog source resistance external to MCU | 10 bit mode $f_{ADCK} > 4$ MHz $f_{ADCK} < 4$ MHz | R_{AS} | — | — | 5 | k Ω |
| | | 8 bit mode (all valid f_{ADCK}) | | — | — | 10 | |

Table 14. 5 Volt 10-bit ADC Operating Conditions (continued)

| C | Characteristic | Conditions | Symb | Min. | Typical | Max. | Unit |
|---|--------------------------------|----------------------|------------|------|---------|------|------|
| D | ADC conversion clock frequency | High Speed (ADLPC=0) | f_{ADCK} | 0.4 | — | 8.0 | MHz |
| | | Low Power (ADLPC=1) | | 0.4 | — | 8.0 | |

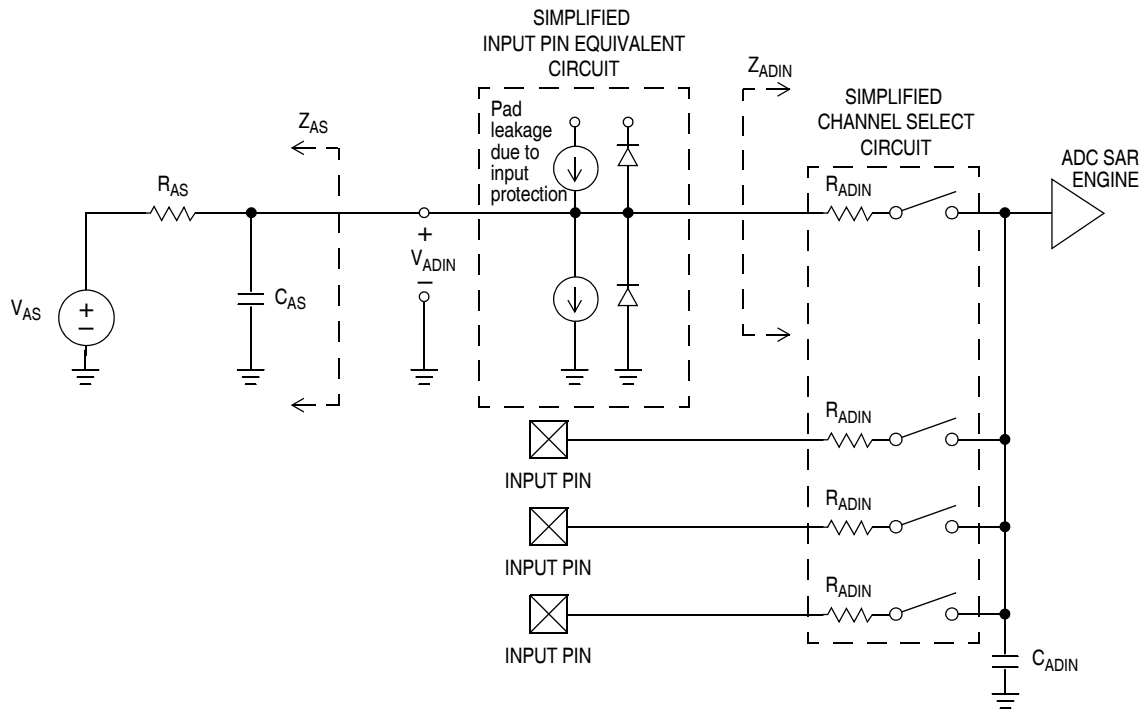


Figure 21. ADC Input Impedance Equivalency Diagram

Table 15. 10-bit ADC Characteristics

| Characteristic | Conditions | C | Symb | Min | Typical ¹ | Max | Unit |
|---|------------|---|------------|-----|----------------------|-----|---------|
| Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1 | — | T | I_{DDAD} | — | 133 | — | μA |
| Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1 | — | T | I_{DDAD} | — | 218 | — | μA |
| Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1 | — | T | I_{DDAD} | — | 327 | — | μA |
| Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1 | — | C | I_{DDAD} | — | 0.582 | 1 | mA |

Table 15. 10-bit ADC Characteristics (continued)

| Characteristic | Conditions | C | Symb | Min | Typical ¹ | Max | Unit |
|--|--|---|--------------------|-----|----------------------|------|------------------|
| Supply current | Stop, reset, module off | T | I _{DDAD} | — | 0.011 | 1 | μA |
| ADC asynchronous clock source | High speed (ADLPC = 0) | T | f _{ADACK} | — | 3.3 | — | MHz |
| | Low power (ADLPC = 1) | | | — | 2 | — | |
| Conversion time (including sample time) | Short sample (ADLSMP=0) | P | t _{ADC} | — | 20 | — | ADCK cycles |
| | Long sample (ADLSMP=1) | | | — | 40 | — | |
| Sample time | Short sample (ADLSMP=0) | P | t _{ADS} | — | 3.5 | — | ADCK cycles |
| | Long sample (ADLSMP=1) | | | — | 23.5 | — | |
| Total unadjusted error | 10 bit mode | C | E _{TUE} | — | ±1 | ±2.5 | LSB ² |
| | 8 bit mode | | | — | ±0.5 | ±1.0 | |
| Differential non-linearity | 10 bit mode | P | DNL | — | ±0.5 | ±1.0 | LSB ² |
| | 8 bit mode | T | | — | ±0.3 | ±0.5 | |
| | Monotonicity and No-Missing-Codes guaranteed | | | | | | |
| Integral non-linearity | 10 bit mode | C | INL | — | ±0.5 | ±1.0 | LSB ² |
| | 8 bit mode | | | — | ±0.3 | ±0.5 | |
| Zero-scale error | 10 bit mode | P | E _{ZS} | — | ±0.5 | ±1.5 | LSB ² |
| | 8 bit mode | T | | — | ±0.5 | ±0.5 | |
| Full-Scale error V _{ADIN} = V _{DDA} | 10 bit mode | P | E _{FS} | — | ±0.5 | ±1.5 | LSB ² |
| | 8 bit mode | T | | — | ±0.5 | ±0.5 | |
| Quantization error | 10 bit mode | D | E _Q | — | — | ±0.5 | LSB ² |
| | 8 bit mode | | | — | — | ±0.5 | |
| Input leakage error pad leakage ³ * RAS | 10 bit mode | D | E _{IL} | — | ±0.2 | ±2.5 | LSB ² |
| | 8 bit mode | | | — | ±0.1 | ±1 | |

¹ Typical values assume Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

² 1 LSB = (V_{REFH} - V_{REFL})/2^N

³ Based on input pad leakage current. Refer to pad electrical.

3.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory. For detailed information about program/erase operations, see the reference manual.

Table 16. Flash Characteristics

| Characteristic | Symbol | Min | Typical ¹ | Max | Unit |
|----------------------------------|-----------------|-----|----------------------|-----|------|
| Supply voltage for program/erase | V _{DD} | 2.7 | — | 5.5 | V |

Table 16. Flash Characteristics (continued)

| Characteristic | Symbol | Min | Typical ¹ | Max | Unit |
|--|------------------|------|----------------------|------|---------|
| Program/Erase voltage | V_{PP} | 11.8 | 12 | 12.2 | V |
| V_{PP} current | | | | | |
| Program | I_{VPP_prog} | — | — | 200 | μA |
| Mass erase | I_{VPP_erase} | — | — | 100 | μA |
| Supply voltage for read operation $0 < f_{Bus} < 10$ MHz | V_{Read} | 1.8 | — | 5.5 | V |
| Byte program time | t_{prog} | 20 | — | 40 | μs |
| Mass erase time | t_{me} | 500 | — | — | ms |
| Cumulative program HV time ² | t_{hv} | — | — | 8 | ms |
| Total cumulative HV time (total of t_{me} & t_{hv} applied to device) | t_{hv_total} | — | — | 2 | hours |
| HVEN to program setup time | t_{pgs} | 10 | — | — | μs |
| PGM/MASS to HVEN setup time | t_{nvs} | 5 | — | — | μs |
| HVEN hold time for PGM | t_{nvh} | 5 | — | — | μs |
| HVEN hold time for MASS | t_{nvh1} | 100 | — | — | μs |
| V_{PP} to PGM/MASS setup time | t_{vps} | 20 | — | — | ns |
| HVEN to V_{PP} hold time | t_{vph} | 20 | — | — | ns |
| V_{PP} rise time ³ | t_{vrs} | 200 | — | — | ns |
| Recovery time | t_{rcv} | 1 | — | — | μs |
| Program/erase endurance TL to TH = $-40^{\circ}C$ to $85^{\circ}C$ | — | 1000 | — | — | cycles |
| Data retention | t_{D_ret} | 15 | — | — | years |

¹ Typicals are measured at 25 °C.

² t_{hv} is the cumulative high voltage programming time to the same row before next erase. Same address can not be programmed more than twice before next erase.

³ Fast V_{PP} rise time may potentially trigger the ESD protection structure, which may result in over current flowing into the pad and cause permanent damage to the pad. External filtering for the V_{PP} power source is recommended. An example V_{PP} filter is shown in Figure 22.

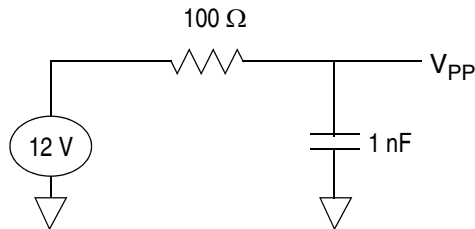
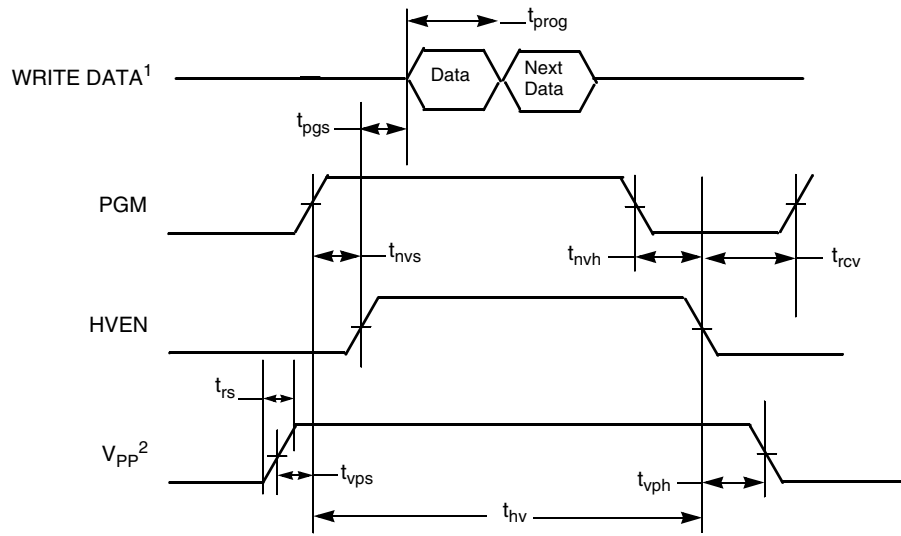
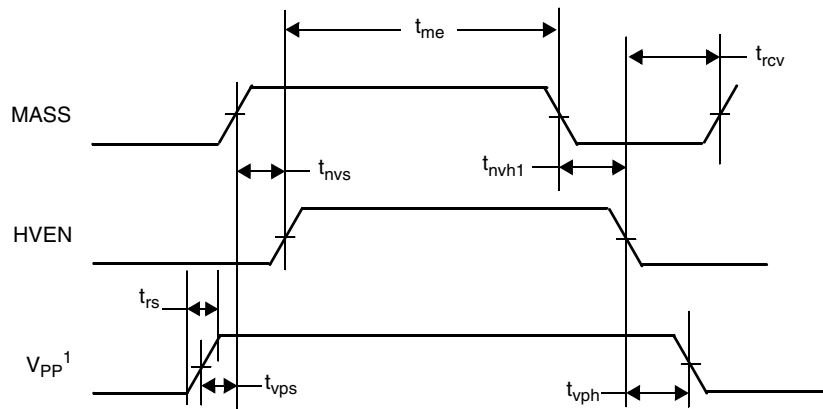


Figure 22. Example V_{PP} Filtering



¹ Next Data applies if programming multiple bytes in a single row, refer to *MC9RS08KA8 Series Reference Manual*.
² V_{DD} must be at a valid operating voltage before voltage is applied or removed from the V_{PP} pin.

Figure 23. Flash Program Timing



¹ V_{DD} must be at a valid operating voltage before voltage is applied or removed from the V_{PP} pin.

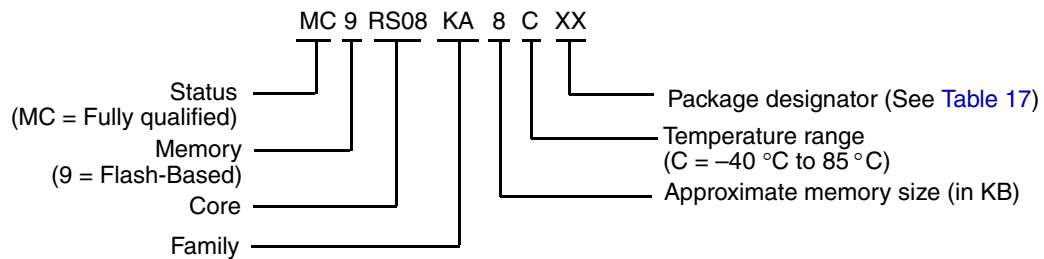
Figure 24. Flash Mass Erase Timing

4 Ordering Information

This section contains ordering numbers for MC9RS08KA8 series devices. See below for an example of the device numbering system.

Table 17. Device Numbering System

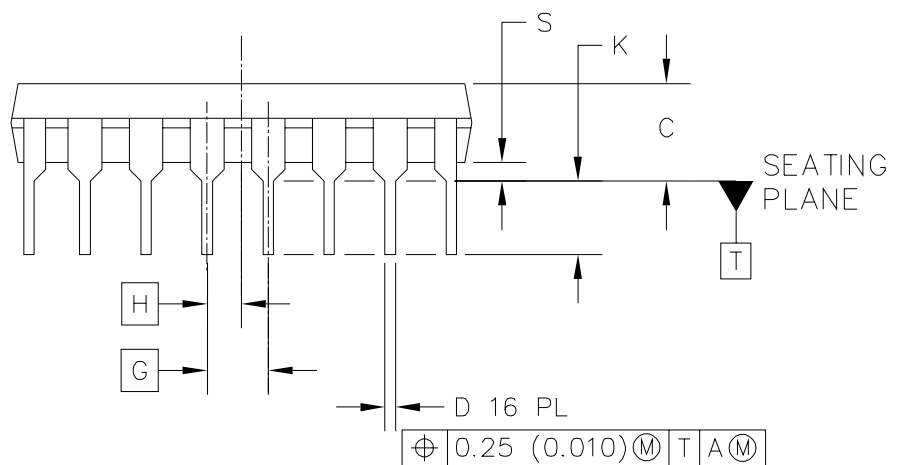
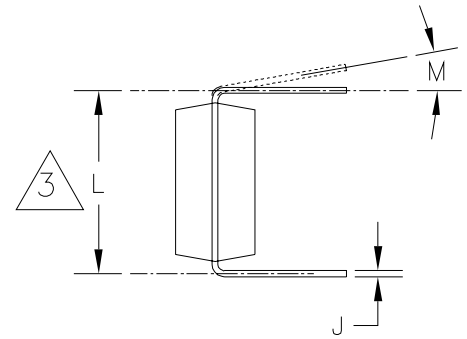
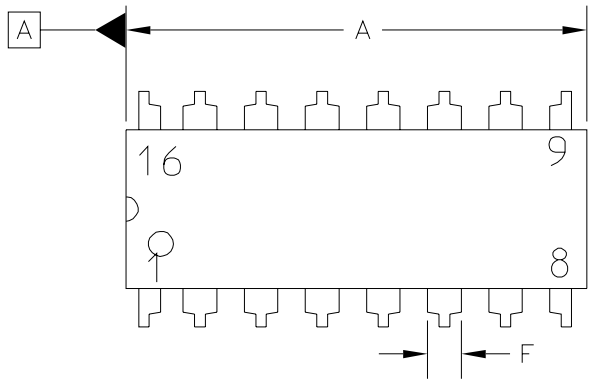
| Device Number | Memory | | Package | | |
|--------------------------|----------------------|------------------------|-----------|------------|--------------|
| | Flash | RAM | Type | Designator | Document No. |
| MC9RS08KA8 MC9RS08KA4 | 8K bytes 4K bytes | 254 bytes 126 bytes | 16 PDIP | PG | 98ASB42431B |
| | | | 16 W-SOIC | WG | 98ASB42567B |
| | | | 16 TSSOP | TG | 98ASH70247A |
| | | | 20 PDIP | PJ | 98ASB42899B |
| | | | 20 W-SOIC | WJ | 98ASB42343B |



5 Mechanical Drawings

The following pages contain mechanical specifications for MC9RS08KA8 series package options.

- 16-pin PDIP (plastic dual in-line pin)
- 16-pin W-SOIC (wide body small outline integrated circuit)
- 16-pin TSSOP (thin shrink sSmall outline package)
- 20-pin PDIP (plastic dual in-line pin)
- 20-pin W-SOIC (wide body small outline integrated circuit)



| | | | |
|---|--------------------------|----------------------------|--|
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| TITLE: 16 LD PDIP | DOCUMENT NO: 98ASB42431B | REV: T | |
| | CASE NUMBER: 648-08 | 19 MAY 2005 | |
| | STANDARD: NON-JEDEC | | |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSIONS DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.
6. 648-01 THRU -08 OBSOLETE, NEW STANDARD 648-09.

| DIM | MILLIMETERS | | INCHES | | DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|-----|-------------|-----|--------|-----|
| | MIN | MAX | MIN | MAX | | MIN | MAX | MIN | MAX |
| A | 18.80 | 19.55 | 0.740 | 0.770 | | | | | |
| B | 6.35 | 6.85 | 0.250 | 0.270 | | | | | |
| C | 3.69 | 4.44 | 0.145 | 0.175 | | | | | |
| D | 0.39 | 0.53 | 0.015 | 0.021 | | | | | |
| F | 1.02 | 1.77 | 0.040 | 0.070 | | | | | |
| G | 2.54 BSC | | 0.100 BSC | | | | | | |
| H | 1.27 BSC | | 0.050 BSC | | | | | | |
| J | 0.21 | 0.38 | 0.008 | 0.015 | | | | | |
| K | 2.80 | 3.30 | 0.110 | 0.130 | | | | | |
| L | 7.50 | 7.74 | 0.295 | 0.305 | | | | | |
| M | 0° | 10° | 0° | 10° | | | | | |
| S | 0.51 | 1.01 | 0.020 | 0.040 | | | | | |

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MECHANICAL OUTLINE

PRINT VERSION NOT TO SCALE

TITLE:

16 LD PDIP

DOCUMENT NO: 98ASB42431B

REV: T

CASE NUMBER: 648-08

19 MAY 2005

STANDARD: NON-JEDEC

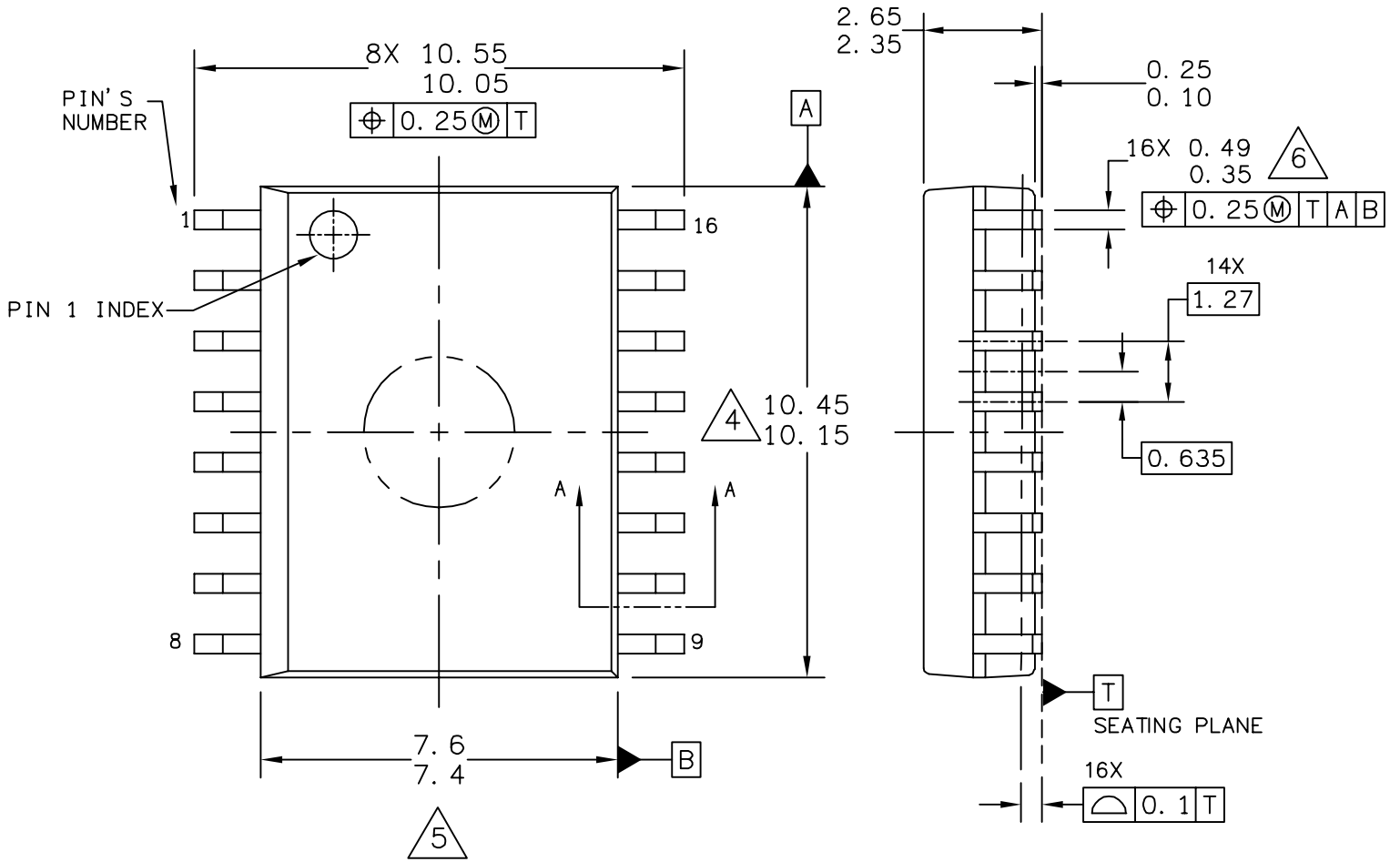
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- 2. CATHODE
- 3. CATHODE
- 4. CATHODE
- 5. CATHODE
- 6. CATHODE
- 7. CATHODE
- 8. CATHODE
- 9. ANODE
- 10. ANODE
- 11. ANODE
- 12. ANODE
- 13. ANODE
- 14. ANODE
- 15. ANODE
- 16. ANODE

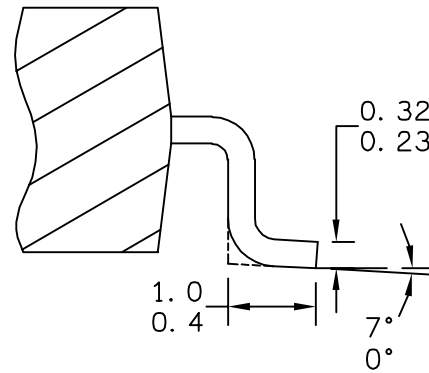
STYLE 2:

- PIN 1. COMMON DRAIN
- 2. COMMON DRAIN
- 3. COMMON DRAIN
- 4. COMMON DRAIN
- 5. COMMON DRAIN
- 6. COMMON DRAIN
- 7. COMMON DRAIN
- 8. COMMON DRAIN
- 9. GATE
- 10. SOURCE
- 11. GATE
- 12. SOURCE
- 13. GATE
- 14. SOURCE
- 15. GATE
- 16. SOURCE

| | | | |
|---|--------------------------|----------------------------|-------------|
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| TITLE: 16 LD PDIP | DOCUMENT NO: 98ASB42431B | | REV: T |
| | CASE NUMBER: 648-08 | | 19 MAY 2005 |
| | STANDARD: NON-JEDEC | | |



0.75 X45°
0.25



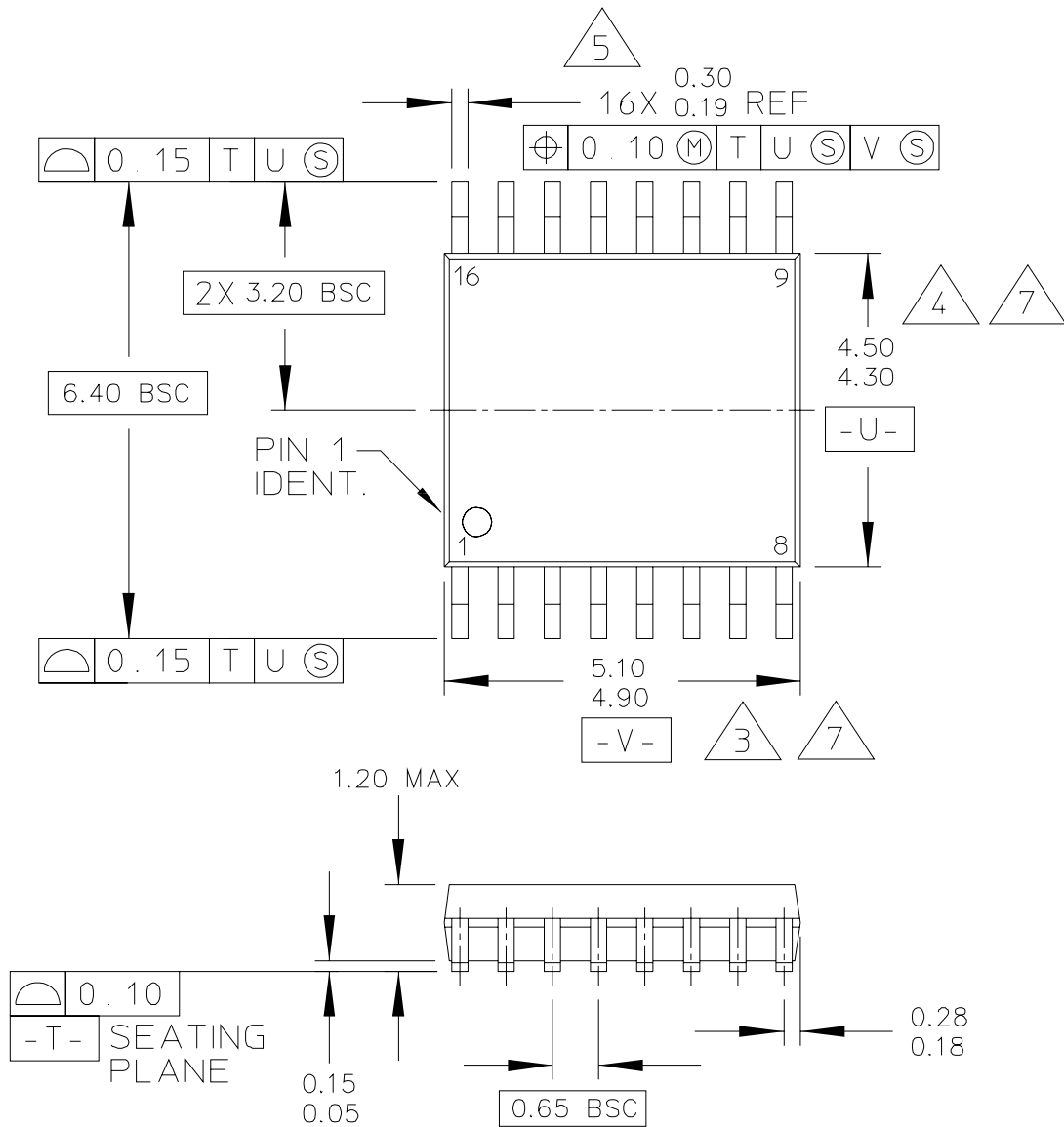
SECTION A-A

| | | | |
|---|---------------------------|----------------------------|--|
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| TITLE: 16LD SOIC W/B, 1.27 PITCH CASE-OUTLINE | DOCUMENT NO: 98ASB42567B | REV: F | |
| | CASE NUMBER: 751G-04 | 02 JUN 2005 | |
| | STANDARD: JEDEC MS-013AA | | |

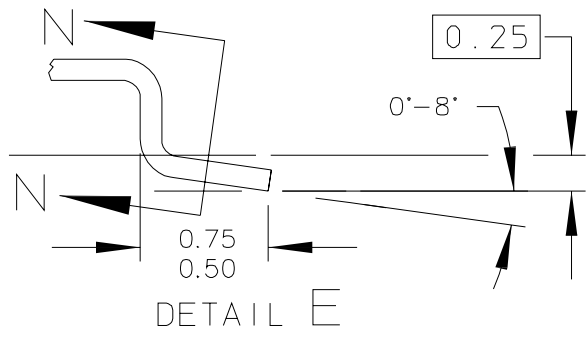
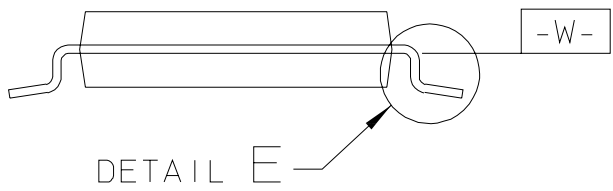
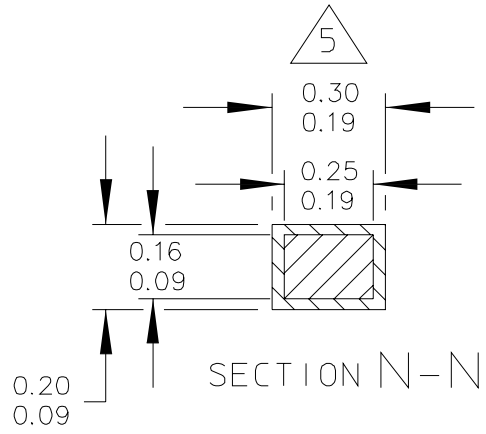
NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62 mm.

| | | | |
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| TITLE: 16LD SOIC W/B, 1.27 PITCH, CASE OUTLINE | DOCUMENT NO: 98ASB42567B | REV: F | |
| | CASE NUMBER: 751G-04 | 02 JUN 2005 | |
| | STANDARD: JEDEC MS-013AA | | |



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| TITLE: 16 LD TSSOP, PITCH 0.65MM | DOCUMENT NO: 98ASH70247A | REV: B | |
| | CASE NUMBER: 948F-01 | 19 MAY 2005 | |
| | STANDARD: JEDEC | | |



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| TITLE: 16 LD TSSOP, PITCH 0.65MM | DOCUMENT NO: 98ASH70247A | REV: B | |
| | CASE NUMBER: 948F-01 | 19 MAY 2005 | |
| | STANDARD: JEDEC | | |

NOTES:

1. CONTROLLING DIMENSION: MILLIMETER

2. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1982.

3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

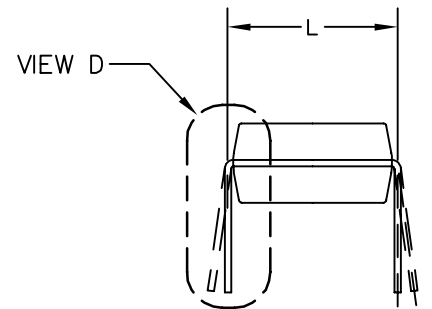
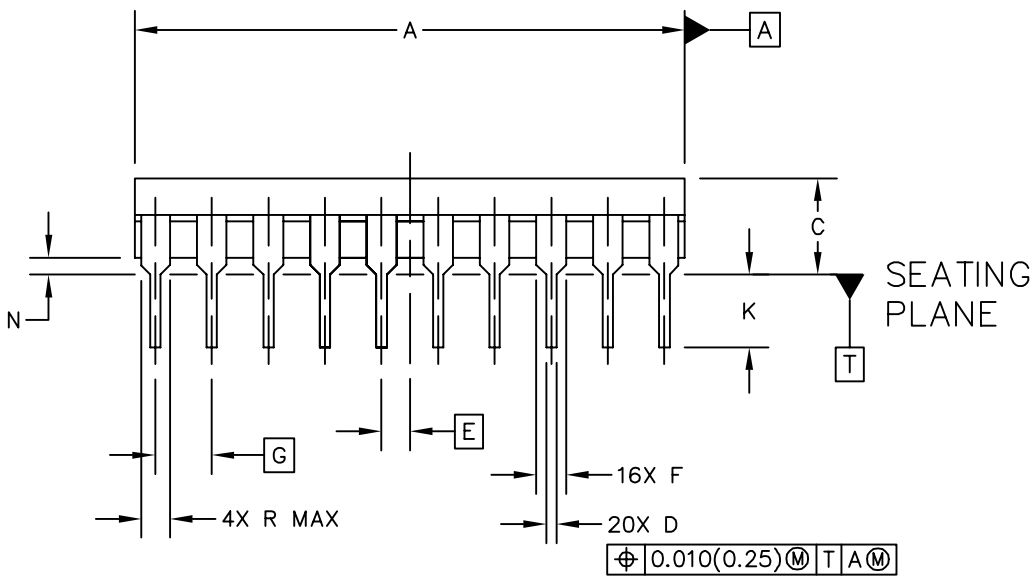
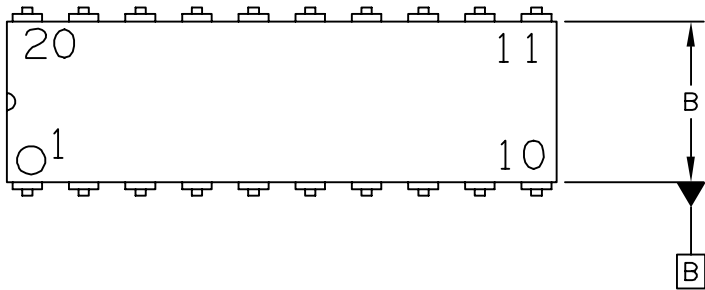
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.

5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

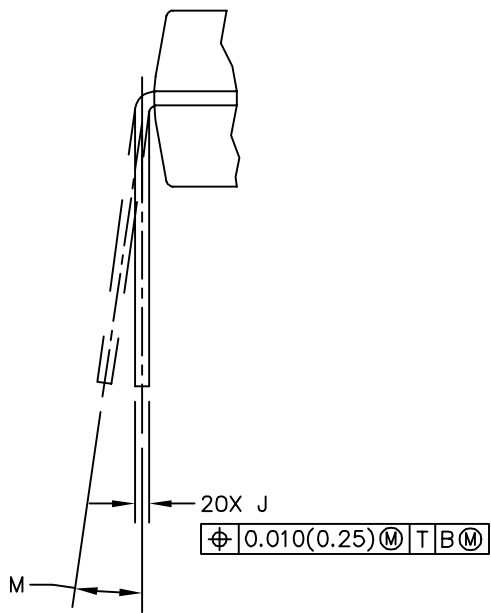
7. DIMENSIONS ARE TO BE DETERMINED AT DATUM PLANE -W-.

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| TITLE: 16 LD TSSOP, PITCH 0.65MM | DOCUMENT NO: 98ASH70247A | REV: B | |
| | CASE NUMBER: 948F-01 | 19 MAY 2005 | |
| | STANDARD: JEDEC | | |



Φ 0.010(0.25) M T A M

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| TITLE: 20LD .300 PDIP | DOCUMENT NO: 98ASB42899B | REV: B | |
| | CASE NUMBER: 738C-01 | 24 MAY 2005 | |
| | STANDARD: NON-JEDEC | | |



VIEW D

| | | | |
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| TITLE: 20LD .300 PDIP | DOCUMENT NO: 98ASB42899B | REV: B | |
| | CASE NUMBER: 738C-01 | 24 MAY 2005 | |
| | STANDARD: NON-JEDEC | | |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

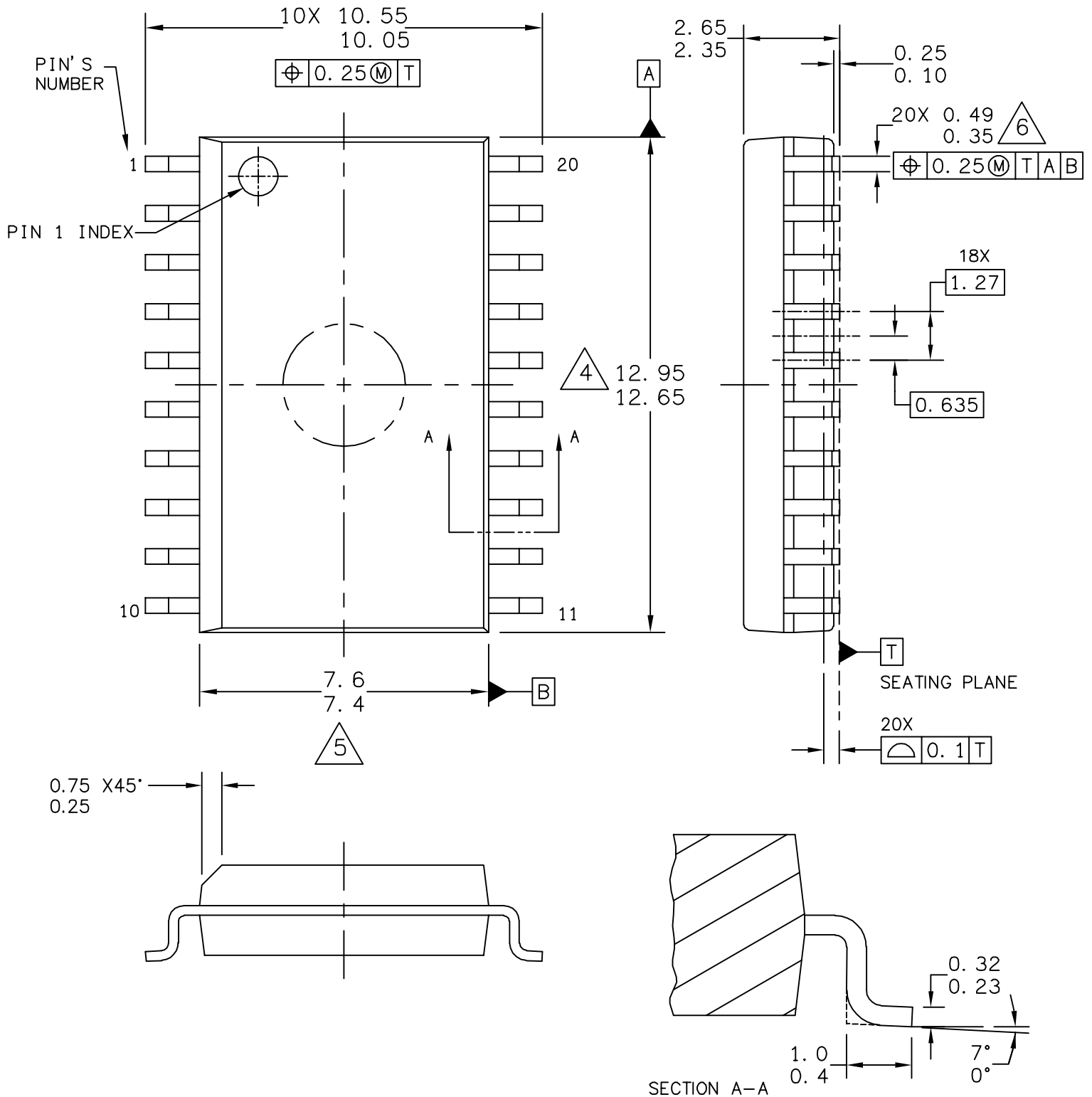
| DIM | MILLIMETERS | | DIM | INCHES | | DIM | MILLIMETERS | | DIM | INCHES | |
|-----|-------------|-------|-----|-----------|-------|-----|-------------|-----|-----|--------|-----|
| | MIN | MAX | | MIN | MAX | | MIN | MAX | | MIN | MAX |
| A | 24.39 | 24.99 | | 0.960 | 0.984 | | | | | | |
| B | 6.96 | 7.49 | | 0.274 | 0.295 | | | | | | |
| C | 3.56 | 5.08 | | 0.140 | 0.200 | | | | | | |
| D | 0.38 | 0.56 | | 0.015 | 0.022 | | | | | | |
| E | 1.27 BSC | | | 0.050 BSC | | | | | | | |
| F | 1.14 | 1.52 | | 0.045 | 0.060 | | | | | | |
| G | 2.54 BSC | | | 0.100 BSC | | | | | | | |
| J | 0.20 | 0.38 | | 0.008 | 0.015 | | | | | | |
| K | 2.79 | 3.76 | | 0.110 | 0.148 | | | | | | |
| L | 7.62 BSC | | | 0.300 BSC | | | | | | | |
| M | 0° | 15° | | 0° | 15° | | | | | | |
| N | 0.50 | 1.01 | | 0.020 | 0.040 | | | | | | |
| R | | 1.29 | | | 0.051 | | | | | | |

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MECHANICAL OUTLINE

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| | | |
|------------------------------|--------------------------|-------------|
| TITLE: 20LD .300 PDIP | DOCUMENT NO: 98ASB42899B | REV: B |
| | CASE NUMBER: 738C-01 | 24 MAY 2005 |
| | STANDARD: NON-JEDEC | |



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| TITLE: 20LD SOIC W/B, 1.27 PITCH CASE-OUTLINE | DOCUMENT NO: 98ASB42343B | REV: J | |
| | CASE NUMBER: 751D-07 | 23 MAR 2005 | |
| | STANDARD: JEDEC MS-013AC | | |

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
- △ THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
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- △ THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62 mm.

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| TITLE: 20LD SOIC W/B, 1.27 PITCH, CASE OUTLINE | DOCUMENT NO: 98ASB42343B | REV: J | |
| | CASE NUMBER: 751D-07 | 23 MAR 2005 | |
| | STANDARD: JEDEC MS-013AC | | |

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Document Number: MC9RS08KA8

Rev. 4

6/2009

