National Semiconductor

MICROCIRCUIT DATA SHEET

MNDS26C32AM-X REV 0B0

Original Creation Date: 01/23/96
Last Update Date: 05/04/01
Last Major Revision Date: 01/23/96

CMOS QUAD DIFFERENTIAL LINE RECEIVER

General Description

The DS26C32A is a quad differential line receiver designed to meet the RS-422, RS-423, and Federal Standards 1020 to 1030 for balanced and unbalanced digital data transmission, while retaining the low power characteristics of CMOS.

The DS26C32A has an input sensitivity of 200 mV over the common mode input voltage range of ± 7V. Each receiver is also equipped with input fail-safe circuitry, which causes the output to go to a logic "1" state when the inputs are open.

The DS26C32A provides an enable and disable function common to all four receivers, and features TRI-STATE outputs with 6 mA source and sink capability. This product is pin compatible with the DS26LS32A and the AM26LS32.

Industry Part Number

DS26C32A

NS Part Numbers

DS26C32AME/883
DS26C32AMJ/883
DS26C32AMW/883
DS26C32AMWG/883

Prime Die

DS26C32

Controlling Document

SEE FEATUES SECTION

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Low power CMOS design
- ±0.2V sensitivity over the entire common mode range
- Input fail-safe circuitry
- Inputs won't load line when Vcc = 0V
- Meets the requirements of EIA standard RS-422
- TRI-STATE outputs for connection to system buses

CONTROLLING DOCUMENTS:

DS26C32AME/883	5962-9164001M2A
DS26C32AMJ/883	5962-9164001MEA
DS26C32AMW/883	5962-9164001MFA
DS26C32AMWG/883	5962-9164001MXA

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage (Vcc)	7V
Common Mode Range (Vcm)	±14V
Differential Input Voltage (Vdiff)	±14V
Enable Input Voltage (Vin)	7V
Storage Temperature Range (Tstg)	-65 C ≤ Ta ≤ +150 C
Lead Temperature (Soldering 4 seconds)	260 C

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.

Recommended Operating Conditions

Operating Voltage (Vcc)	4.5V to 5.5V
Operating Temperature Range	-55 C ≤ Ta ≤ +125 C

Electrical Characteristics

DC PARAMETERS

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vtl	Minimum Differential Input Voltage	Vcc=5V, Vout=Voh or Vol, -7 < Vcm < +7	1		-200	+200	mV	1, 2, 3
Rin	Input Resistance	Vcc= 5V, -7 < Vcm < +7, "One input AC Gnd"			4.5	11	KOhm	1, 2, 3
Iin	Input Current	Vcc=5V, Vin= +10V, Other Input = Gnd				+1.8	mA	1, 2, 3
		Vcc=5V, Vin= -10V, Other Input = Gnd				-2.7	mA	1, 2, 3
Voh	Logical "1" Output Voltage	Vcc=4.5V, Vdiff=+1V, Iout = -6.0mA			3.8		V	1, 2, 3
Vol	Logical "0" Output Voltage	Vcc=5.5V, Vcc=Max, Vdiff=-1V, Iout = 6.0mA				0.3	V	1, 2, 3
Vih	Minimum Enable High Level Voltage		1		2.0		V	1, 2, 3
Vil	Maximum Enable Low Level Voltage		1			0.8	V	1, 2, 3
Ioz	Maximum TRI-STATE Output Leakage Current	Vout=Vcc or Gnd, $\overline{\text{Enable}}$ = Vih				±5.0	uA	1, 2, 3
Ii	Maximum Enable Input Current	Vin = Vcc or Gnd				± 1.0	uA	1, 2, 3
Icc	Quiescent Power Supply Current	Vdif= +1V, Vcc = 5.5V				25	mA	1, 2, 3

Electrical Characteristics

AC PARAMETERS: PROPAGATION DELAY TIME:

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc=5V ±10%, Cl=50pF, Vdiff=2.5V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tPLH	Input to Output Propagation Delay	Vcm= 0V				35	nS	9, 10, 11
tPHL	Input to Output Propagation Delay	Vcm= 0V				35	nS	9, 10, 11
tRise	Output Rise Time	Vcm= 0V				9	nS	9, 10, 11
tFall	Output Fall Time	Vcm= 0V				9	nS	9, 10, 11
tPLZ	Output Disable Time	Rl=1000 Ohms				29	nS	9, 10, 11
tPZL	Output Enable Time	Rl=1000 Ohms				29	nS	9, 10, 11
tPHZ	Output Disable Time	Rl=1000 Ohms				29	nS	9, 10, 11
tPZH	Output Enable Time	Rl=1000 Ohms				29	nS	9, 10, 11

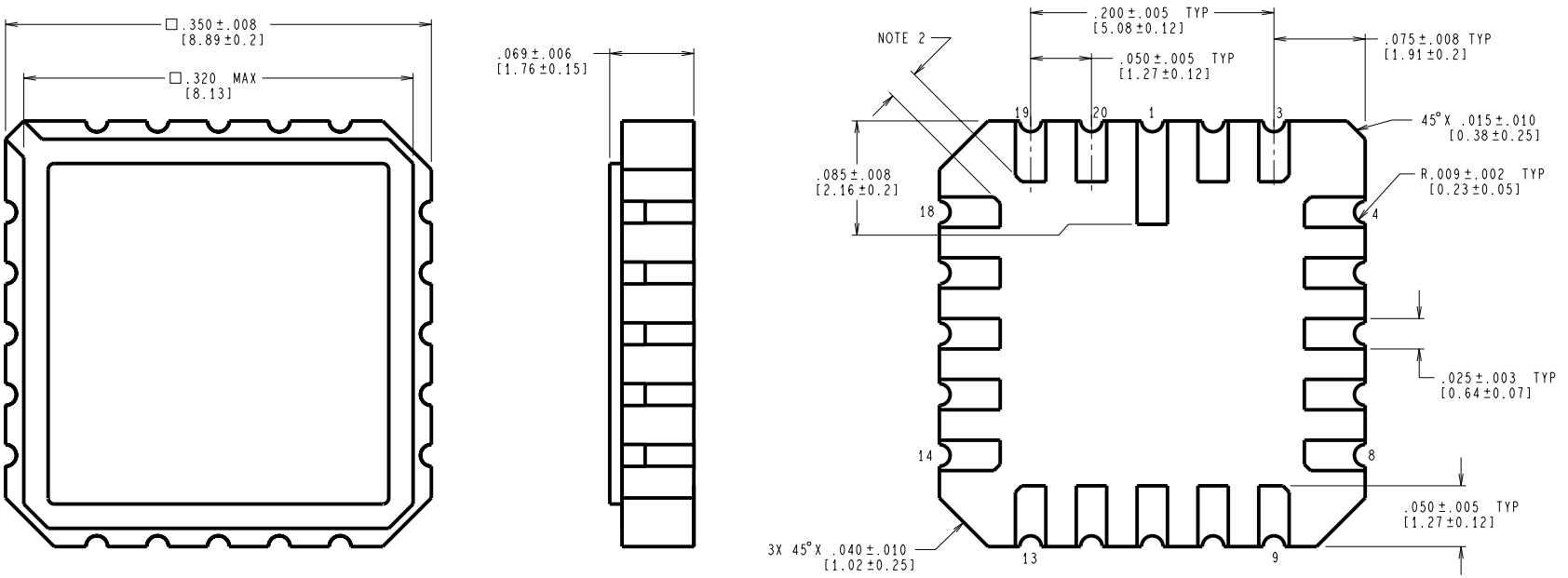
Note 1: Parameter tested go-no-go only.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
E20ARE	LCC (E), TYPE C, 20 TERMINAL(P/P DWG)
J16ARL	CERDIP (J), 16 LEAD (P/P DWG)
P000355A	CERAMIC SOIC (WG), 16 LEAD (PINOUT)
P000439A	CERDIP (J), 16 LEAD (PIN OUT)
P000440A	LCC (E), TYPE C, 20 TERMINAL (PINOUT)
P000443A	CERPACK (W), 16 LEAD (PIN OUT)
W16ARL	CERPACK (W), 16 LEAD (P/P DWG)
WG16ARC	CERAMIC SOIC (WG), 16 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
E	REVISE AND REDRAW.	10005	02/10/94	DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

   a. 50 MICROINCHES/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICROINCHES/1.27-8.89 MICROMETERS NICKEL.

   b. SOLDER DIP.
   SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.

2. CORNER PADS MAY HAVE A 45°X.020IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE .015IN/0.38mm DIMENSION.

4. REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL/AERO
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: Dwayne Grady	02/10/94
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION
INCH [MM]

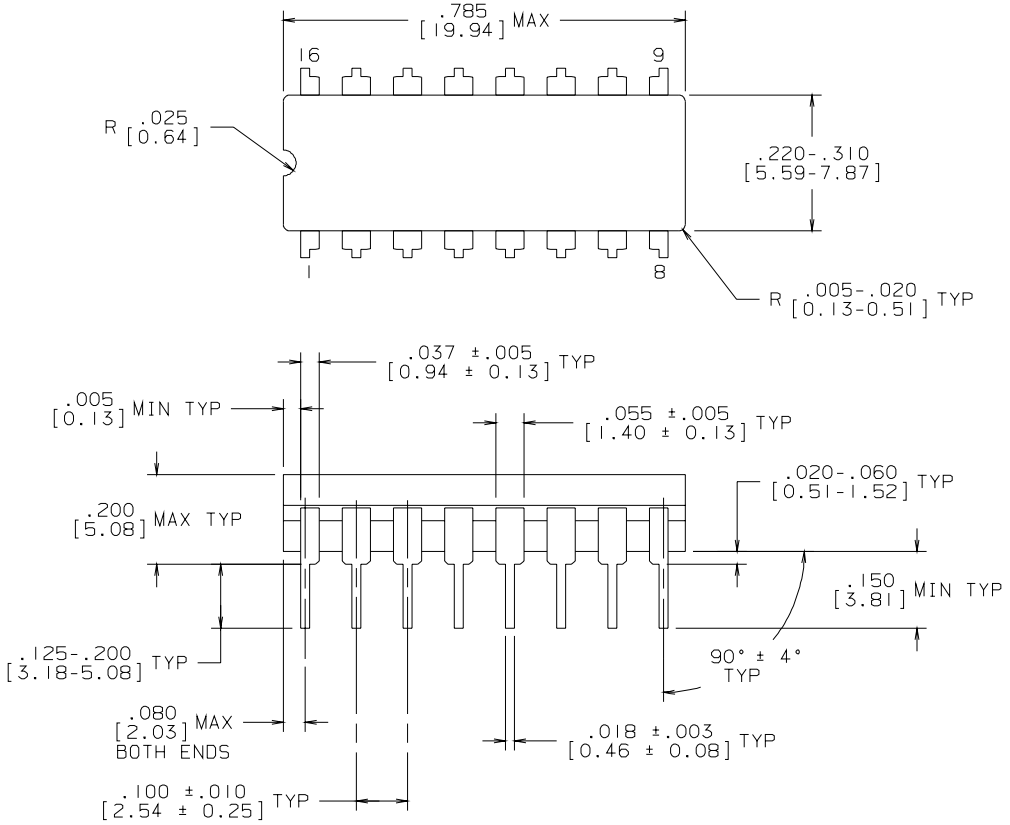
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

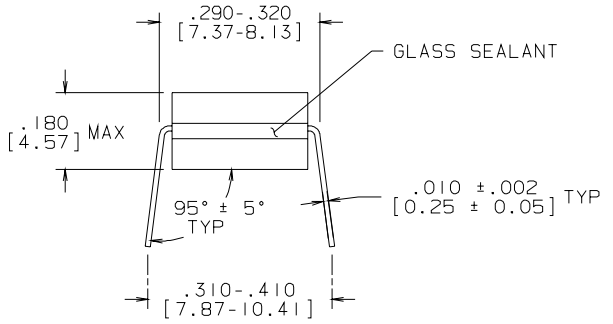
LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-E20A	E

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	09996	09/15/93	TL/





MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

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2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 16 LEAD

PROJECTION

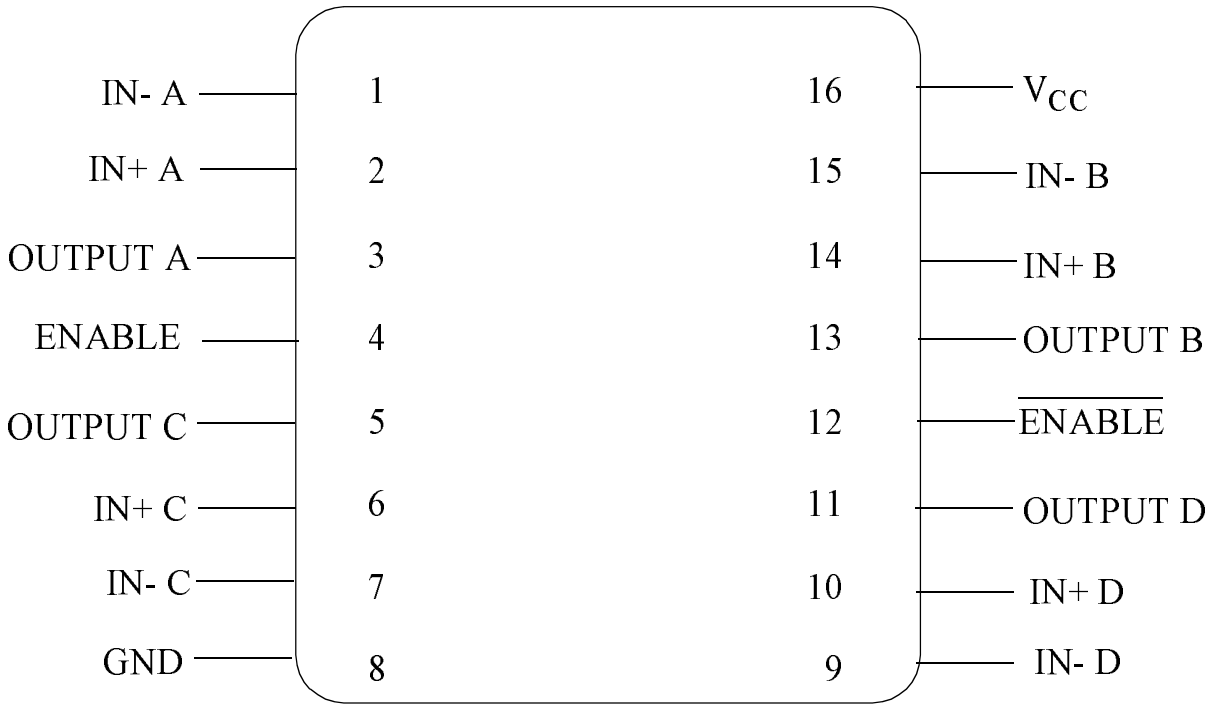
INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J16A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1

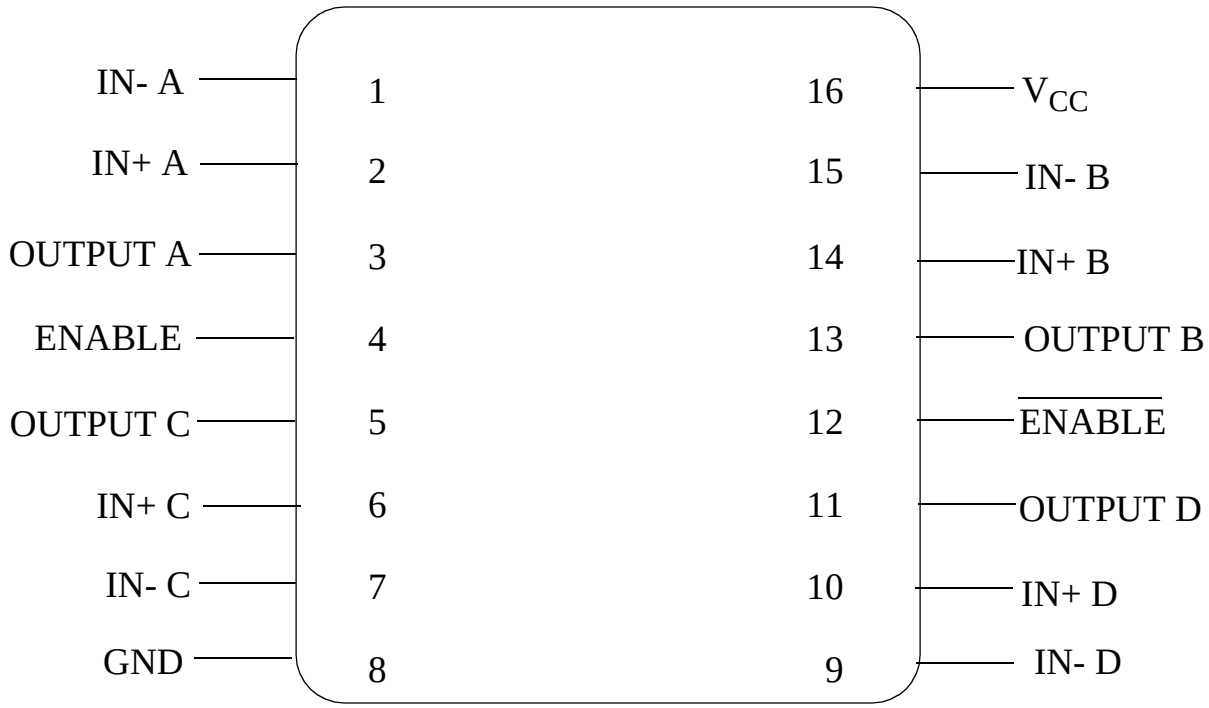
NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AD, DATED 04/1981.



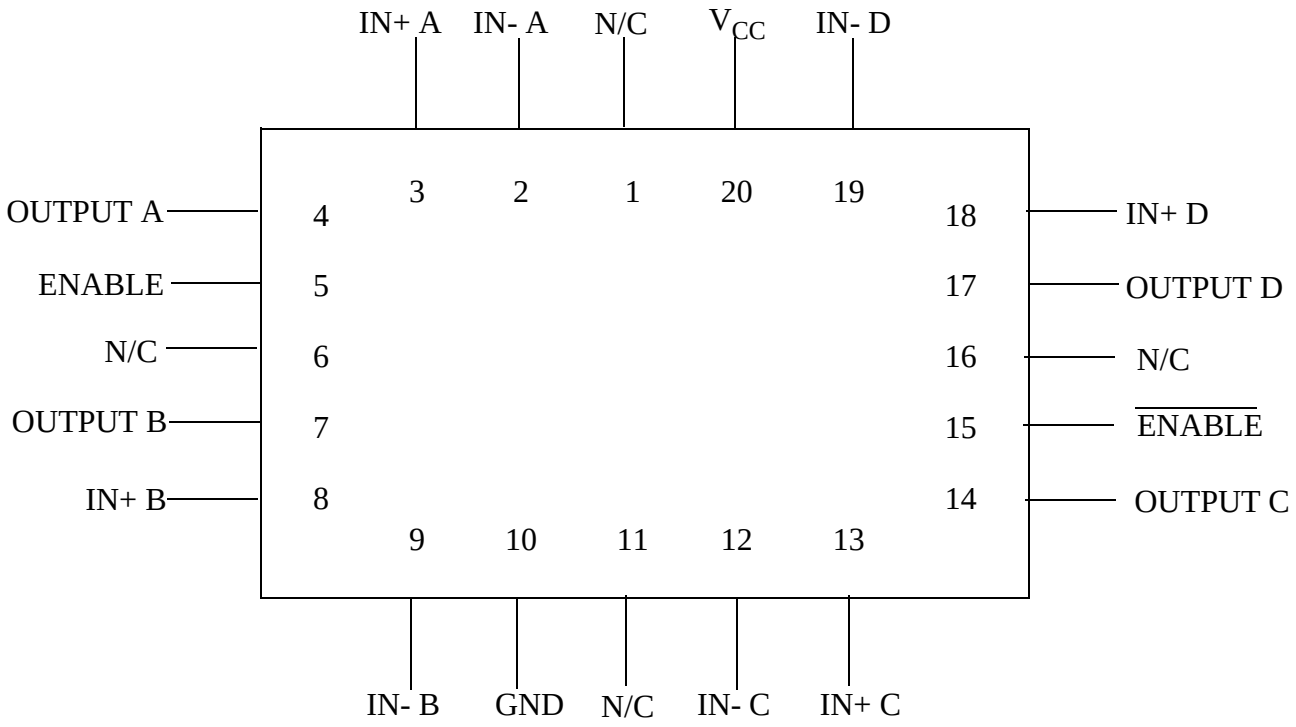
DS26C32AMWG
16 - LEAD CERAMIC SOIC
CONNECTION DIAGRAM
TOP VIEW
P000355A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



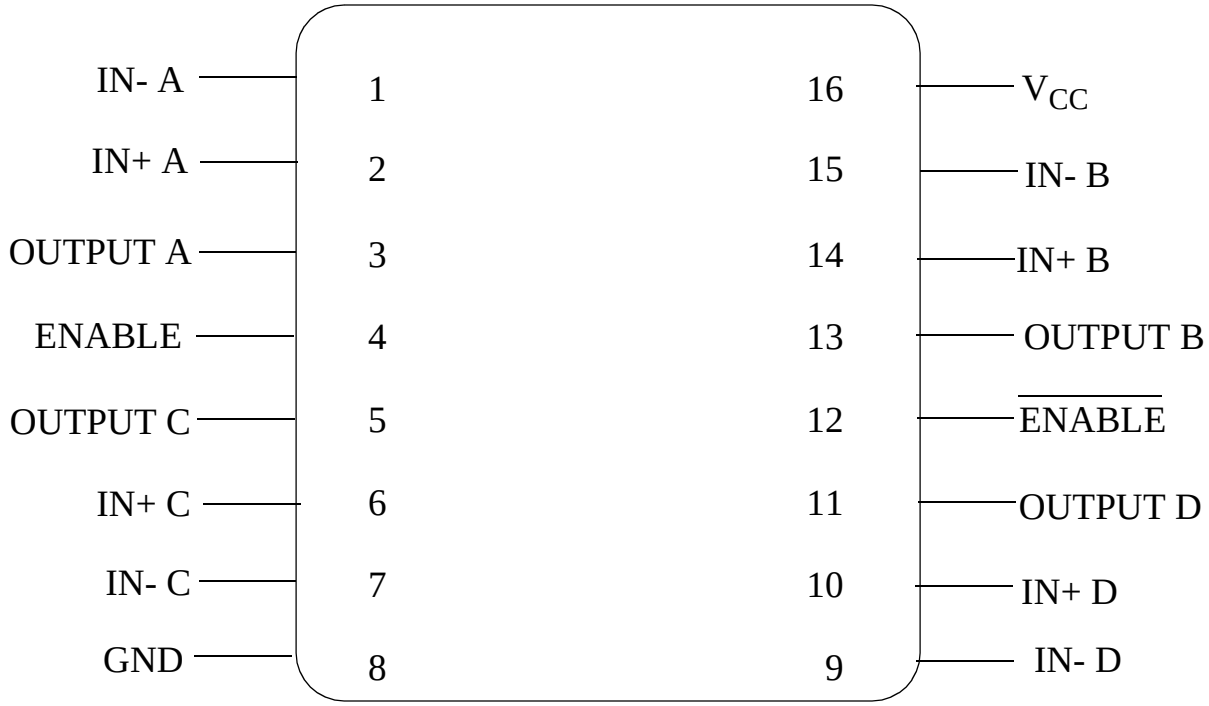
DS26C32AMJ
16 - LEAD DIP
CONNECTION DIAGRAM
TOP VIEW
P000439A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



DS26C32AME
20 - LEAD LCC
CONNECTION DIAGRAM
TOP VIEW
P000440A

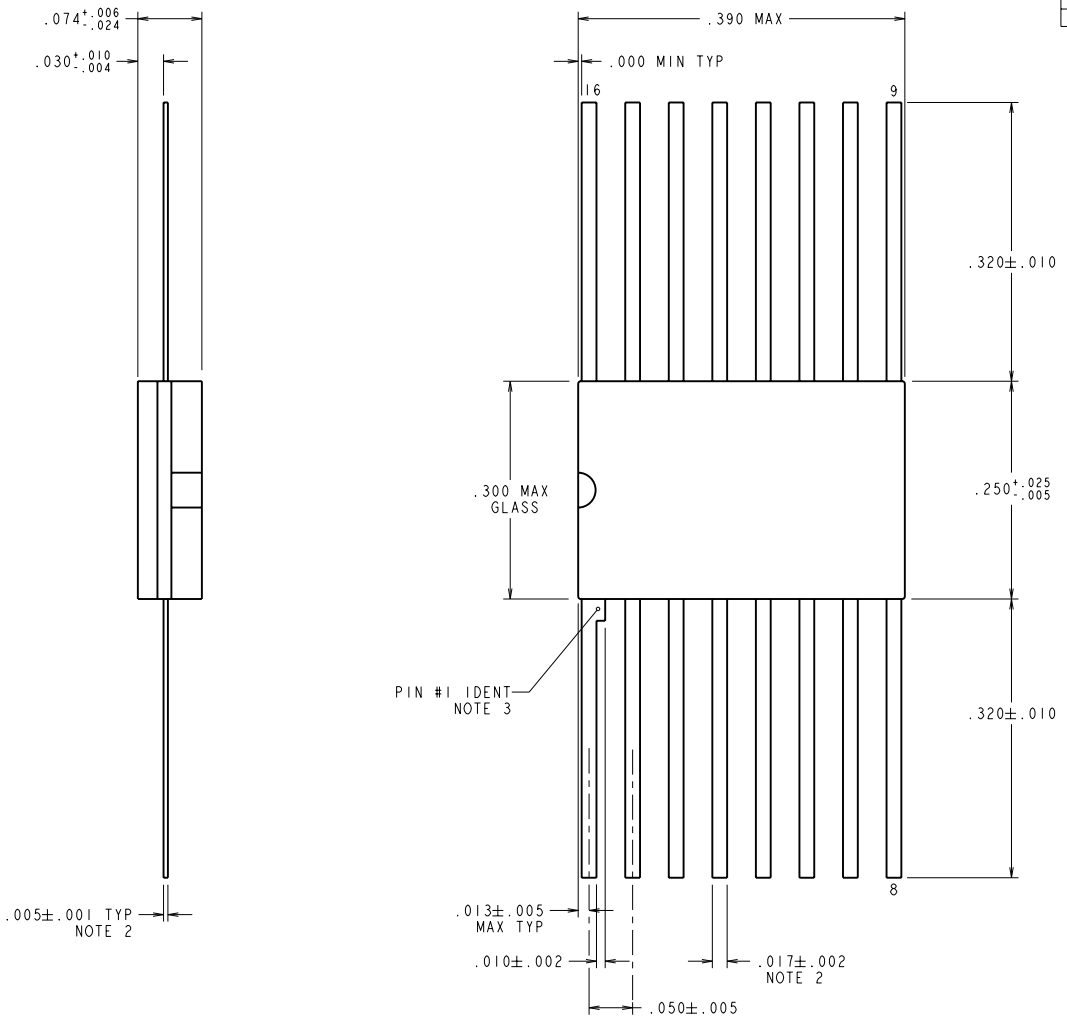
National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



DS26C32AMW
16 - LEAD CERPACK
CONNECTION DIAGRAM
TOP VIEW
P000443A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
K	REVISE AND REDRAW PER NEW STANDARD.	10514	07/28/94	DEG/AEP
L	.017±.002 WAS .017±.020.	10656	10/21/94	DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
4. REFERENCE JEDEC REGISTRATION MO-092, VARIATION AC, DATED 04/89.

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN D.E.Grady	07/28/94
DFTG. CHK.	
ENGR. CHK.	

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2900 Semiconductor dr, Santa Clara, CA 95052-8090

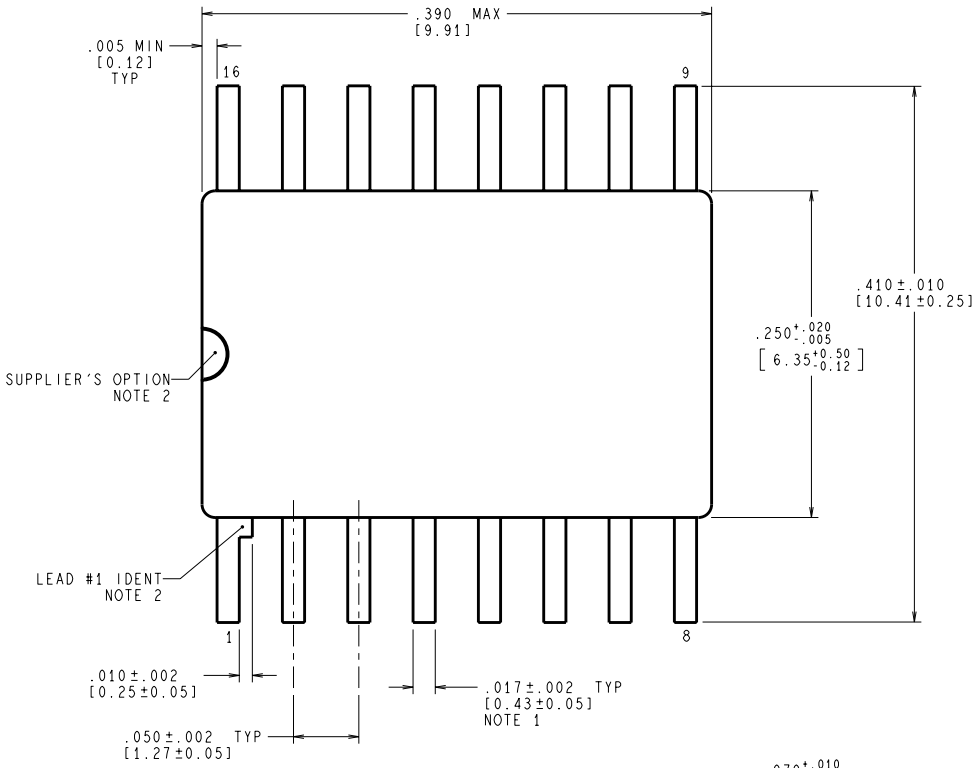
CERPACK, 16 LEAD

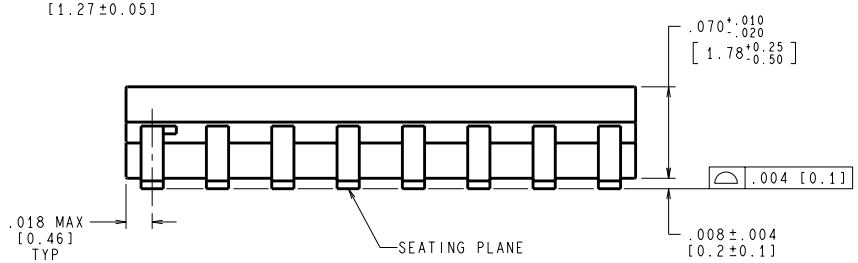
PROJECTION — INCH [MM]

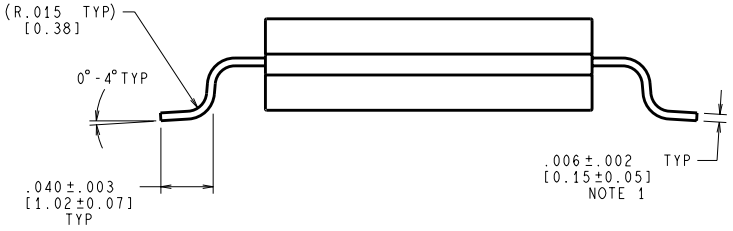
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-W16A	L

DO NOT SCALE DRAWING — SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11376	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002; DIM .040±.003 WAS .037±.003	11443	04/19/1996	MS/KH
C	R .015[0.38] WAS R .006[0.15]	11840	10/08/1997	TL/







NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 16 LEAD, GULL WING

PROJECTION | INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-WG16A	C

DO NOT SCALE DRAWING | SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0B0	M0002087	05/04/01	Rose Malone	Update MDS: MNDS26C32AM-X, Rev. 0A0 to MNDS26C32AM-X, Rev. 0B0. Added to Main Table, Features Section and Graphics Section reference WG pkg.