Features

- **EE Programmable 65,536 x 1-, 131,072 x 1-, 262,144 x 1-, 524,288 x 1-, 1,048,576 x 1-, 2,097,152 x 1-, and 4,194,304 x 1-bit Serial Memories Designed to Store Configuration Programs for Field Programmable Gate Arrays (FPGAs)**
- **Supports both 3.3V and 5.0V Operating Voltage Applications**
- **In-System Programmable (ISP) via Two-Wire Bus**
- **Simple Interface to SRAM FPGAs**
- **Compatible with Atmel AT6000, AT40K and AT94K Devices, Altera® FLEX®, APEX™ Devices, ORCA®, Xilinx® XC3000, XC4000, XC5200, Spartan®, Virtex® FPGAs**
- **Cascadable Read-back to Support Additional Configurations or Higher-density Arrays**
- **Very Low-power CMOS EEPROM Process**
- **Programmable Reset Polarity**
- **Available in 6 mm x 6 mm x 1 mm 8-lead LAP (Pin-compatible with 8-lead SOIC/VOIC Packages), 8-lead PDIP, 8-lead SOIC, 20-lead PLCC, 20-lead SOIC and 44-lead TQFP Packages**
- **Emulation of Atmel's AT24CXXX Serial EEPROMs**
- **Low-power Standby Mode**
- **High-reliability**
  - **Endurance: 100,000 Write Cycles**
  - **Data Retention: 90 Years for Industrial Parts (at 85° C) and 190 Years for Commercial Parts (at 70° C)**
- **Green (Pb/Halide-free/RoHS Compliant) Package Options Available**

1. Description

The AT17LV series FPGA Configuration EEPROMs (Configurators) provide an easy-to-use, cost-effective configuration memory for Field Programmable Gate Arrays. The AT17LV series device is packaged in the 8-lead LAP, 8-lead PDIP, 8-lead SOIC, 20-lead PLCC, 20-lead SOIC and 44-lead TQFP, see Table 1-1. The AT17LV series Configurators uses a simple serial-access procedure to configure one or more FPGA devices. The user can select the polarity of the reset function by programming four EEPROM bytes. These devices also support a write-protection mechanism within its programming mode.

The AT17LV series configurators can be programmed with industry-standard programmers, Atmel's ATDH2200E Programming Kit or Atmel's ATDH2225 ISP Cable.

FPGA Configuration EEPROM Memory

AT17LV65
AT17LV128
AT17LV256
AT17LV512
AT17LV010
AT17LV002
AT17LV040

3.3V and 5V System Support

11. Absolute Maximum Ratings*

Operating Temperature	-40° C to +85° C
Storage Temperature	-65° C to +150° C
Voltage on Any Pin with Respect to Ground	-0.1V to V_{CC} +0.5V
Supply Voltage (V_{CC})	-0.5V to +7.0V
Maximum Soldering Temp. (10 sec. @ 1/16 in.)	260° C
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100 pF)	2000V

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

12. Operating Conditions

Symbol	Description		3.3V		5V		Units
			Min	Max	Min	Max	
V_{CC}	Commercial	Supply voltage relative to GND -0° C to +70° C	3.0	3.6	4.75	5.25	V
	Industrial	Supply voltage relative to GND -40° C to +85° C	3.0	3.6	4.5	5.5	V

13. DC Characteristics

V_{CC} = 3.3V ± 10%

Symbol	Description		AT17LV65/ AT17LV128/ AT17LV256		AT17LV512/ AT17LV010		AT17LV002/ AT17LV040		Units
			Min	Max	Min	Max	Min	Max	
V_{IH}	High-level Input Voltage		2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Low-level Input Voltage		0	0.8	0	0.8	0	0.8	V
V_{OH}	High-level Output Voltage (I_{OH} = -2.5 mA)	Commercial	2.4		2.4		2.4		V
V_{OL}	Low-level Output Voltage (I_{OL} = +3 mA)			0.4		0.4		0.4	V
V_{OH}	High-level Output Voltage (I_{OH} = -2 mA)	Industrial	2.4		2.4		2.4		V
V_{OL}	Low-level Output Voltage (I_{OL} = +3 mA)			0.4		0.4		0.4	V
I_{CCA}	Supply Current, Active Mode			5		5		5	mA
I_L	Input or Output Leakage Current (V_{IN} = V_{CC} or GND)		-10	10	-10	10	-10	10	µA
I_{CCS}	Supply Current, Standby Mode	Commercial		50		100		150	µA
		Industrial		100		100		150	µA

14. DC Characteristics

V_{CC} = 5V ± 5% Commercial; V_{CC} = 5V ± 10% Industrial

Symbol	Description		AT17LV65/ AT17LV128/ AT17LV256		AT17LV512/ AT17LV010		AT17LV002/ AT17LV040		Units
			Min	Max	Min	Max	Min	Max	
V_{IH}	High-level Input Voltage		2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Low-level Input Voltage		0	0.8	0	0.8	0	0.8	V
V_{OH}	High-level Output Voltage (I_{OH} = -2.5 mA)	Commercial	3.7		3.86		3.86		V
V_{OL}	Low-level Output Voltage (I_{OL} = +3 mA)			0.32		0.32		0.32	V
V_{OH}	High-level Output Voltage (I_{OH} = -2 mA)	Industrial	3.6		3.76		3.76		V
V_{OL}	Low-level Output Voltage (I_{OL} = +3 mA)			0.37		0.37		0.37	V
I_{CCA}	Supply Current, Active Mode			10		10		10	mA
I_L	Input or Output Leakage Current (V_{IN} = V_{CC} or GND)		-10	10	-10	10	-10	10	µA
I_{CCS}	Supply Current, Standby Mode	Commercial		75		200		350	µA
		Industrial		150		200		350	µA

17. AC Characteristics

V_{CC} = 3.3V ± 10%

Symbol	Description	AT17LV65/128/256				AT17LV512/010/002/040				Units
		Commercial		Industrial		Commercial		Industrial		
		Min	Max	Min	Max	Min	Max	Min	Max	
T_{OE}[1]	OE to Data Delay		50		55		50		55	ns
T_{CE}[1]	$\overline{CE}$ to Data Delay		60		60		55		60	ns
T_{CAC}[1]	CLK to Data Delay		75		80		55		60	ns
T_{OH}	Data Hold from $\overline{CE}$, OE, or CLK	0		0		0		0		ns
T_{DF}[2]	$\overline{CE}$ or OE to Data Float Delay		55		55		50		50	ns
T_{LC}	CLK Low Time	25		25		25		25		ns
T_{HC}	CLK High Time	25		25		25		25		ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	35		60		30		35		ns
T_{HCE}	$\overline{CE}$ Hold Time from CLK (to guarantee proper counting)	0		0		0		0		ns
T_{HOE}	OE High Time (guarantees counter is reset)	25		25		25		25		ns
F_{MAX}	Maximum Clock Frequency		10		10		15		10	MHz

Notes: 1. AC test lead = 50 pF.

2. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady-state active levels.

18. AC Characteristics when Cascading

V_{CC} = 3.3V ± 10%

Symbol	Description	AT17LV65/128/256				AT17LV512/010/002/040				Units
		Commercial		Industrial		Commercial		Industrial		
		Min	Max	Min	Max	Min	Max	Min	Max	
T_{CDF}[2]	CLK to Data Float Delay		60		60		50		50	ns
T_{OCK}[1]	CLK to $\overline{CEO}$ Delay		55		60		50		55	ns
T_{OCE}[1]	$\overline{CE}$ to $\overline{CEO}$ Delay		55		60		35		40	ns
T_{OOE}[1]	$\overline{RESET}$/OE to $\overline{CEO}$ Delay		40		45		35		35	ns
F_{MAX}	Maximum Clock Frequency		8		8		12.5		10	MHz

Notes: 1. AC test lead = 50 pF.

2. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady-state active levels.

19. AC Characteristics

V_{CC} = 5V ± 5% Commercial; V_{CC} = 5V ± 10% Industrial

		AT17LV65/128/256				AT17LV512/010/002/040				
		Commercial		Industrial		Commercial		Industrial		
Symbol	Description	Min	Max	Min	Max	Min	Max	Min	Max	Units
T_{OE}[1]	OE to Data Delay		30		35		30		35	ns
T_{CE}[1]	$\overline{CE}$ to Data Delay		45		45		45		45	ns
T_{CAC}[1]	CLK to Data Delay		50		55		50		50	ns
T_{OH}	Data Hold from $\overline{CE}$, OE, or CLK	0		0		0		0		ns
T_{DF}[2]	$\overline{CE}$ or OE to Data Float Delay		50		50		50		50	ns
T_{LC}	CLK Low Time	20		20		20		20		ns
T_{HC}	CLK High Time	20		20		20		20		ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	35		40		20		25		ns
T_{HCE}	$\overline{CE}$ Hold Time from CLK (to guarantee proper counting)	0		0		0		0		ns
T_{HOE}	OE High Time (guarantees counter is reset)	20		20		20		20		ns
F_{MAX}	Maximum Clock Frequency		12.5		12.5		15		15	MHz

Notes: 1. AC test lead = 50 pF.

2. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady-state active levels.

20. AC Characteristics when Cascading

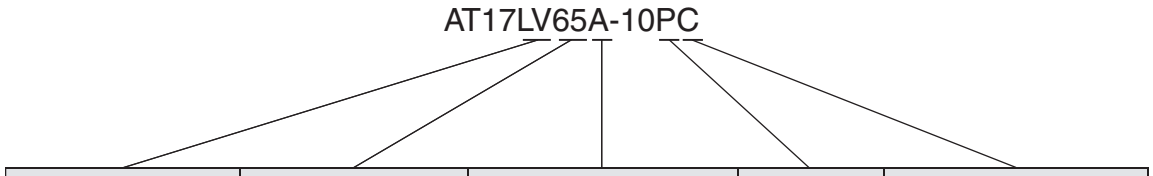
V_{CC} = 5V ± 5% Commercial; V_{CC} = 5V ± 10% Industrial

		AT17LV65/128/256				AT17LV512/010/002/040				
		Commercial		Industrial		Commercial		Industrial		
Symbol	Description	Min	Max	Min	Max	Min	Max	Min	Max	Units
T_{CDF}[2]	CLK to Data Float Delay		50		50		50		50	ns
T_{OCK}[1]	CLK to $\overline{CEO}$ Delay		35		40		35		40	ns
T_{OCE}[1]	$\overline{CE}$ to $\overline{CEO}$ Delay		35		35		35		35	ns
T_{OOE}[1]	$\overline{RESET}$/OE to $\overline{CEO}$ Delay		30		35		30		30	ns
F_{MAX}	Maximum Clock Frequency		10		10		12.5		12.5	MHz

Notes: 1. AC test lead = 50 pF.

2. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady-state active levels.

Figure 21-1. Ordering Code



Voltage	Size (Bits)	Special Pinouts	Package	Temperature
3.0V to 5.5V	65 = 65K 128 = 128K 256 = 256K 512 = 512K 010 = 1M 002 = 2M 040 = 4M	A = Altera Blank = Xilinx/Atmel/ Other	C = 8CN4 P = 8P3 N = 8S1 J = 20J S = 20S2 TQ = 44A BJ = 44J	C = Commercial I = Industrial U = Fully Green

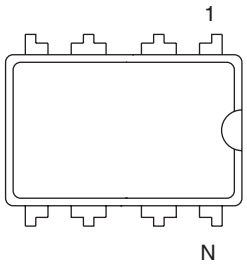
Package Type	
8CN4	8-lead, 6 mm x 6 mm x 1 mm, Leadless Array Package (LAP) – Pin-compatible with 8-lead SOIC/VOID Packages
8P3	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
20J	20-lead, Plastic J-leaded Chip Carrier (PLCC)
20S2	20-lead, 0.300" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
44A	44-lead, Thin (1.0 mm) Plastic Quad Flat Package Carrier (TQFP)

22.2 Green Package Options (Pb/Halide-free/RoHS Compliant)

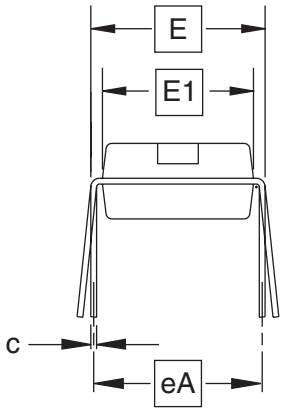
Memory Size	Ordering Code	Package	Operation Range
256-Kbit[1]	AT17LV256-10CU	8CN4	Industrial (-40° C to 85° C)
	AT17LV256-10JU	20J	
	AT17LV256-10NU	8S1	
	AT17LV256-10PU	8P3	
	AT17LV256-10SU	20S2	
512-Kbit[1]	AT17LV512-10CU	8CN4	
	AT17LV512-10JU	20J	
1-Mbit[1]	AT17LV010-10CU	8CN4	
	AT17LV010-10JU	20J	
	AT17LV010-10PU	8P3	
2-Mbit[1]	AT17LV002-10CU	8CN4	
	AT17LV002-10JU	20J	
	AT17LV002-10SU	20S2	
	AT17LV002-10TQU	44A	
4-Mbit[1]	AT17LV040-10TQU	44A	

Note: 1. For operating 5V operating voltage, please refer to the corresponding AC and DC Characteristics.

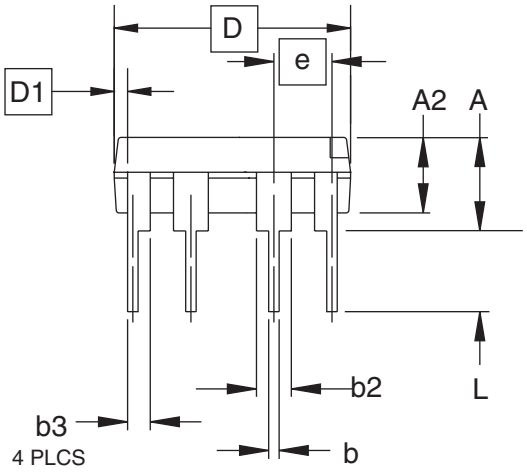
23.2 8P3 – PDIP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = inches)

SYMBOL	MIN	NOM	MAX	NOTE
A			0.210	2
A2	0.115	0.130	0.195	
b	0.014	0.018	0.022	5
b2	0.045	0.060	0.070	6
b3	0.030	0.039	0.045	6
c	0.008	0.010	0.014	
D	0.355	0.365	0.400	3
D1	0.005			3
E	0.300	0.310	0.325	4
E1	0.240	0.250	0.280	3
e	0.100 BSC			
eA	0.300 BSC			4
L	0.115	0.130	0.150	2

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
4. E and eA measured with the leads constrained to be perpendicular to datum.
5. Pointed or rounded lead tips are preferred to ease insertion.
6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8P3**, 8-lead, 0.300" Wide Body, Plastic Dual In-line Package (PDIP)	8P3	B