MC14001B Series

B-Suffix Series CMOS Gates

MC14001B, MC14011B, MC14023B, MC14025B, MC14071B, MC14073B, MC14081B, MC14082B

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

ON Semiconductor®

MARKING DIAGRAMS

Features

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range.
- Double Diode Protection on All Inputs Except: Triple Diode Protection on MC14011B and MC14081B
- Pin−for−Pin Replacements for Corresponding CD4000 Series B Suffix Devices
- Pb−Free Packages are Available

PDIP−14
P SUFFIX
CASE 646

```
14
MC140xxBCP
○ AWLYYWWG
1
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SOIC−14
D SUFFIX
CASE 751A

```
14
140xxBG
○ AWLYWW
1
```

TSSOP−14
DT SUFFIX
CASE 948G

```
14
14
0xxB
ALYW■
○      ■
1
```

SOEIAJ−14
F SUFFIX
CASE 965

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14
MC140xxB
○ ALYWG
1
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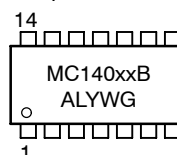
xx   = Specific Device Code
A   = Assembly Location
WL, L   = Wafer Lot
YY, Y   = Year
WW, W   = Work Week
G or ■ = Pb−Free Package
(Note: Microdot may be in either location)

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. Temperature Derating:
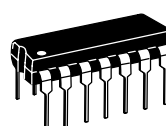   Plastic "P and D/DW" Packages: − 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.
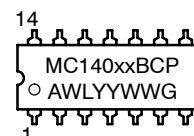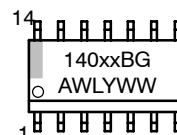
DEVICE INFORMATION

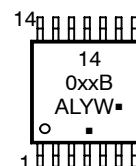| Device	Description
MC14001B	Quad 2−Input NOR Gate
MC14011B	Quad 2−Input NAND Gate
MC14023B	Triple 3−Input NAND Gate
MC14025B	Triple 3−Input NOR Gate
MC14071B	Quad 2−Input OR Gate
MC14073B	Triple 3−Input AND Gate
MC14081B	Quad 2−Input AND Gate
MC14082B	Dual 4−Input AND Gate

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ [2]	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	– – –	0.05 0.05 0.05	– – –	0 0 0	0.05 0.05 0.05	– – –	0.05 0.05 0.05	Vdc
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	– – –	4.95 9.95 14.95	5.0 10 15	– – –	4.95 9.95 14.95	– – –	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	– – –	1.5 3.0 4.0	– – –	2.25 4.50 6.75	1.5 3.0 4.0	– – –	1.5 3.0 4.0	Vdc
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	– – –	3.5 7.0 11	2.75 5.50 8.25	– – –	3.5 7.0 11	– – –	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	− 3.0 − 0.64 − 1.6 − 4.2	– – – –	− 2.4 − 0.51 − 1.3 − 3.4	− 4.2 − 0.88 − 2.25 − 8.8	– – – –	− 1.7 − 0.36 − 0.9 − 2.4	– – – –	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	– – –	0.51 1.3 3.4	0.88 2.25 8.8	– – –	0.36 0.9 2.4	– – –	mAdc
Input Current	I_{in}	15	–	± 0.1	–	±0.00001	± 0.1	–	± 1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}		–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	– – –	0.25 0.5 1.0	– – –	0.0005 0.0010 0.0015	0.25 0.5 1.0	– – –	7.5 15 30	μAdc
Total Supply Current [3] [4] (Dynamic plus Quiescent, Per Gate, C_L = 50 pF)	I_T	5.0 10 15	I_T = (0.3 μA/kHz) f + I_{DD}/N I_T = (0.6 μA/kHz) f + I_{DD}/N I_T = (0.9 μA/kHz) f + I_{DD}/N							μAdc

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L − 50) \text{ Vfk}$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001 x the number of exercised gates per package.
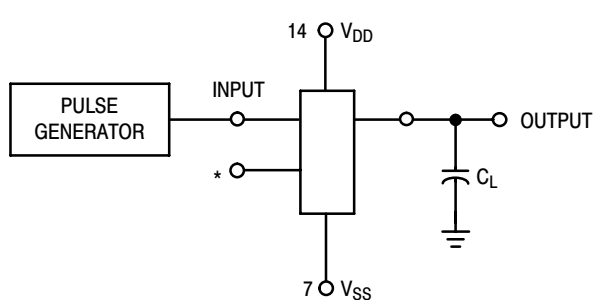
B−SERIES GATE SWITCHING TIMES

SWITCHING CHARACTERISTICS [5] (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ [6]	Max	Unit
Output Rise Time, All B−Series Gates t_{TLH} = (1.35 ns/pF) C_L + 33 ns t_{TLH} = (0.60 ns/pF) C_L + 20 ns t_{TLH} = (0.40 ns/PF) C_L + 20 ns	t_{TLH}	 5.0 10 15	 – – –	 100 50 40	 200 100 80	ns
Output Fall Time, All B−Series Gates t_{THL} = (1.35 ns/pF) C_L + 33 ns t_{THL} = (0.60 ns/pF) C_L + 20 ns t_{THL} = (0.40 ns/pF) C_L + 20 ns	t_{THL}	 5.0 10 15	 – – –	 100 50 40	 200 100 80	ns
Propagation Delay Time MC14001B, MC14011B only t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 80 ns t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 32 ns t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 27 ns All Other 2, 3, and 4 Input Gates t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 115 ns t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 47 ns t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 37 ns 8−Input Gates (MC14068B, MC14078B) t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 155 ns t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 62 ns t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 47 ns	t_{PLH}, t_{PHL}	 5.0 10 15 5.0 10 15 5.0 10 15	 – – – – – – – – –	 125 50 40 160 65 50 200 80 60	 250 100 80 300 130 100 350 150 110	ns

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

*All unused inputs of AND, NAND gates must be connected to V_{DD}.
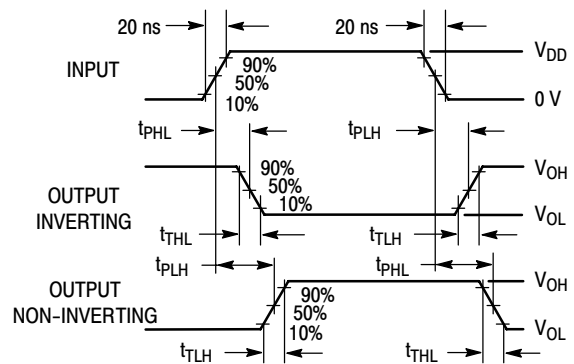 All unused inputs of OR, NOR gates must be connected to V_{SS}.

Figure 1. Switching Time Test Circuit and Waveforms

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ORDERING INFORMATION

| Device	Package	Shipping[†]
MC14081BCP	PDIP−14	25 Units / Rail
MC14081BCPG	PDIP−14 (Pb−Free)	
MC14081BD	SOIC−14	55 Units / Rail
MC14081BDG	SOIC−14 (Pb−Free)	
MC14081BDR2	SOIC−14	2500 Units / Tape & Reel
MC14081BDR2G	SOIC−14 (Pb−Free)	
MC14081BDTR2	TSSOP−14*	
MC14081BDTR2G	TSSOP−14* (Pb−Free)	
MC14081BFEL	SOEIAJ−14	2000 Units / Tape & Reel
MC14081BFELG	SOEIAJ−14 (Pb−Free)	
MC14082BCP	PDIP−14	2000 Units / Box
MC14082BCPG	PDIP−14 (Pb−Free)	
MC14082BD	SOIC−14	55 Units / Rail
MC14082BDG	SOIC−14 (Pb−Free)	
MC14082BDR2	SOIC−14	2500 Units / Tape & Reel
MC14082BDR2G	SOIC−14 (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

PACKAGE DIMENSIONS

PDIP−14
CASE 646−06
ISSUE P
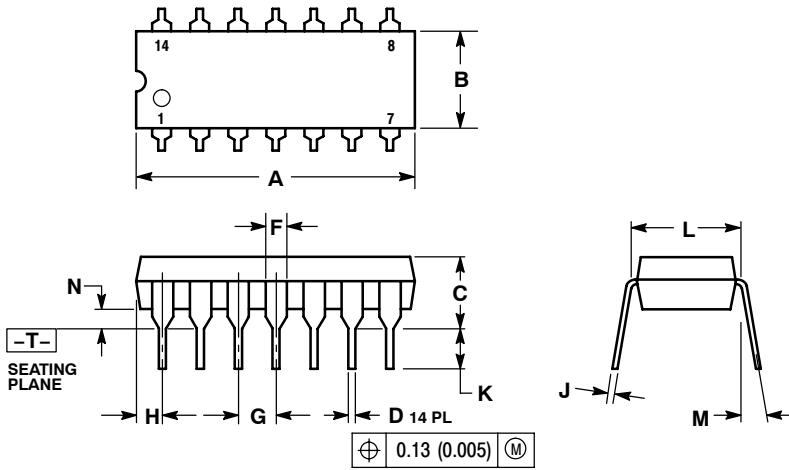
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	−−−	10 °	−−−	10 °
N	0.015	0.039	0.38	1.01

SEATING PLANE

−T−

0.13 (0.005) Ⓜ

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MC14001B Series

PACKAGE DIMENSIONS

SOIC−14
CASE 751A−03
ISSUE H
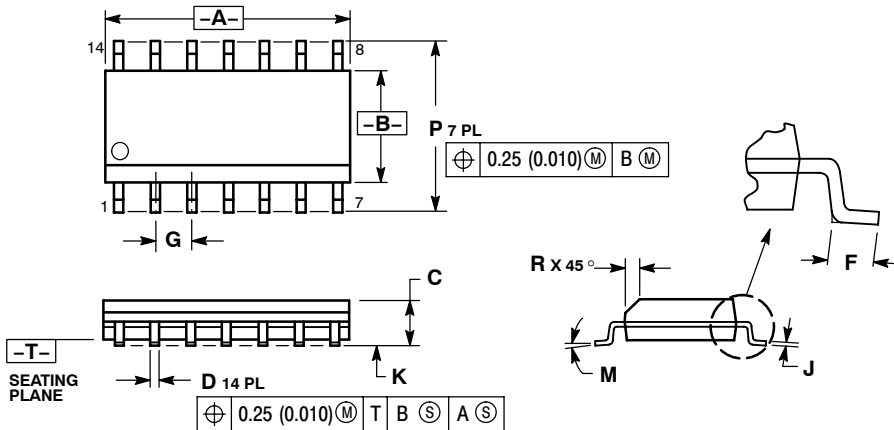
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*
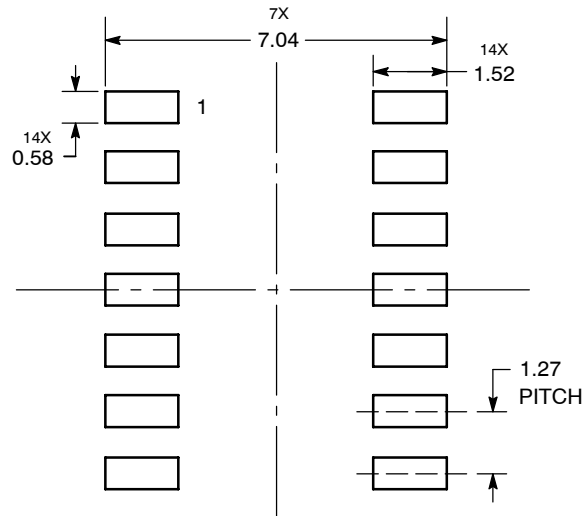
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.