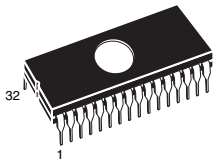
M27C801

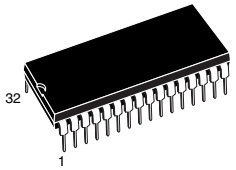
8 Mbit (1Mb x 8) UV EPROM and OTP EPROM

Features

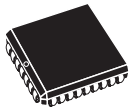
- 5 V ± 10% supply voltage in Read operation
- Access time: 55 ns
- low Power Consumption:
  - Active current: 35 mA at 5 MHz
  - Standby current: 100 µA
- Programming voltage: 12.75 V ± 0.25 V
- Programming time: 50 µs/word
- Electronic signature
  - Manufacturer code: 20h
  - Device code: 42h
- ECOPACK® packages available



FDIP32W (F)



PDIP32 (B)



PLCC32 (K)

1 Description

The M27C801 is an 8 Mbit EPROM offered in the two ranges UV (ultra violet erase) and OTP (one time programmable). It is ideally suited for applications where fast turn-around and pattern experimentation are important requirements and is organized as 1,048,576 by 8 bits.

The FDIP32W (window ceramic frit-seal package) has transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

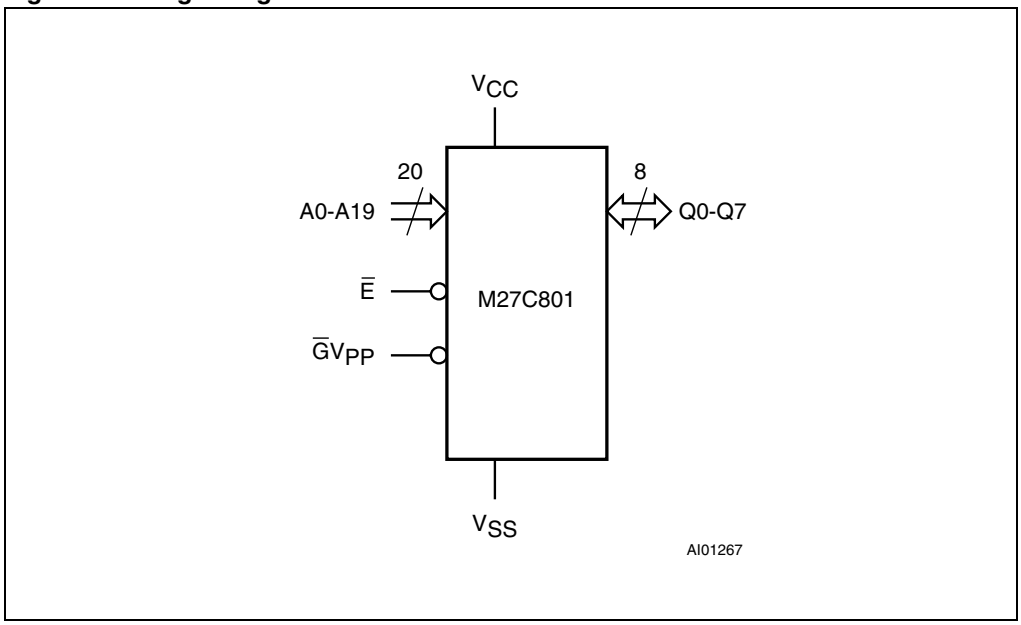
For applications where the content is programmed only one time and erasure is not required, the M27C801 is offered in PDIP32 and PLCC32 packages.

In order to meet environmental requirements, ST offers the M27C801 in ECOPACK® packages. ECOPACK packages are Lead-free. The category of second-level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK® specifications are available at: www.st.com.

See *Figure 1: Logic diagram* and *Table 1: Signal descriptions* for a brief overview of the signals connected to this device.

Figure 1. Logic diagram



3 Maximum ratings

Stressing the device outside the ratings listed in *Table 4* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the Operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
T_A	Ambient operating temperature (1)	–40 to 125	°C
T_{BIAS}	Temperature under bias	–50 to 125	°C
T_{STG}	Storage temperature	–65 to 150	°C
V_{IO} (2)	Input or output voltage (except A9)	–2 to 7	V
V_{CC}	Supply voltage	–2 to 7	V
V_{A9} (2)	A9 voltage	–2 to 13.5	V
V_{PP}	Program supply voltage	–2 to 14	V

1. Depends on range.
2. Minimum DC voltage on Input or Output is –0.5 V with possible undershoot to –2.0 V for a period less than 20 ns. Maximum DC voltage on Output is V_{CC} +0.5 V with possible overshoot to V_{CC} +2 V for a period less than 20 ns.

4 DC and AC characteristics

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristic tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 5. AC measurement conditions

Parameter	High Speed	Standard
Input rise and fall times	≤10ns	≤20ns (10% to 90%)
Input pulse voltages	0 to 3V	0.4 to 2.4V
Input and output timing ref. voltages	1.5V	0.8 and 2V

Figure 5. AC testing input output waveform

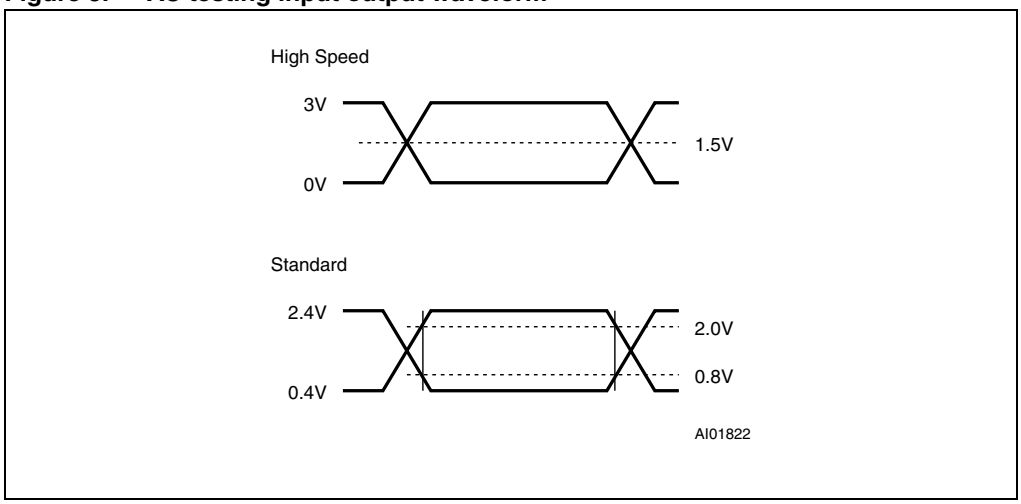


Figure 6. AC testing load circuit

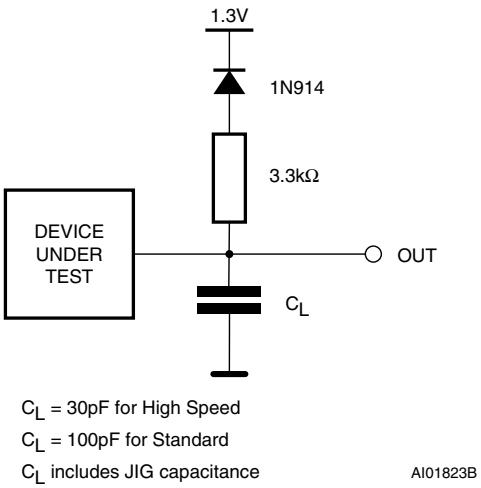


Table 6. Capacitance(1) (2)

Symbol	Parameter	Test condition	Min.	Max.	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V		6	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V		12	pF

1. T_A = 25 °C, f = 1 MHz.
2. Sampled only, not 100% tested.

Table 7. Read mode DC characteristics(1) (2)

Symbol	Parameter	Test condition	Min.	Max.	Unit
I_{LI}	Input leakage current	0V ≤V_{IN} ≤V_{CC}		±10	µA
I_{LO}	Output leakage current	0V ≤V_{OUT} ≤V_{CC}		±10	µA
I_{CC}	Supply current	$\overline{E}$ = V_{IL}, $\overline{G}V_{PP}$ = V_{IL}, I_{OUT} = 0 mA, f = 5 MHz		35	mA
I_{CC1}	Supply current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V		100	µA
I_{PP}	Program current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input low voltage		–0.3	0.8	V
V_{IH} (3)	Input high voltage		2	V_{CC} + 1	V
V_{OL}	Output low voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output high voltage TTL	I_{OH} = –1 mA	3.6		V
	Output high voltage CMOS	I_{OH} = –100 µA	V_{CC} – 0.7		V

1. T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5 V ± 10%.
2. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
3. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 8. Programming mode DC characteristics(1) (2)

Symbol	Parameter	Test condition	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply current			50	mA
I_{PP}	Program current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input low voltage		–0.3	0.8	V
V_{IH}	Input high voltage		2	V_{CC} + 0.5	V
V_{OL}	Output low voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output high voltage TTL	I_{OH} = –1mA	3.6		V
V_{ID}	A9 voltage		11.5	12.5	V

1. T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V
2. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Read mode AC characteristics(1) (2)

Symbol	Alt	Parameter	Test condition	-55 (3)		-80/-90		-100		Unit
				Min.	Max.	Min.	Max.	Min	Max.	
t_{AVQV}	t_{ACC}	Address valid to output valid	$\overline{E} = V_{IL}$, $\overline{G}V_{PP} = V_{IL}$		55		80		100	ns
t_{ELQV}	t_{CE}	Chip Enable low to output valid	$\overline{G}V_{PP} = V_{IL}$		55		80		100	ns
t_{GLQV}	t_{OE}	Output Enable low to output valid	$\overline{E} = V_{IL}$		30		40		50	ns
t_{EHQZ}(4)	t_{DF}	Chip Enable high to output Hi-Z	$\overline{G}V_{PP} = V_{IL}$	0	25	0	35	0	40	ns
t_{GHQZ}(4)	t_{DF}	Output Enable high to output Hi-Z	$\overline{E} = V_{IL}$	0	25	0	35	0	40	ns
t_{AXQX}	t_{OH}	Address transition to output transition	$\overline{E} = V_{IL}$, $\overline{G}V_{PP} = V_{IL}$	0		0		0		ns

1. T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5 V ± 10%.
2. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
3. Speed obtained with High Speed AC measurement conditions.
4. Sampled only, not 100% tested.

Figure 7. Read mode AC waveforms

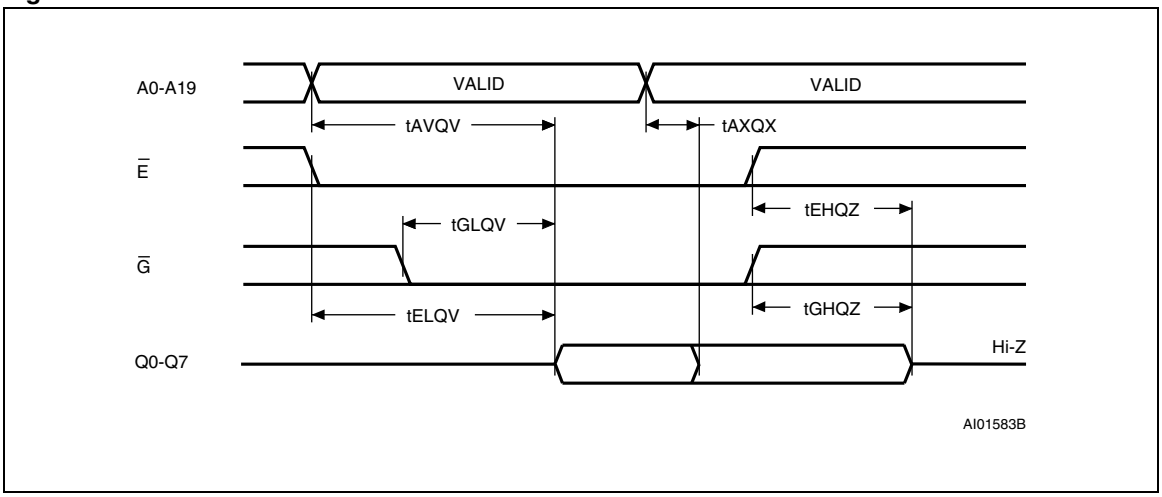


Table 10. Margin mode AC characteristics(1) (2)

Symbol	Alt	Parameter	Test condition	Min	Max	Unit
t_{A9HVPH}	t_{AS9}	V_{A9} high to V_{PP} high		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} high to Chip Enable low		2		µs
t_{A10HEH}	t_{AS10}	V_{A10} high to Chip Enable high (Set)		1		µs
t_{A10LEH}	t_{AS10}	V_{A10} low to Chip Enable high (Reset)		1		µs
t_{EXA10X}	t_{AH10}	Chip Enable transition to V_{A10} transition		1		µs
t_{EXVPX}	t_{VPH}	Chip Enable transition to V_{PP} transition		2		µs
t_{VPXA9X}	t_{AH9}	V_{PP} transition to V_{A9} transition		2		µs

1. T_A = 25 °C; V_{CC} = 6.25 V ± 0.25 V; V_{PP} = 12.75 V ± 0.25 V
2. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Figure 8. Margin mode AC waveforms

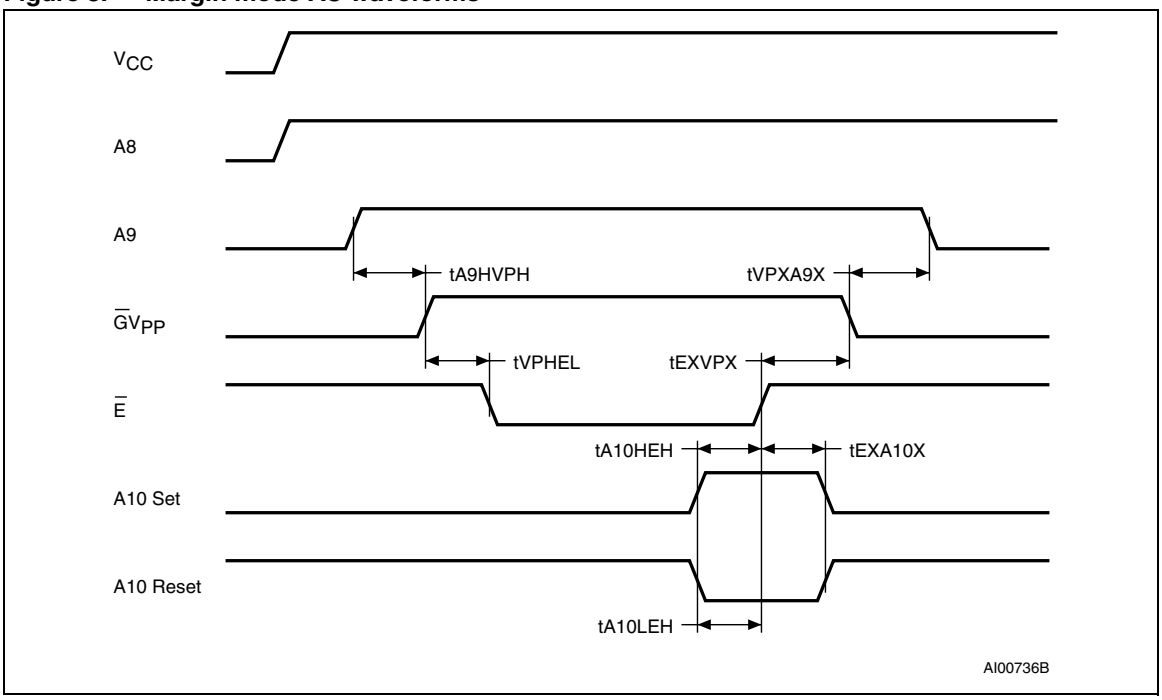
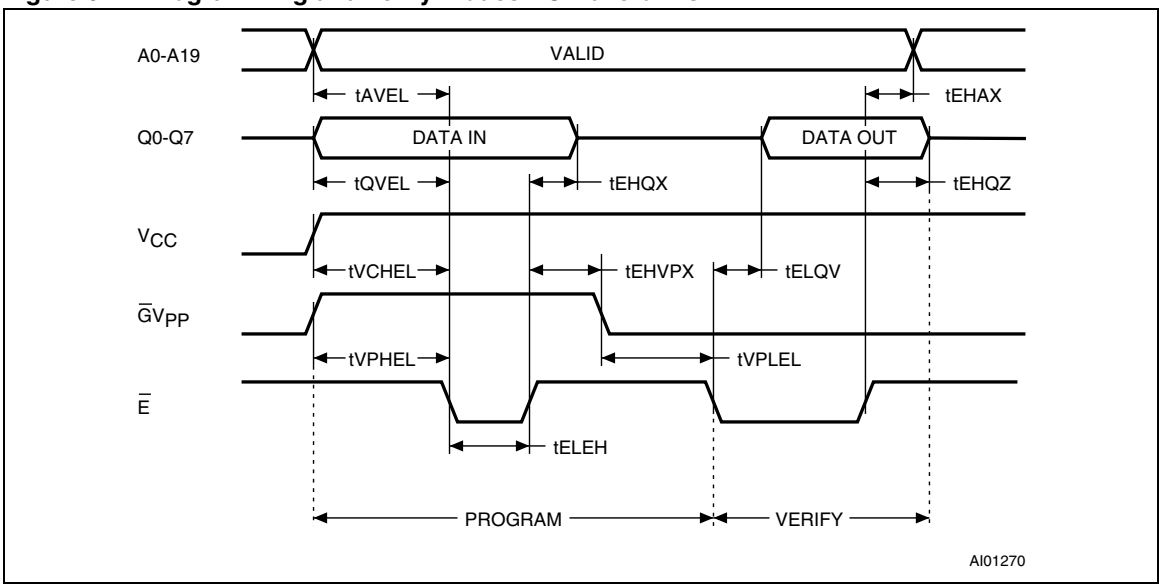


Table 11. Programming mode AC characteristics (1)

Symbol	Alt	Parameter	Test condition	Min.	Max.	Unit
t_{AVEL}	t_{AS}	Address valid to Chip Enable low		2		µs
t_{QVEL}	t_{DS}	Input valid to Chip Enable low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} high to Chip Enable low		2		µs
t_{VPHEL}	t_{OES}	V_{PP} high to Chip Enable low		2		µs
t_{VPLVPH}	t_{PRT}	V_{PP} rise time		50		ns
t_{ELEH}	t_{PW}	Chip Enable program pulse width (initial)		45	55	µs
t_{EHQX}	t_{DH}	Chip Enable high to Input transition		2		µs
t_{EHVPX}	t_{OEH}	Chip Enable high to V_{PP} transition		2		µs
t_{VPLEL}	t_{VR}	V_{PP} low to Chip Enable low		2		µs
t_{ELQV}	t_{DV}	Chip Enable low to output valid			1	µs
t_{EHQZ} (2)	t_{DFP}	Chip Enable high to output Hi-Z		0	130	ns
t_{EHAX}	t_{AH}	Chip Enable high to address transition		0		ns

1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 9. Programming and verify modes AC waveforms



5 Package mechanical data

5.1 32-pin ceramic frit-seal DIP, with round window (FDIP32WA)

Figure 10. FDIP32WA package outline

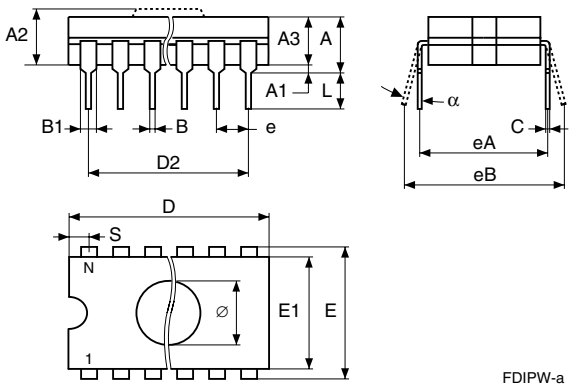


Table 12. FDIP32WA package mechanical data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.72			0.225
A1	0.51		1.40	0.020		0.055
A2	3.91		4.57	0.154		0.180
A3	3.89		4.50	0.153		0.177
B	0.41		0.56	0.016		0.022
B1		1.45			0.057	
C	0.23		0.30	0.009		0.012
D	41.73		42.04	1.643		1.655
D2		38.10			1.500	
e		2.54			0.100	
E		15.24			0.600	
E1	13.06		13.36	0.514		0.526
eA		14.99			0.590	
eB	16.18		18.03	0.637		0.710
L	3.18		4.10	0.125		0.161
N		32			32	
S	1.52		2.49	0.060		0.098
Ø		7.11			0.280	
α	4°		11°	4°		11°

5.2 32-pin plastic DIP, 600 mils width (PDIP32)

Figure 11. PDIP32 package outline

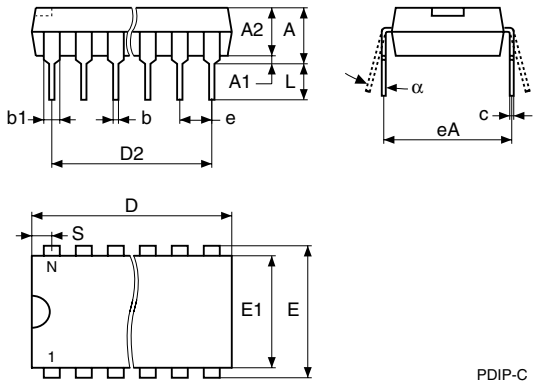


Table 13. PDIP32 package mechanical data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A			4.83			0.190
A1	0.38			0.015		
A2		3.81			0.150	
b	0.41		0.53	0.016		0.021
b1	1.14		1.65	0.045		0.065
c	0.23		0.38	0.009		0.015
D	41.78		42.29	1.645		1.665
D2		38.10			1.500	
eA		15.24			0.600	
e		2.54			0.100	
E	15.24		15.88	0.600		0.625
E1	13.46		13.97	0.530		0.550
S	1.65		2.21	0.065		0.087
L	3.05		3.56	0.120		0.140
α	0°		15°	0°		15°
N	32			32		

6 Part numbering

Table 15. Ordering information scheme

Example: M27C801 -55 K 1

Device type

M27

Supply voltage

C = 5 V ±10%

Device function

801 = 8 Mbit (1Mb x 8)

Speed

-55 (1) = 55 ns

-80 = 80 ns

-90 = 90 ns

-100 = 100 ns

Package

F = FDIP32W

B = PDIP32

K = PLCC32

Temperature range

1 = 0 to 70 °C

6 = –40 to 85 °C

1. High Speed, see *DC and AC characteristics* section for further information.

For a list of available options (speed, package, etc...) or for further information on any aspect of this device, please contact the nearest STMicroelectronics sales office.