



P-Channel JFETs

2N5114JAN/JANTX/JANTXV
2N5115JAN/JANTX/JANTXV
2N5116JAN/JANTX/JANTXV

Table with 5 columns: Part Number, VGS(off) (V), rDS(on) Max (Ω), ID(off) Typ (pA), tON Max (ns). Rows include 2N5114, 2N5115, and 2N5116.

FEATURES

- Low On-Resistance: 2N5114 <75 Ω
• Fast Switching—tON: 16 ns
• High Off-Isolation—ID(off): -10 pA
• Low Capacitance: 6 pF
• Low Insertion Loss

BENEFITS

- Low Error Voltage
• High-Speed Analog Circuit Performance
• Negligible "Off-Error," Excellent Accuracy
• Good Frequency Response
• Eliminates Additional Buffering

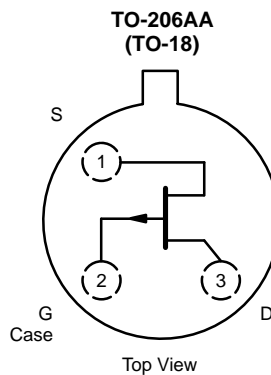
APPLICATIONS

- Analog Switches
• Choppers
• Sample-and-Hold
• Normally "On" Switches
• Current Limiters

DESCRIPTION

The 2N5114JAN/JANTX/JANTXV series consists of p-channel JFET analog switches designed to provide low on-resistance, good off-isolation, and fast switching. These

JFETs are optimized for use in complementary switching applications with the Vishay Siliconix 2N4856A series.



ABSOLUTE MAXIMUM RATINGS

Gate-Drain Voltage 30 V
Gate-Source Voltage 30 V
Gate Current -50 mA
Storage Temperature -65 to 200°C
Operating Junction Temperature -55 to 200°C

Lead Temperature (1/16" from case for 10 sec.) 300°C
Power Dissipationa 500 mW

Notes
a. Derate 3 mW/°C above 25°C

SPECIFICATIONS (T _A = 25 °C UNLESS OTHERWISE NOTED)											
Parameter	Symbol	Test Conditions	Typ ^a	Limits						Unit	
				2N5114		2N5115		2N5116			
				Min	Max	Min	Max	Min	Max		
Static											
Gate-Source Breakdown Voltage	V _{(BR)GSS}	I _G = 1 μA, V _{DS} = 0 V	45	30		30		30		V	
Gate-Source Cutoff Voltage	V _{GS(off)}	V _{DS} = -15 V, I _D = -1 nA		5	10	3	6	1	4		
Saturation Drain Current ^b	I _{DSS}	V _{GS} = 0 V		V _{DS} = -18 V							
				V _{DS} = -15 V			-15	-60	-5	-25	mA
Gate Reverse Current	I _{GSS}	V _{GS} = 20 V, V _{DS} = 0 V				500		500		500	
				T _A = 150 °C	0.01		1		1		1
Gate Operating Current ^c	I _G	V _{DG} = -15 V, I _D = -1 mA	-5								
Drain Cutoff Current	I _{D(off)}	V _{DS} = -15 V		V _{GS} = 12 V	-10		-500				
				V _{GS} = 7 V	-10			-500			pA
				V _{GS} = 5 V	-10					-500	
		V _{DS} = -15 V T _A = 150 °C		V _{GS} = 12 V	-0.02		-1				
				V _{GS} = 7 V	-0.02				-1		
				V _{GS} = 5 V	-0.02					-1	
Drain-Source On-Voltage	V _{DS(on)}	V _{GS} = 0 V		I _D = -15 mA	-1.0		-1.3				
				I _D = -7 mA	-0.7			-0.8			
				I _D = -3 mA	-0.5				-0.6		
Drain-Source On-Resistance	r _{DS(on)}	V _{GS} = 0 V, I _D = -1 mA				75		100		150	Ω
Gate-Source Forward Voltage	V _{GS(F)}	I _G = -1 mA, V _{DS} = 0 V	-0.7		-1		-1		-1		V
Dynamic											
Drain-Source On-Resistance	r _{ds(on)}	V _{GS} = 0 V, I _D = 0 mA, f = 1 kHz				75		100		175	Ω
Common-Source Input Capacitance	C _{iss}	V _{DS} = -15 V, V _{GS} = 0 V f = 1 MHz	20		25		25		27		
Common-Source Reverse Transfer Capacitance	C _{rss}	V _{DS} = 0 V f = 1 MHz		V _{GS} = 12 V	5		7				
				V _{GS} = 7 V	6			7			
				V _{GS} = 5 V	6					7	
Switching											
Turn-On Time	t _{d(on)}	See Switching Circuit				6		10		25	
	t _r				10		20		35		
Turn-Off Time	t _{d(off)}				6		8		20		
	t _f				15		30		60		

Notes

- a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- b. Pulse test: PW ≤ 300 μs duty cycle ≤ 3%.
- c. This parameter not registered with JEDEC.

PSCIA

SWITCHING TIME TEST CIRCUIT			
	2N5114	2N5115	2N5116
V_{DD}	-10 V	-6 V	-6 V
V_{GG}	20 V	12 V	8 V
R_L^*	430 Ω	910 Ω	2000 Ω
R_G^*	100 Ω	220 Ω	390 Ω
$I_{D(on)}$	-15 mA	-7 mA	-3 mA
$V_{GS(H)}$	0 V	0 V	0 V
$V_{GS(L)}$	-11 V	-7 V	-5 V

*Non-inductive

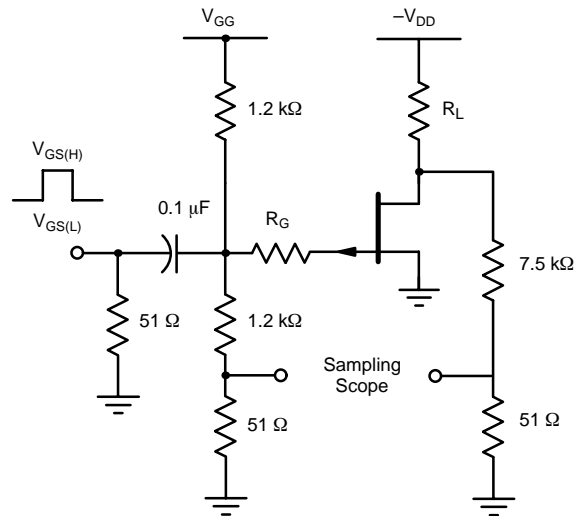
INPUT PULSE

Rise Time < 1 ns
 Fall Time < 1 ns
 Pulse Width 100 ns
 PRF 1 MHz

SAMPLING SCOPE

Rise Time 0.4 ns
 Input Resistance 10 M Ω
 Input Capacitance 1.5 pF

See Typical Characteristics curves for changes.





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