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January 2008

74AC374, 74ACT374
Octal D-Type Flip-Flop with 3-STATE Outputs

Features

- I_{CC} and I_{OZ} reduced by 50%
- Buffered positive edge-triggered clock
- 3-STATE outputs for bus-oriented applications
- Outputs source/sink 24mA
- See 273 for reset version
- See 377 for clock enable version
- See 373 for transparent latch version
- See 574 for broadside pinout version
- See 564 for broadside pinout version with inverted outputs
- ACT374 has TTL-compatible inputs

General Description

The AC/ACT374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.
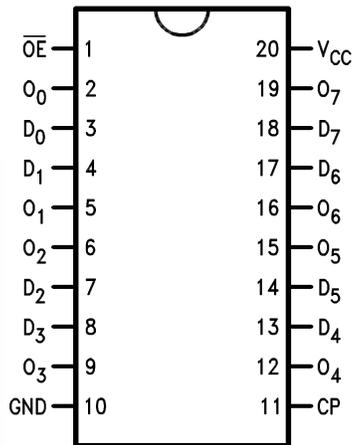
Ordering Information

Order Number	Package Number	Package Description
74AC374SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74AC374SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC374MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC374PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT374SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACT374SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT374MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74ACT374MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT374PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram
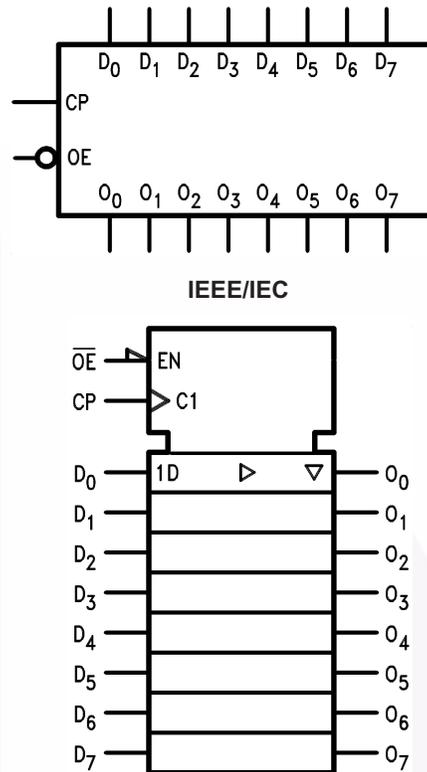
$\overline{OE}$	1	20 V_{CC}
O_0	2	19 O_7
D_0	3	18 D_7
D_1	4	17 D_6
O_1	5	16 O_6
O_2	6	15 O_5
D_2	7	14 D_5
D_3	8	13 D_4
O_3	9	12 O_4
GND	10	11 CP

Pin Description

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	3-STATE Output Enable Input
O_0–O_7	3-STATE Outputs

Functional Description

The AC/ACT374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Logic Symbols

D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7

CP

OE

O_0 O_1 O_2 O_3 O_4 O_5 O_6 O_7

IEEE/IEC

$\overline{OE}$	EN	
CP	C1	
D_0	1D	O_0
D_1		O_1
D_2		O_2
D_3		O_3
D_4		O_4
D_5		O_5
D_6		O_6
D_7		O_7

Truth Table

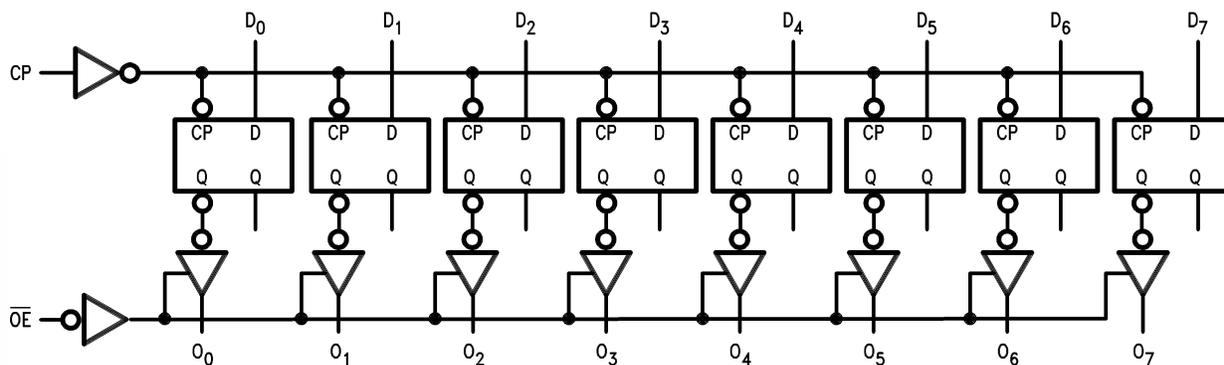| Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H	⌐	L	H
L	⌐	L	L
X	X	H	Z

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

⌐ = LOW-to-HIGH Transition

Logic Diagram

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	−0.5V to +7.0V
I_{IK}	DC Input Diode Current	
	$V_I = -0.5V$	−20mA
	$V_I = V_{CC} + 0.5$	+20mA
V_I	DC Input Voltage	−0.5V to V_{CC} + 0.5V
I_{OK}	DC Output Diode Current	
	$V_O = -0.5V$	−20mA
	$V_O = V_{CC} + 0.5V$	+20mA
V_O	DC Output Voltage	−0.5V to V_{CC} + 0.5V
I_O	DC Output Source or Sink Current	±50mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin	±50mA
T_{STG}	Storage Temperature	−65°C to +150°C
T_J	Junction Temperature	140°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	
	AC	2.0V to 6.0V
	ACT	4.5V to 5.5V
V_I	Input Voltage	0V to V_{CC}
V_O	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	−40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate, AC Devices: V_{IN} from 30% to 70% of V_{CC}, V_{CC} @ 3.3V, 4.5V, 5.5V	125mV/ns
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACT Devices: V_{IN} from 0.8V to 2.0V, V_{CC} @ 4.5V, 5.5V	125mV/ns

DC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C Typ.	T_A = +25°C Guaranteed Limits	T_A = −40°C to +85°C Guaranteed Limits	Units
V_{IH}	Minimum HIGH Level Input Voltage	3.0	V_{OUT} = 0.1V or V_{CC} − 0.1V	1.5	2.1	2.1	V
		4.5		2.25	3.15	3.15	
		5.5		2.75	3.85	3.85	
V_{IL}	Maximum LOW Level Input Voltage	3.0	V_{OUT} = 0.1V or V_{CC} − 0.1V	1.5	0.9	0.9	V
		4.5		2.25	1.35	1.35	
		5.5		2.75	1.65	1.65	
V_{OH}	Minimum HIGH Level Output Voltage	3.0	I_{OUT} = −50µA	2.99	2.9	2.9	V
		4.5		4.49	4.4	4.4	
		5.5		5.49	5.4	5.4	
		3.0	V_{IN} = V_{IL} or V_{IH}, I_{OH} = −12mA		2.56	2.46	
		4.5	V_{IN} = V_{IL} or V_{IH}, I_{OH} = −24mA		3.86	3.76	
		5.5	V_{IN} = V_{IL} or V_{IH}, I_{OH} = −24mA[1]		4.86	4.76	
V_{OL}	Maximum LOW Level Output Voltage	3.0	I_{OUT} = 50µA	0.002	0.1	0.1	V
		4.5		0.001	0.1	0.1	
		5.5		0.001	0.1	0.1	
		3.0	V_{IN} = V_{IL} or V_{IH}, I_{OL} = 12mA		0.36	0.44	
		4.5	V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24mA		0.36	0.44	
		5.5	V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24mA[1]		0.36	0.44	
I_{IN}[2]	Maximum Input Leakage Current	5.5	V_I = V_{CC}, GND		±0.1	±1.0	µA
I_{OZ}	Maximum 3-STATE Leakage Current	5.5	V_I (OE) = V_{IL}, V_{IH}; V_I = V_{CC}, GND; V_O = V_{CC}, GND		±0.25	±2.5	µA
I_{OLD}	Minimum Dynamic Output Current[3]	5.5	V_{OLD} = 1.65V Max.			75	mA
I_{OHD}		5.5	V_{OHD} = 3.85V Min.			−75	mA
I_{CC}[2]	Maximum Quiescent Supply Current	5.5	V_{IN} = V_{CC} or GND		4.0	40.0	µA

Notes:

1. All outputs loaded; thresholds on input associated with output under test.

2. I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

3. Maximum test duration 2.0ms, one output loaded at a time.

DC Electrical Characteristics for ACT

Symbol	Parameter	V$_{CC}$ (V)	Conditions	T$_A$ = +25°C Typ.	Guaranteed Limits	T$_A$ = −40°C to +85°C	Units
V$_{IH}$	Minimum HIGH Level Input Voltage	4.5	V$_{OUT}$ = 0.1V or V$_{CC}$ − 0.1V	1.5	2.0	2.0	V
		5.5		1.5	2.0	2.0	
V$_{IL}$	Maximum LOW Level Input Voltage	4.5	V$_{OUT}$ = 0.1V or V$_{CC}$ − 0.1V	1.5	0.8	0.8	V
		5.5		1.5	0.8	0.8	
V$_{OH}$	Minimum HIGH Level Output Voltage	4.5	I$_{OUT}$ = −50µA	4.49	4.4	4.4	V
		5.5		5.49	5.4	5.4	
		4.5	V$_{IN}$ = V$_{IL}$ or V$_{IH}$, I$_{OH}$ = −24mA		3.86	3.76	
		5.5	V$_{IN}$ = V$_{IL}$ or V$_{IH}$, I$_{OH}$ = −24mA[4]		4.86	4.76	
V$_{OL}$	Maximum LOW Level Output Voltage	4.5	I$_{OUT}$ = 50µA	0.001	0.1	0.1	V
		5.5		0.001	0.1	0.1	
		4.5	V$_{IN}$ = V$_{IL}$ or V$_{IH}$, I$_{OL}$ = 24mA		0.36	0.44	
		5.5	V$_{IN}$ = V$_{IL}$ or V$_{IH}$, I$_{OL}$ = 24mA[4]		0.36	0.44	
I$_{IN}$	Maximum Input Leakage Current	5.5	V$_I$ = V$_{CC}$, GND		±0.1	±1.0	µA
I$_{OZ}$	Maximum 3-STATE Leakage Current	5.5	V$_I$ = V$_{IL}$, V$_{IH}$; V$_O$ = V$_{CC}$, GND		±0.25	±2.5	µA
I$_{CCT}$	Maximum I$_{CC}$/Input	5.5	V$_I$ = V$_{CC}$ − 2.1V	0.6		1.5	mA
I$_{OLD}$	Minimum Dynamic Output Current[5]	5.5	V$_{OLD}$ = 1.65V Max.			75	mA
I$_{OHD}$		5.5	V$_{OHD}$ = 3.85V Min.			−75	mA
I$_{CC}$	Maximum Quiescent Supply Current	5.5	V$_{IN}$ = V$_{CC}$ or GND		4.0	40.0	µA

Notes:

4. All outputs loaded; thresholds on input associated with output under test.

5. Maximum test duration 2.0ms, one output loaded at a time.

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AC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)[6]	$T_A = +25°C$, $C_L = 50pF$			$T_A = -40°C$ to $+85°$, $C_L = 50pF$		Units
			Min.	Typ.	Max.	Min.	Max.	
f_{MAX}	Maximum Clock Frequency	3.3	60	110		60		MHz
		5.0	100	155		100		
t_{PLH}	Propagation Delay, CP to O_n	3.3	3.0	11.0	13.5	1.5	15.5	ns
		5.0	2.5	8.0	9.5	1.5	10.5	
t_{PHL}	Propagation Delay, CP to O_n	3.3	2.5	10.0	12.5	2.0	14.0	ns
		5.0	2.0	7.0	9.0	1.5	10.0	
t_{PZH}	Output Enable Time	3.3	3.0	9.5	11.5	1.5	13.0	ns
		5.0	2.0	7.0	8.5	1.0	9.5	
t_{PZL}	Output Enable Time	3.3	2.5	9.0	11.5	1.5	13.0	ns
		5.0	2.0	6.5	8.5	1.0	9.5	
t_{PHZ}	Output Disable Time	3.3	3.0	10.5	12.5	2.0	14.5	ns
		5.0	2.0	8.0	11.0	2.0	12.5	
t_{PLZ}	Output Disable Time	3.3	2.0	8.0	11.5	1.0	12.5	ns
		5.0	1.5	6.5	8.5	1.0	10.0	

Note:
6. Voltage range 3.3 is 3.3V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V.

AC Operating Requirements for AC

Symbol	Parameter	V_{CC} (V)[7]	$T_A = +25°C$, $C_L = 50pF$	$T_A = -40°C$ to $+85°C$, $C_L = 50pF$		Units
			Typ.	Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW, D_n to CP	3.3	2.0	5.5	6.0	ns
		5.0	1.0	4.0	4.5	
t_H	Hold Time, HIGH or LOW, D_n to CP	3.3	−1.0	1.0	1.0	ns
		5.0	0	1.5	1.5	
t_W	CP Pulse Width, HIGH or LOW	3.3	4.0	5.5	6.0	ns
		5.0	2.5	4.0	4.5	

Note:
7. Voltage range 3.3 is 3.3V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V.

AC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V)[8]	$T_A = +25°C$, $C_L = 50pF$			$T_A = -40°C$ to $+85°C$, $C_L = 50pF$		Units
			Min.	Typ.	Max.	Min.	Max.	
f_{MAX}	Maximum Clock Frequency	5.0	100	160		90		MHz
t_{PLH}	Propagation Delay, CP to O_n	5.0	2.0	8.5	10.0	2.0	11.5	ns
t_{PHL}	Propagation Delay, CP to O_n	5.0	2.0	8.0	9.5	1.5	11.0	ns
t_{PZH}	Output Enable Time	5.0	2.0	8.0	9.5	1.5	10.5	ns
t_{PZL}	Output Enable Time	5.0	1.5	8.0	9.0	1.5	10.5	ns
t_{PHZ}	Output Disable Time	5.0	1.5	8.5	11.5	1.0	12.5	ns
t_{PLZ}	Output Disable Time	5.0	1.5	7.0	8.5	1.0	10.0	ns

Note:
8. Voltage range 5.0 is 5.0V $\pm$ 0.5V.

AC Operating Requirements for ACT

Symbol	Parameter	V_{CC} (V)[9]	$T_A = +25°C$, $C_L = 50pF$	$T_A = -40°C$ to $+85°C$, $C_L = 50pF$	Units
			Typ.	Guaranteed Minimum	
t_S	Setup Time, HIGH or LOW, D_n to CP	5.0	1.0	5.5	5.5	ns
t_H	Hold Time, HIGH or LOW, D_n to CP	5.0	0	1.5	1.5	ns
t_W	CP Pulse Width, HIGH or LOW	5.0	2.5	5.0	5.0	ns

Note:
9. Voltage range 5.0 is 5.0V $\pm$ 0.5V.

Capacitance

Symbol	Parameter	Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = OPEN	4.5	pF

Physical Dimensions

LAND PATTERN RECOMMENDATION

NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC
   MS-013, VARIATION AC, ISSUE E
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD
   FLASH OR BURRS.
D) CONFORMS TO ASME Y14.5M-1994
E) LANDPATTERN STANDARD: SOIC127P1030X265-20L
F) DRAWING FILENAME: MKT-M20BREV3

DETAIL A
SCALE: 2:1
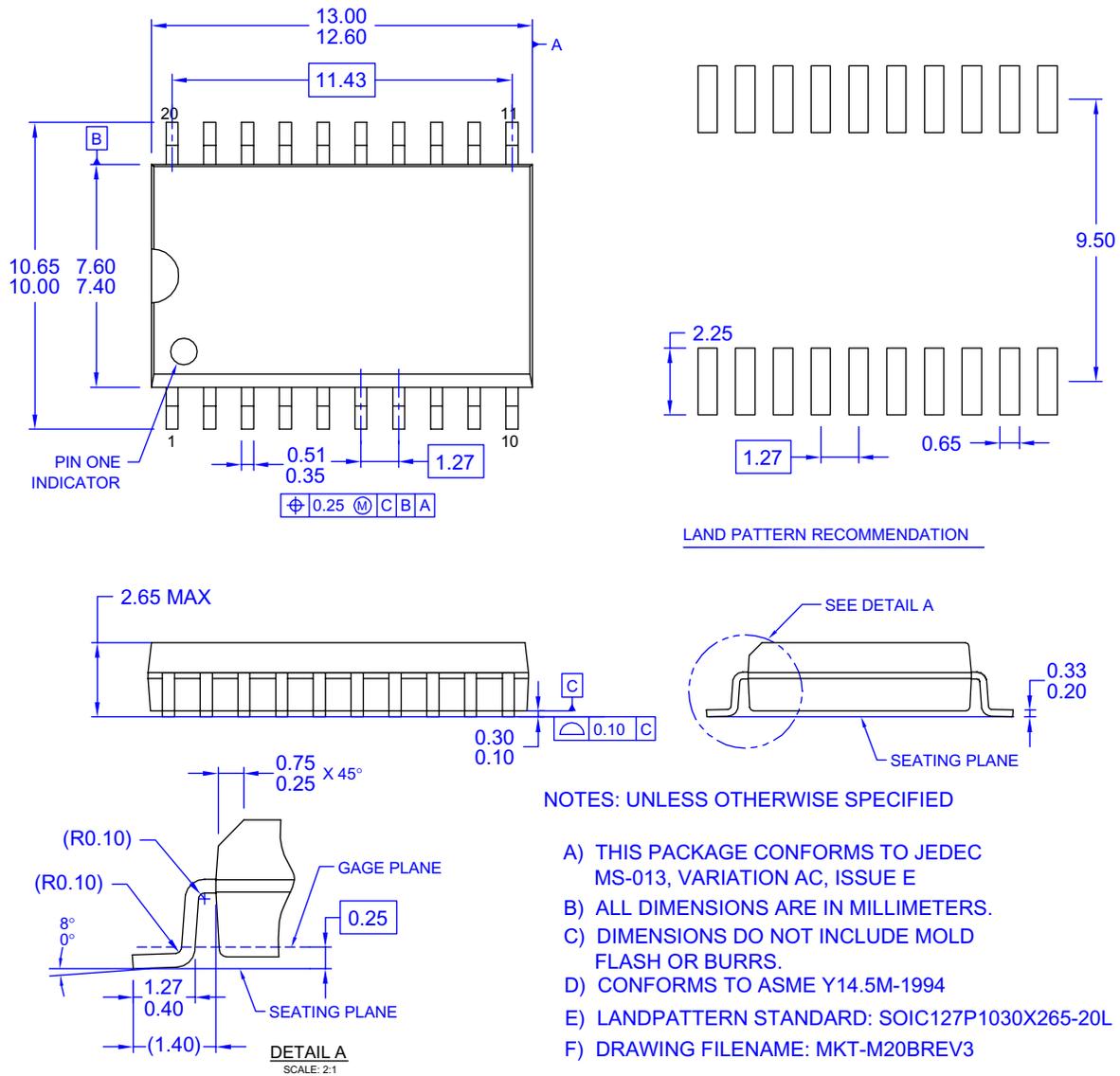
Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
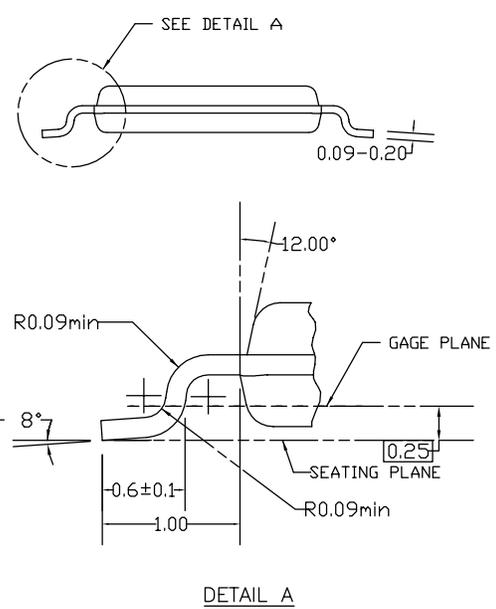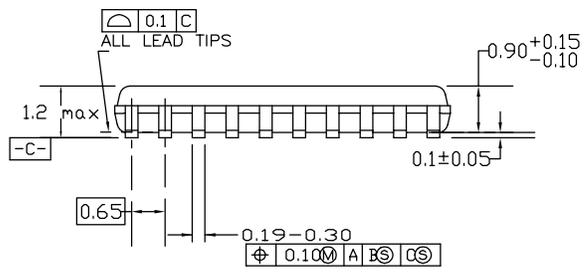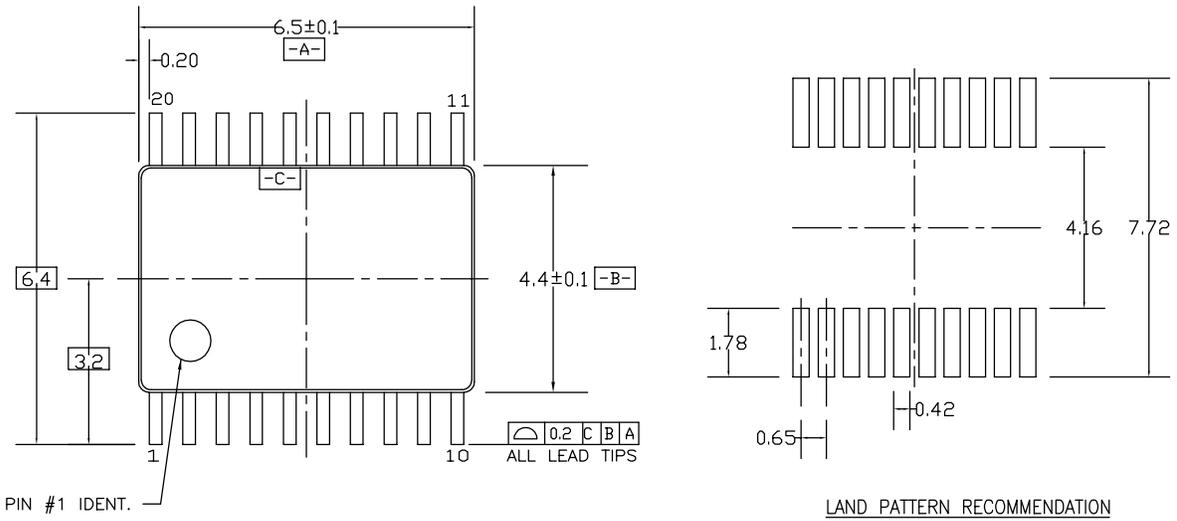
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Physical Dimensions (Continued)

12.6±0.10
−A−

0.40 TYP

20   11

7.8

3.9

5.3±0.10
−B−

PIN #1 IDENT.   1   10

| △ | 0.2 | C | B | A |

ALL LEAD TIPS

LAND PATTERN RECOMMENDATION

20 19   12 11

5.01 TYP
9.27 TYP

(2.13 TYP)

1   2   9   10

1.27 TYP   0.6 TYP

ALL LEAD TIPS

| △ | 0.1 | C |

2.1 MAX.

−C−

1.27 TYP

1.8±0.1

0.15±0.05

0.35−0.51

| ⊕ | 0.12 Ⓜ | C | A |

DIMENSIONS ARE IN MILLIMETERS

NOTES:
A. CONFORMS TO EIAJ EDR−7320 REGISTRATION,
   ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD
   FLASH, AND TIE BAR EXTRUSIONS.

M20DREVC

SEE DETAIL A

0.15−0.25

7° TYP

GAGE PLANE

0.25

0°−8° TYP

0.60±0.15

1.25

SEATING PLANE

DETAIL A

Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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Physical Dimensions (Continued)

6.5±0.1
-A-
0.20
20 11
-C-
6.4
3.2
4.4±0.1 -B-
0.2 C B A
1 10 ALL LEAD TIPS
PIN #1 IDENT.

4.16   7.72
1.78
0.42
0.65

LAND PATTERN RECOMMENDATION

0.1 C
ALL LEAD TIPS
0.90 +0.15 −0.10
1.2 max
-C-
0.1±0.05
0.65
0.19−0.30
0.10 M A B S C S

DIMENSIONS ARE IN MILLIMETERS

SEE DETAIL A
0.09−0.20

12.00°
R0.09min
GAGE PLANE
0 − 8°
0.25
SEATING PLANE
0.6±0.1
R0.09min
1.00

DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC,
   REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH,
   AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

Figure 3. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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Physical Dimensions (Continued)
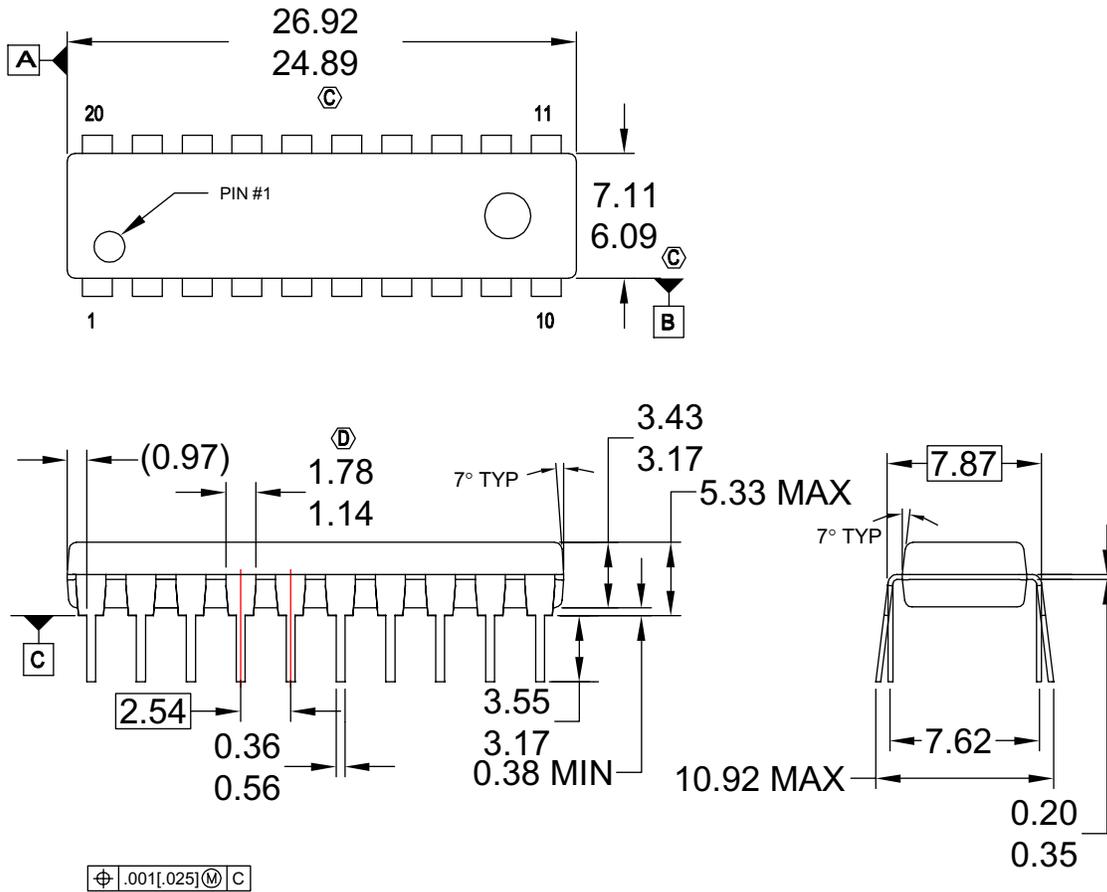
NOTES:
A. CONFORMS TO JEDEC REGISTRATION MS-001, VARIATIONS AD.
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25MM.
D. DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED 0.25MM.
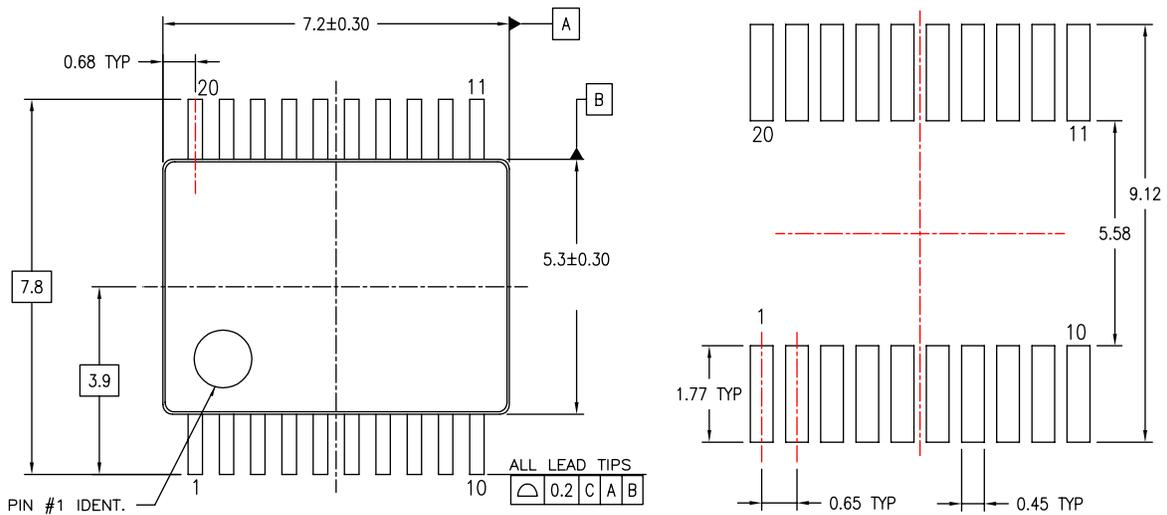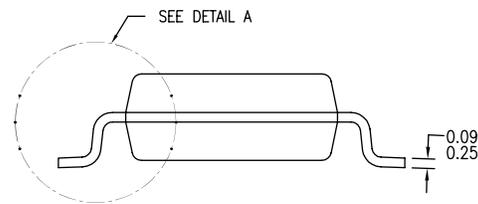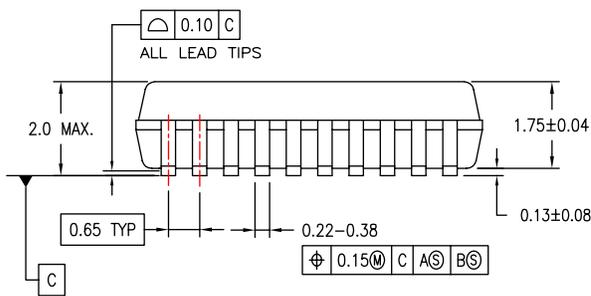E. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
F. DRAWING FILE NAME: N20AREV8

Figure 4. 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

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Physical Dimensions (Continued)

7.2±0.30 — A

0.68 TYP

20   11   B

5.3±0.30

7.8

3.9

PIN #1 IDENT.

1   10

ALL LEAD TIPS
△ 0.2 C A B

20   11

9.12

5.58

1   10

1.77 TYP

0.65 TYP   0.45 TYP

LAND PATTERN RECOMMENDATIONS

△ 0.10 C
ALL LEAD TIPS

2.0 MAX.   1.75±0.04

0.65 TYP   0.13±0.08

0.22−0.38

⊕ 0.15Ⓜ C AⓈ BⓈ

C

DIMENSIONS ARE IN MILLIMETERS

SEE DETAIL A

0.09
0.25

0° MIN.   GAGE PLANE

0.25

0° − 8°

0.75±0.2   SEATING PLANE

(1.25)

DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO−150,
VARIATION AE, DATE 1/94.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH,
AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M − 1994.
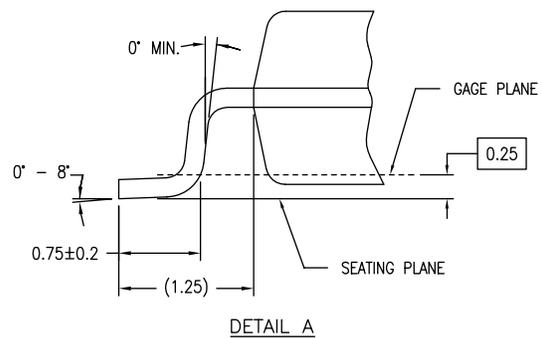
MSA20REVB

Figure 5. 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide

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		SuperSOT™-6	
		SuperSOT™-8	

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