NAND Flash and Mobile LPDRAM 168-Ball Package-on-Package (PoP) MCP Combination Memory (TI OMAP™)

MT29CxGxxMAxxxxx

Features

- Micron® NAND Flash and LPDRAM components
- RoHS-compliant, "green" package
- Separate NAND Flash and LPDRAM interfaces
- Space-saving multichip package/package-on-package combination
- Low-voltage operation (1.70–1.95V)
- Industrial temperature range: –40°C to +85°C

NAND Flash-Specific Features

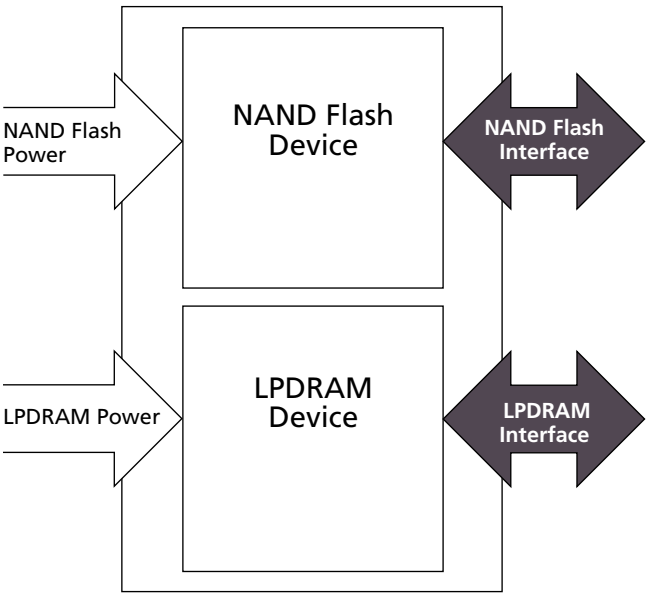
Organization

- Page size
  - x8: 2112 bytes (2048 + 64 bytes)
  - x16: 1056 words (1024 + 32 words)
- Block size: 64 pages (128K + 4K bytes)

Mobile LPDRAM-Specific Features

- No external voltage reference required
- No minimum clock rate requirement
- 1.8V LVCMOS-compatible inputs
- Programmable burst lengths
- Partial-array self refresh (PASR)
- Deep power-down (DPD) mode
- Selectable output drive strength
- STATUS REGISTER READ (SRR) supported[1]

Figure 1: PoP Block Diagram



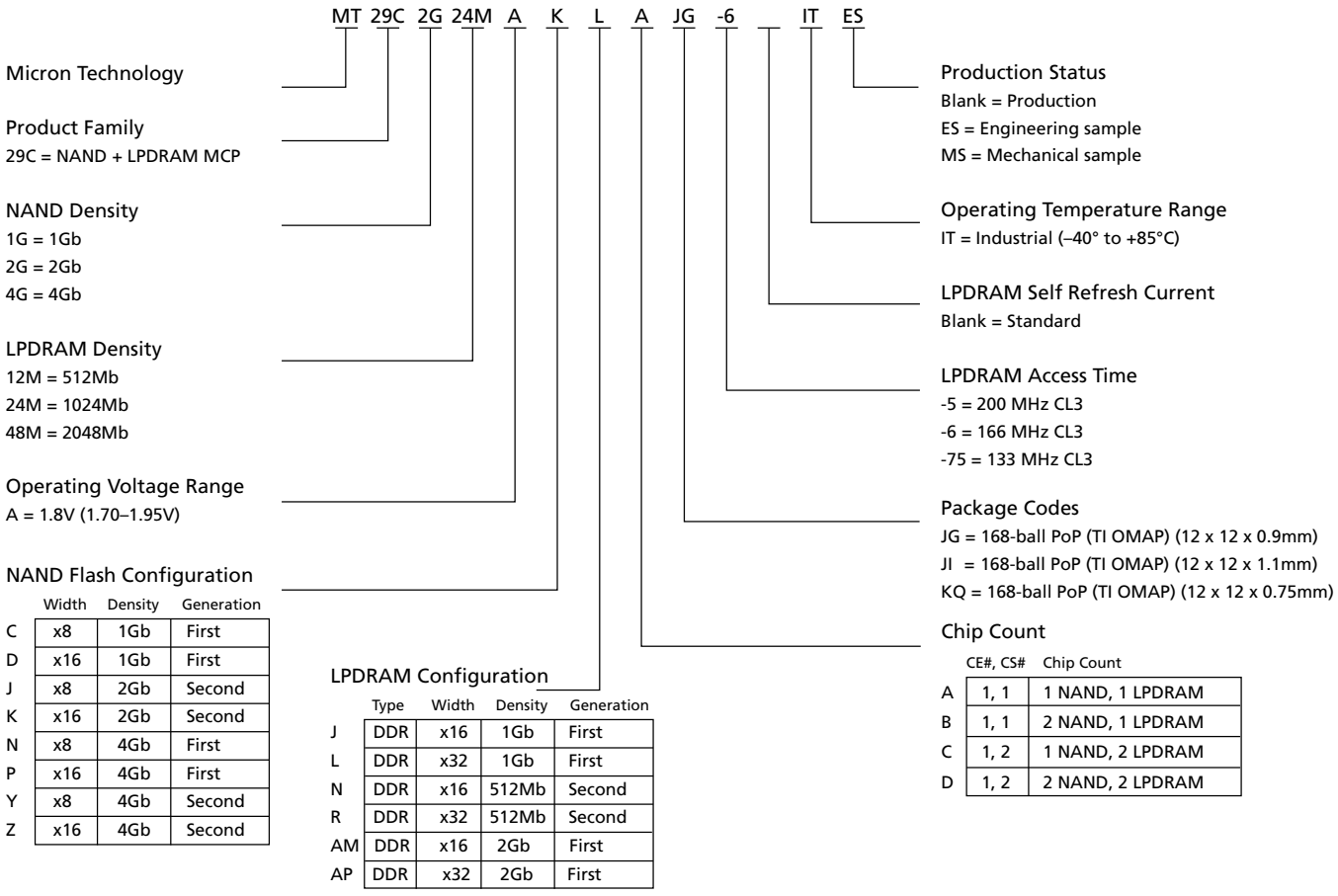
Options[2]	Marking
• Mobile LPDRAM	
– 200 MHz CL3[3]	-5
– 166 MHz CL3	-6
– 133 MHz CL3	-75

Notes:
1. Contact factory for remapped SRR output.
2. For part numbering and physical part markings, see Figure 2 (page 2) and Table 1 (page 3).
3. CL = CAS (READ) latency.

Part Numbering Information

Micron NAND Flash and LPDRAM devices are available in different configurations and densities.

Figure 2: 168-Ball Part Number Chart



	Width	Density	Generation
C	x8	1Gb	First
D	x16	1Gb	First
J	x8	2Gb	Second
K	x16	2Gb	Second
N	x8	4Gb	First
P	x16	4Gb	First
Y	x8	4Gb	Second
Z	x16	4Gb	Second

	Type	Width	Density	Generation
J	DDR	x16	1Gb	First
L	DDR	x32	1Gb	First
N	DDR	x16	512Mb	Second
R	DDR	x32	512Mb	Second
AM	DDR	x16	2Gb	First
AP	DDR	x32	2Gb	First

	CE#, CS#	Chip Count
A	1, 1	1 NAND, 1 LPDRAM
B	1, 1	2 NAND, 1 LPDRAM
C	1, 2	1 NAND, 2 LPDRAM
D	1, 2	2 NAND, 2 LPDRAM

Note: 1. Not all possible combinations are available. Contact factory for availability.

Table 1: Production Part Numbers

Part Number	NAND Product	LPDDR Product	Physical Part Marking
MT29C2G24MAKLAJG-6 IT	MT29F2G16ABDHC-ET	MT46H32M32LFJG-6 IT	JW192
MT29C2G24MAKLAJG-75 IT	MT29F2G16ABDHC-ET	MT46H32M32LFJG-6 IT	JW193
MT29C2G48MAKLCJI-6 IT	MT29F2G16ABDHC-ET	MT46H32M32LFJG-6 IT	JW256
MT29C2G48MAKLCJI-75 IT	MT29F2G16ABDHC-ET	MT46H32M32LFJG-6 IT	JW255
MT29C4G48MAPLCJG-6 IT	MT29F4G16ABCWC-ET	MT46H32M32LFJG-6 IT	JW426
MT29C4G48MAPLCJI-6 IT	MT29F4G16ABCWC-ET	MT46H32M32LFJG-6 IT	JW295
MT29C4G48MAPLCJI-75 IT	MT29F4G16ABCWC-ET	MT46H32M32LFJG-6 IT	JW294

Device Marking

Due to the size of the package, the Micron-standard part number is not printed on the top of the device. Instead, an abbreviated device mark consisting of a 5-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at the FBGA Part Marking Decoder site: www.micron.com/decoder. To view the location of the abbreviated mark on the device, refer to customer service note CSN-11, "Product Mark/Label," at www.micron.com/csn.

MCP General Description

Micron package-on-package (PoP) MCP products combine NAND Flash and Mobile LPDRAM devices in a single MCP. These products target mobile applications with low-power, high-performance, and minimal package-footprint design requirements. The NAND Flash and Mobile LPDRAM devices are also members of the Micron discrete memory products portfolio.

The NAND Flash and Mobile LPDRAM devices are packaged with separate interfaces (no shared address, control, data, or power balls). This bus architecture supports an optimized interface to processors with separate NAND Flash and Mobile LPDRAM buses. The NAND Flash and Mobile LPDRAM devices have separate core power connections and share a common ground (that is, Vss is tied together on the two devices).

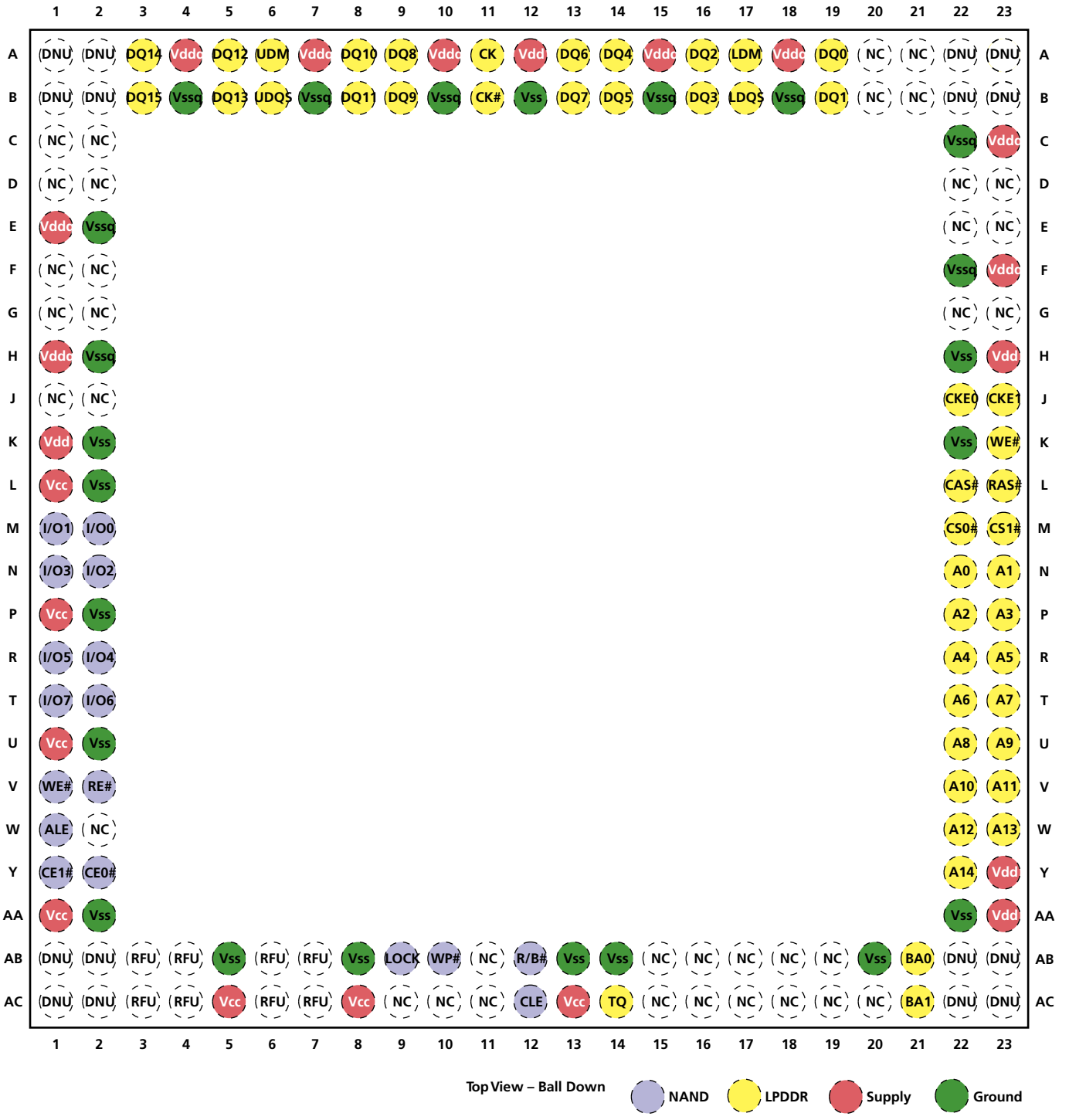
The bus architecture of this device also supports separate NAND Flash and Mobile LPDRAM functionality without concern for device interaction. Operational characteristics for the NAND Flash and Mobile LPDRAM devices are found in the standard Micron data sheets for each of the discrete devices.

For device specifications and complete Micron NAND Flash features documentation, refer to the component data sheet at www.micron.com/nand, or contact your local Micron sales office.

For device specifications and complete Mobile LPDRAM features documentation, refer to the component data sheet at www.micron.com/products/mobiledram, or contact your local Micron sales office.

Ball Assignments and Descriptions

Figure 3: 168-Ball VFBGA (NAND x8; LPDDR x16) Ball Assignments



Note: 1. Contact factory for availability of x16 LPDDR configuration.

Figure 4: 168-Ball VFBGA (NAND x16; LPDDR x32) Ball Assignments

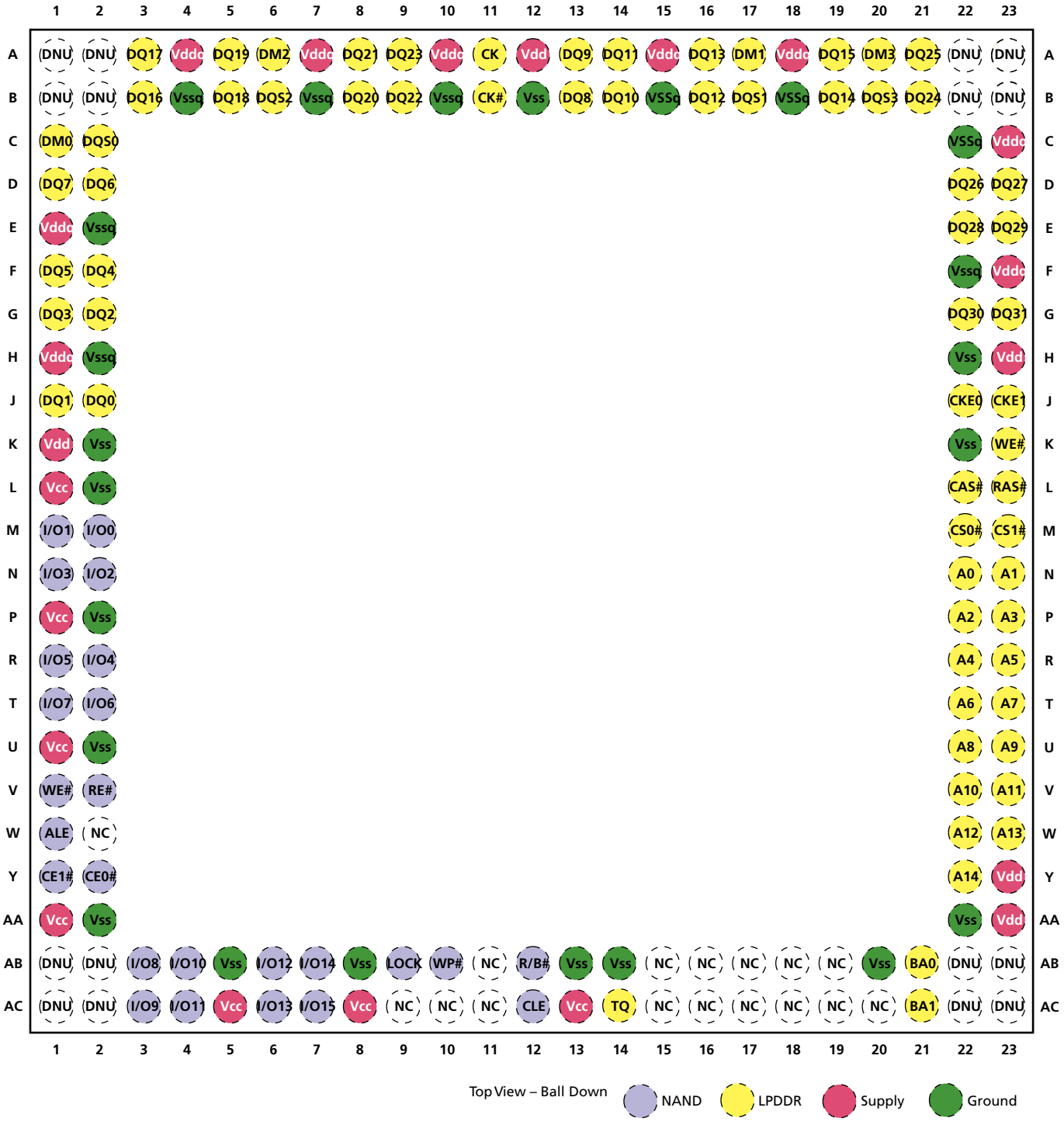


Table 2: x8, x16 NAND Ball Descriptions

Symbol	Type	Description
ALE	Input	Address latch enable: When ALE is HIGH, addresses can be transferred to the on-chip address register.
CE0#, CE1#	Input	Chip enable: Gates transfers between the host system and the NAND device. CE1# is used when a second CE# is required and is RFU in all other configurations.
CLE	Input	Command latch enable: When CLE is HIGH, commands can be transferred to the on-chip command register.
LOCK	Input	When LOCK is HIGH during power-up, the BLOCK LOCK function is enabled. To disable BLOCK LOCK, connect LOCK to Vss during power-up, or leave it unconnected (internal pull-down).
RE#	Input	Read enable: Gates information from the NAND device to the host system.
WE#	Input	Write enable: Gates information from the host system to the NAND device.
WP#	Input	Write protect: Driving WP# LOW blocks ERASE and PROGRAM operations.
I/O[7:0] (x8) I/O[15:0] (x16)	Input/ output	Data inputs/outputs: The bidirectional I/Os transfer address, data, and instruction information. Data is output only during READ operations; at other times the I/Os are inputs. I/O[15:8] are RFU[1] for NAND x8 devices.
R/B#	Output	Ready/busy: Open-drain, active-LOW output that indicates when an internal operation is in progress.
Vcc	Supply	Vcc: NAND power supply.

Note: 1. Balls marked RFU may or may not be connected internally. These balls should not be used. Contact factory for details.

Table 3: x16, x32 LPDDR Ball Descriptions

Symbol	Type	Description
A[14:0] (x16) A[14:0] (x32)	Input	Address inputs: Specifies the row or column address. Also used to load the mode registers. The maximum LPDDR address is determined by density and configuration. Consult the LPDDR product data sheet for the maximum address for a given density and configuration. Unused address balls become RFU.[1]
BA0, BA1	Input	Bank address inputs: Specifies one of the 4 banks.
CAS#	Input	Column select: Specifies which command to execute.
CK, CK#	Input	CK is the system clock. CK and CK# are differential clock inputs. All address and control signals are sampled and referenced on the crossing of the rising edge of CK with the falling edge of CK#.
CKE0, CKE1	Input	Clock enable. CKE0 is used for a single LPDDR product. CKE1 is used for dual LPDDR products and is considered RFU for single LPDDR MCPs.
CS0#, CS1#	Input	Chip select: CS0# is used for a single LPDDR product. CS1# is used for dual LPDDR products and is considered RFU for single LPDDR MCPs.
UDM, LDM (x16) DM[3:0] (x32)	Input	Data mask: Determines which bytes are written during WRITE operations. For x16 LPDDR, unused DM balls become RFU.
RAS#	Input	Row select: Specifies the command to execute.
WE#	Input	Write enable: Specifies the command to execute.
DQ[15:0] (x16) DQ[31:0] (x32)	Input/ output	Data bus: Data inputs/outputs. DQ[31:16] are RFU for x16 LPDDR devices.
UDQS, LDQS (x16) DQS[3:0] (x32)	Input/ output	Data strobe: Coordinates READ/WRITE transfers of data; one DQS per DQ byte. For x16 LPDDR, unused DQS balls become RFU.
TQ	Output	Temperature sensor output: TQ HIGH when LPDDR T_J exceeds 85°C.
Vdd	Supply	Vdd: LPDDR power supply.
Vddq	Supply	Vddq: LPDDR I/O power supply.
Vssq	Supply	Vssq: LPDDR I/O ground.

Note: 1. Balls marked RFU may or may not be connected internally. These balls should not be used. Contact factory for details.

Table 4: Non-Device-Specific Descriptions

Symbol	Type	Description
Vss	Supply	Vss: Shared ground.
Symbol	**Type**	**Description**
DNU	–	Do not use: Must be grounded or left floating.
NC	–	No connect: Not internally connected.
RFU[1]	–	Reserved for future use.

Note: 1. Balls marked RFU may or may not be connected internally. These balls should not be used. Contact factory for details.

Electrical Specifications

Table 5: Absolute Maximum Ratings

Parameters/Conditions	Symbol	Min	Max	Unit
Vcc, Vdd, Vddq supply voltage relative to Vss	Vcc, Vdd, Vddq	–1.0	2.4	V
Voltage on any pin relative to Vss	Vin	–0.5	2.4 or (supply voltage[1] + 0.3V), whichever is less	V
Storage temperature range	–	–55	+150	°C

Note: 1. Supply voltage references Vcc, Vdd, or Vddq.

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 6: Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc, Vdd	1.70	1.80	1.95	V
I/O supply voltage	Vddq	1.70	1.80	1.95	V
Operating temperature range	–	–40	–	+85	°C

Device Diagrams

Figure 5: 168-Ball (Single LPDDR) Functional Block Diagram

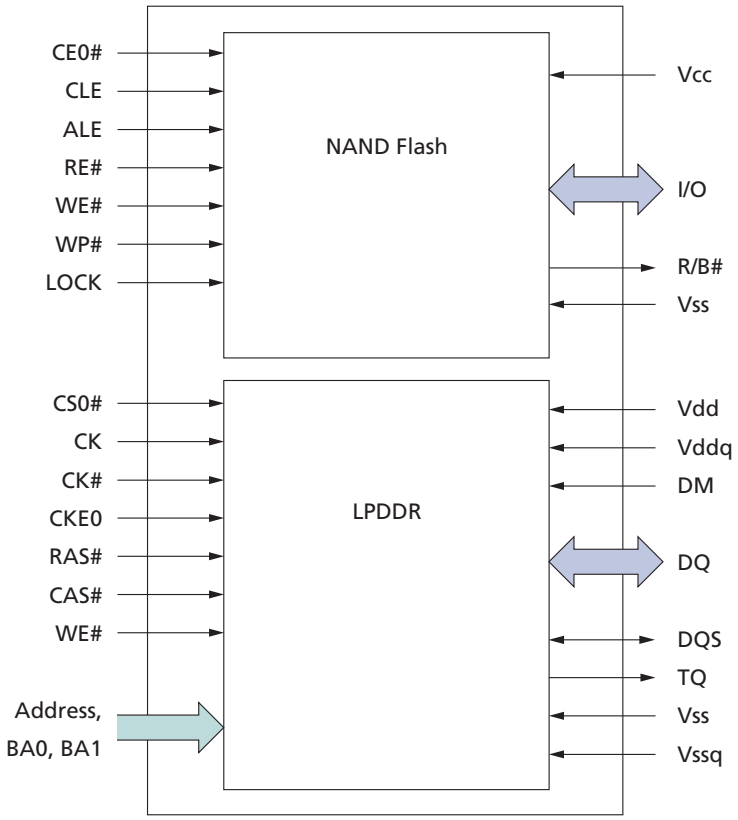
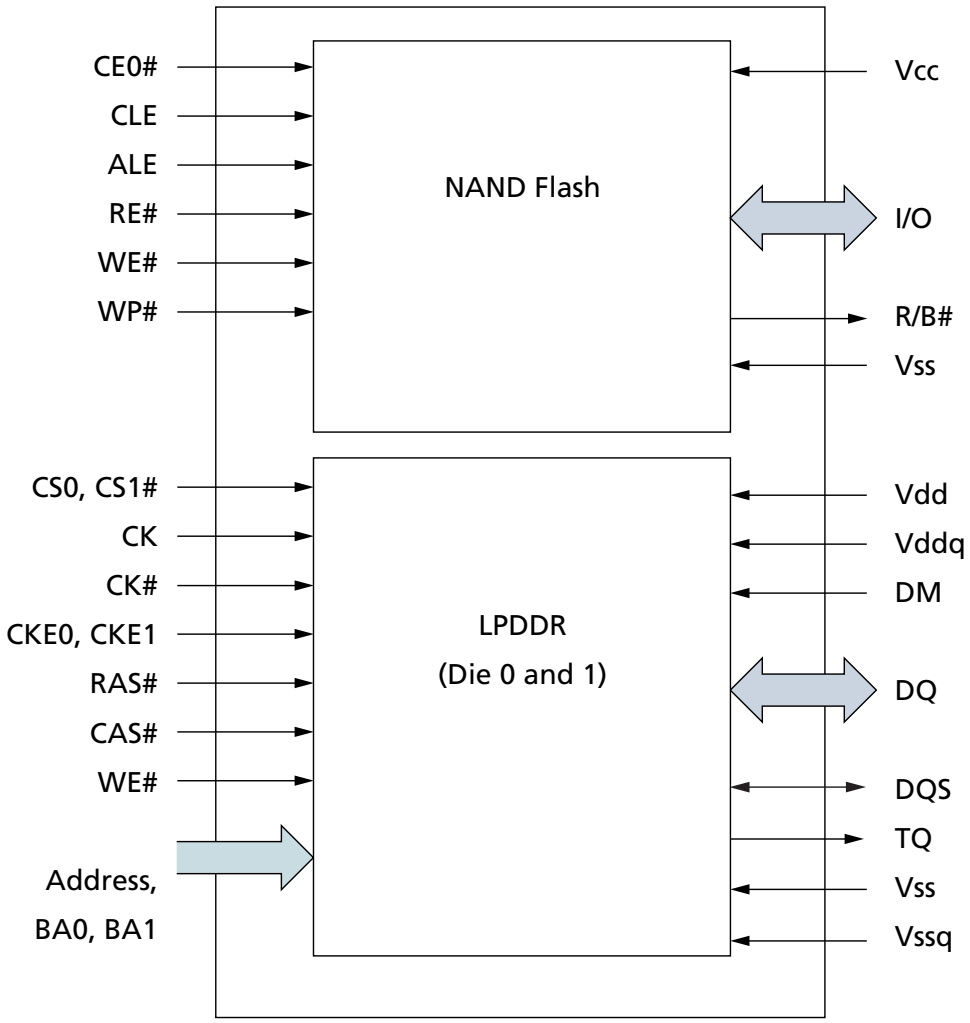
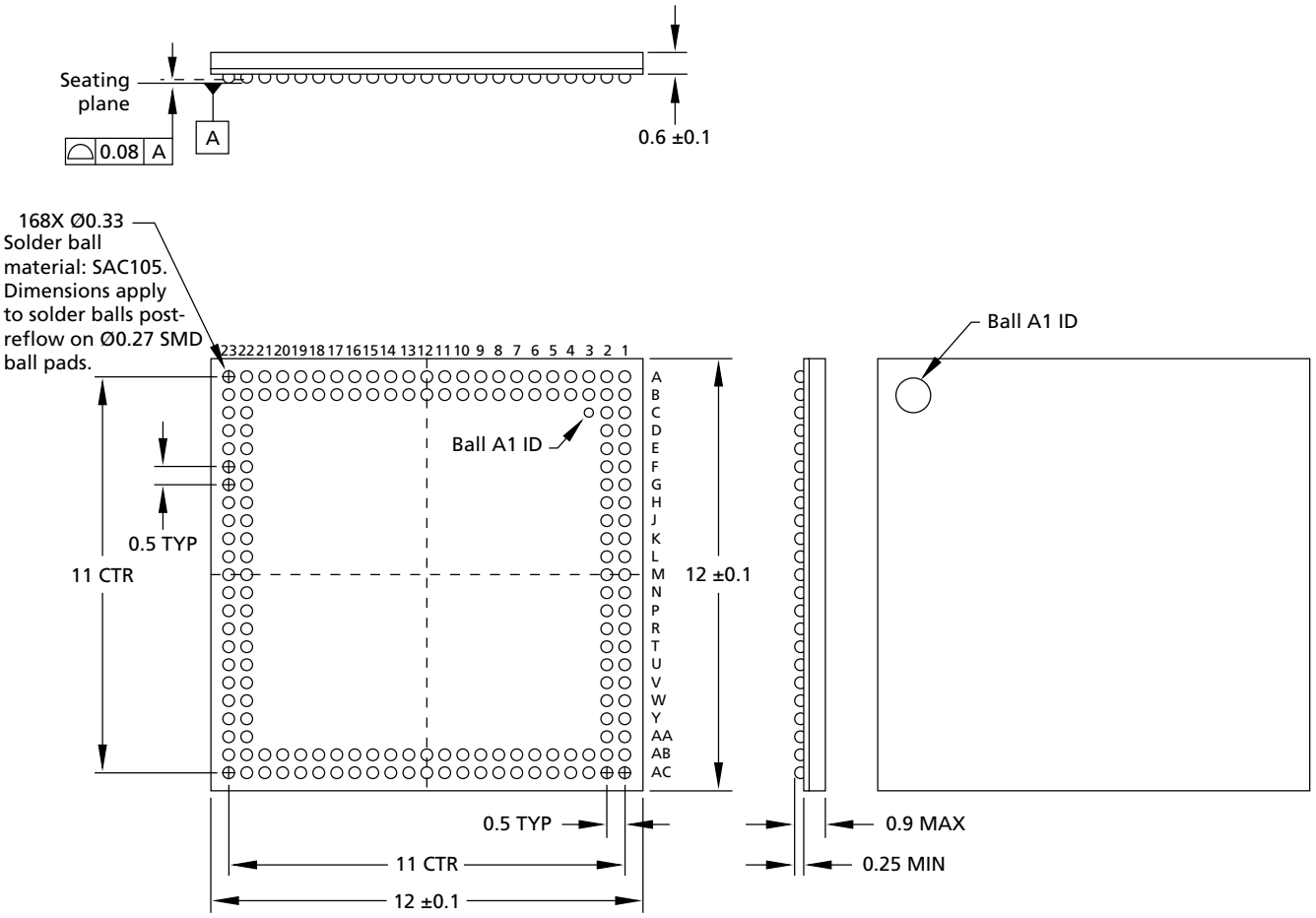


Figure 6: 168-Ball (Dual LPDDR) Functional Block Diagram



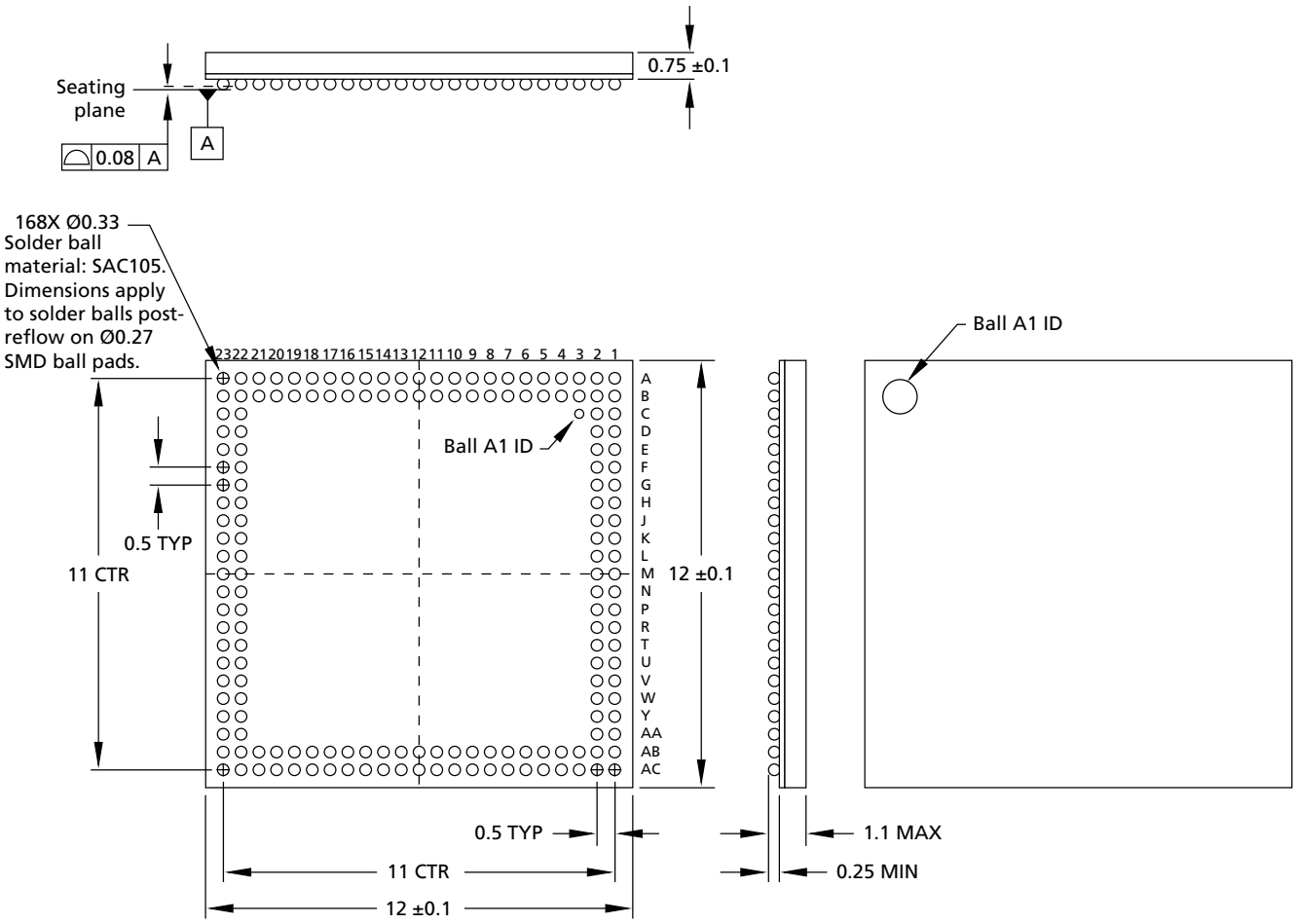
Package Dimensions

Figure 7: 168-Ball VFBGA (Package Code: JG)



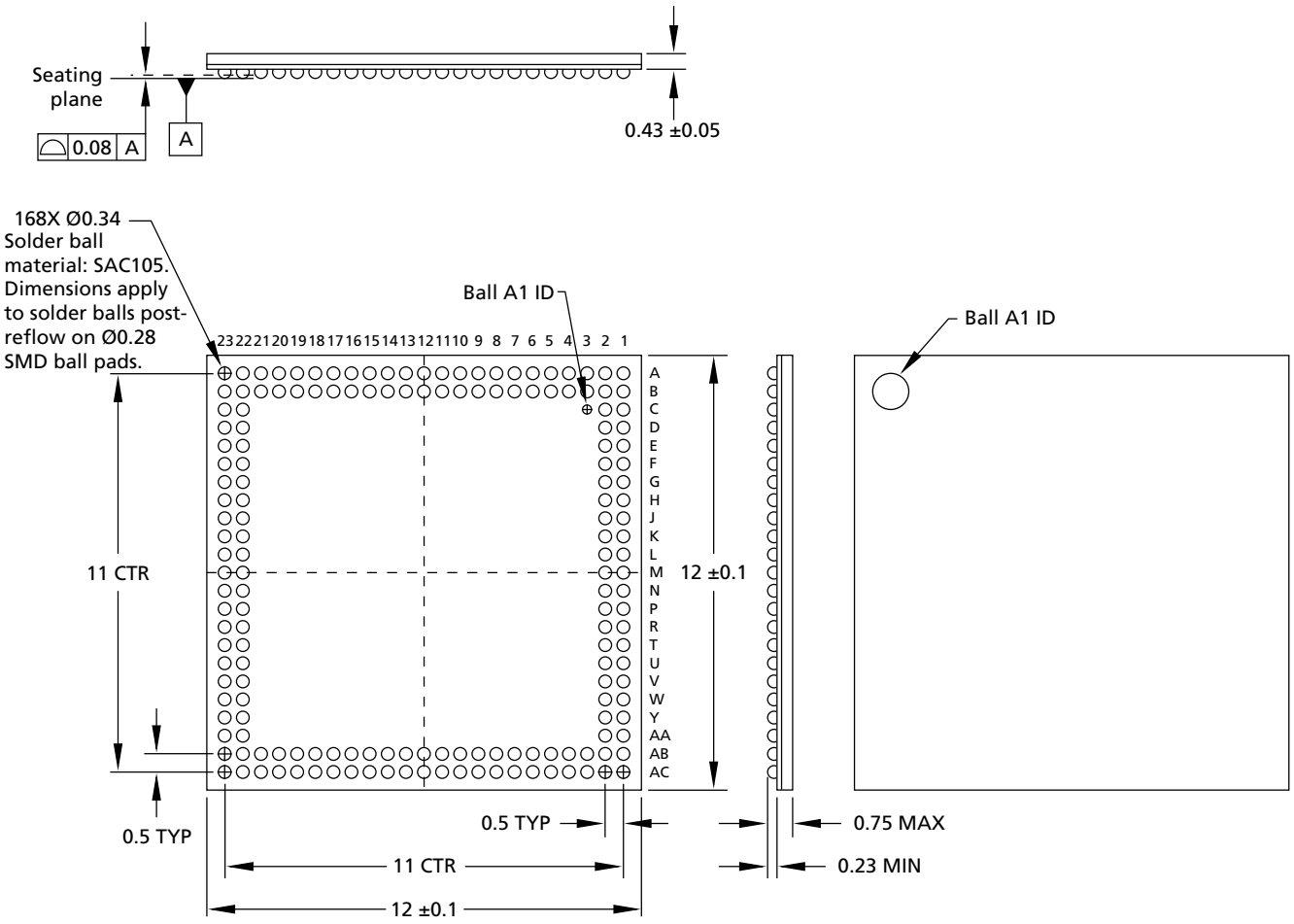
Note: 1. All dimensions are in millimeters.

Figure 8: 168-Ball VFBGA (Package Code: JI)



Note: 1. All dimensions are in millimeters.

Figure 9: 168-Ball WFBGA (Package Code: KQ)



Note: 1. All dimensions are in millimeters.

Revision History

Rev. I, Preliminary – 6/09

- Updated Figure 2 (page 2) for NAND Flash Configuration codes by adding "y" information: y (x8, 4Gb, Second) and z (x16, 4Gb, second).
- Changed ball Y22 from NC to A14 in Figure 4 (page 6).
- Changed A[13:0] to A[14:0] in Table 3 (page 8).

Rev. H, Preliminary – 5/09

- Deleted "Device size" bullets from NAND-Flash-Specific Features on the page 1.
- Added 200 MHz CL3 (-5) to Options/Marking table on page 1.
- Updated Figure 2 (page 2) to list "-5 = 200 MHz CL3" under "LPDRAM Access Time." Udated the Package Codes to show the preferred format. Added "CS#" after "CE#" in the Chip Count. Changed row B under Chip Count to "1, 1" and row D to "1, 2." Added "AM" and "AP" under "LPDRAM Configuration." Added "KQ" under "Package Codes." Deleted "L = Low-Power Option."
- Modified Figure 5 (page 11) to change "CS#" to "CSO#," "CKE" to "CKE0," and "CE#" to "CE0#."
- Modified Figure 6 (page 12) to change "CE#" to "CE0#."
- Added new Figure 9 (page 15).

Rev. G, Preliminary – 3/09

- Added MT29C4G48MAPLCJG-6 IT to part number table.

Rev. F, Preliminary – 11/08

- Updated template for external publication

Rev. E, Preliminary – 09/08

- “MT29CxGxxMAxxxJG, MT29CxGxxMAxxxJI”: As the third-from-the-last character in the part number, replaced “A” with an “x.”
- Figure 3, Ball Assignment: 168-Ball VFBGA (x8 NAND Flash and x16 LPDRAM): Updated figure by replacing “NC”s in lower-left corner with “RFU”s.
- Table 2, “NAND Flash Ball Descriptions,” In CE1#/CE0# row, reversed order of ball numbers to reflect correct highest-to-lowest order; changed “NC” to “RFU1” in the I/O row; added note 1.
- Table 3, “LPDDR Ball Descriptions,”: In BA1/BA0, CKE1/CKE0, and CS1#/CS0# rows, reversed order of ball numbers to reflect correct highest-to-lowest order; in NC row, removed AE-indicated ball assignments and created a new RFU row.
- Figure 6, 168-Ball Dual LPDDR Functional Block Diagram: Added figure adapted from 152-ball.
- Figure 7, 168-Ball VFBGA (Package Code: JG): Updated figure with current version from MDM.
- Figure 8, 168-Ball VFBGA (Package Code: JI): Updated figure with current version from MDM.

Rev. D, Preliminary – 04/08

- Changed status to preliminary.
- Figure 2: 168-Ball Part Number Chart on page 2: Added JI part number and package code.
- Figure 3: Ball Assignment: 168-Ball VFBGA (x8 NAND Flash and x16 LPDRAM); Figure 4: 168-Ball VFBGA (NAND x16; LPDDR x32) Ball Assignments; Table 2, “NAND Flash Ball Descriptions,”; Table 3, “LPDDR Ball Descriptions,”; and Table 4, “Non-Device-Specific Ball Descriptions,”: Updated ball assignments.
- Removed former capacitance tables. See component data sheets for capacitance.
- Figure 8: 168-Ball VFBGA (Package Code: JI): Added figure.

Rev. C, Advance – 02/08

- Figure 2: 168-Ball Part Number Chart: Updated self-refresh current definition.
- Figure 7: 168-Ball VFBGA (Package Code: JG): Updated package diagram with 0.15 tolerance.

Rev. B – 12/07

- “LP-DRAM-Specific Features”: Added SRR feature.
- Separated original single ball-assignment table into separate tables: Table 2, “NAND Flash Ball Descriptions,” Table 3, “LPDDR Ball Descriptions,” and Table 4, “Non-Device-Specific Ball Descriptions.”
- Figure 3, 137-Ball TFBGA (LPDDR) Ball Assignments, on page 4: changed pin P1 from NC to RFU.
- Removed “Mobile” from LP-DRAM references.

Rev. A – 12/07

- Initial release.

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This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.