National Semiconductor

November 9, 2009

DS91M124

125 MHz 1:4 M-LVDS Repeater with LVCMOS Input

General Description

The DS91M124 is a 1:4 M-LVDS repeater for driving and distributing clock or data signals to up to four multipoint networks.

M-LVDS (Multipoint LVDS) is a new family of bus interface devices based on LVDS technology specifically designed for multipoint and multidrop cable and backplane applications. It differs from standard LVDS in providing increased drive current to handle double terminations that are required in multipoint applications. Controlled transition times minimize reflections that are common in multipoint configurations due to unterminated stubs.

A single DS91M124 channel is a 1:4 repeater that accepts LVTTL/LVCMOS signals at the driver inputs and converts them to differential M-LVDS signal levels. It features independent driver enable pins for each driver output.

The DS91M124 has a flow-through pinout for easy PCB layout. It provides a new alternative for high speed multipoint interface applications. It is packaged in a space saving SOIC-16 package.

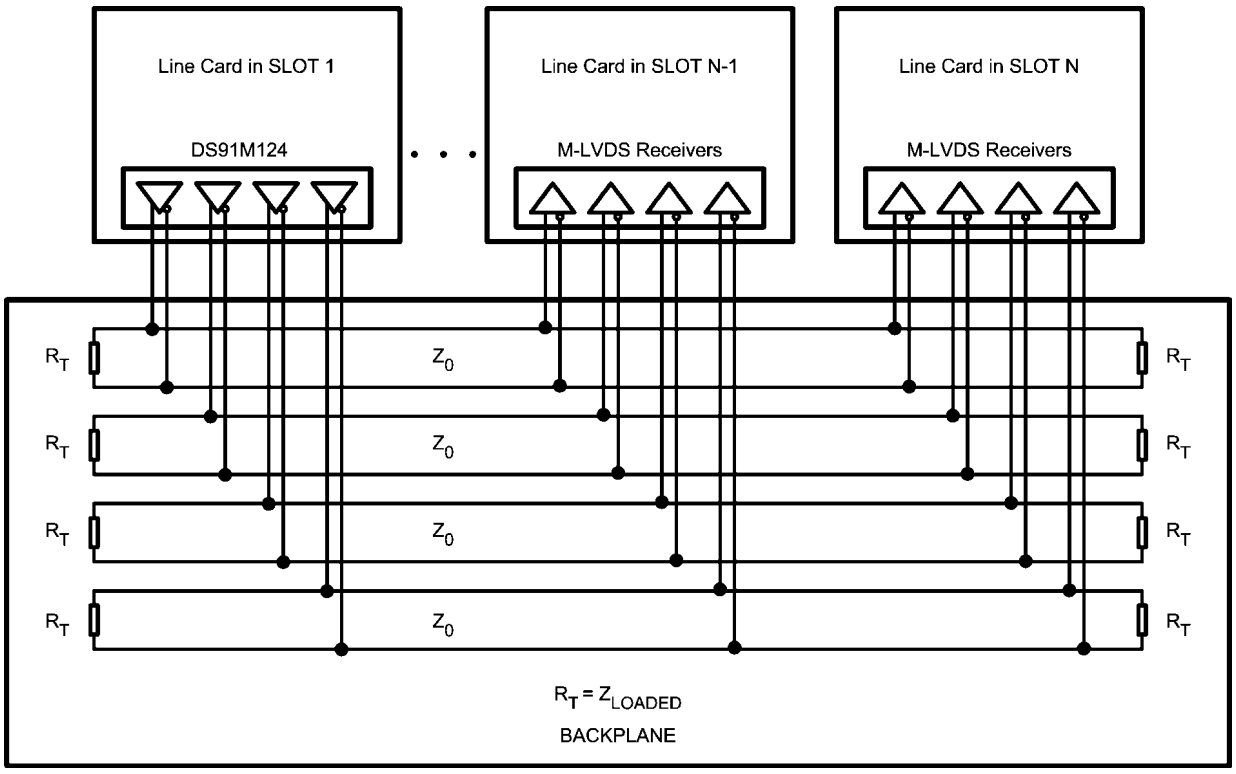
Features

- DC - 125 MHz / 250 Mbps low jitter, low skew, low power operation
- Independent Driver Enable pins
- Conforms to TIA/EIA-899 M-LVDS Standard
- Controlled transition times minimize reflections
- 8 kV ESD on M-LVDS I/O pins protects adjoining components
- Flow-through pinout simplifies PCB layout
- Industrial operating temperature range (–40°C to +85°C)
- Available in a space saving SOIC-16 package

Applications

- Multidrop / Multipoint clock and data distribution
- High-Speed, Low Power, Short-Reach alternative to TIA/EIA-485/422
- Clock distribution in AdvancedTCA (ATCA) and MicroTCA (µTCA) backplanes

Typical Application



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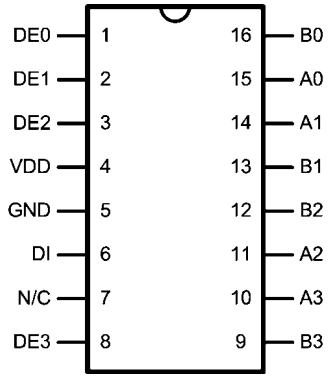
Ordering Information

Order Number	Function	Package Type
DS91M124TMA	1:4 Repeater	SOIC-16

Pin Diagram



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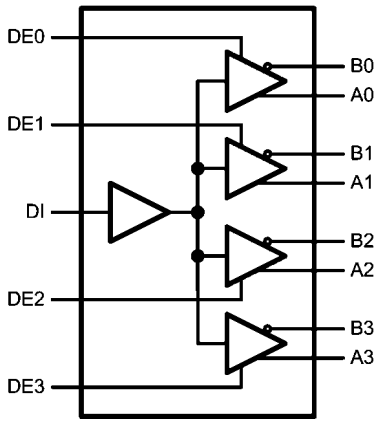
Logic Diagram



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Pin Descriptions

Number	Name	I/O, Type	Description
1, 2, 3, 8	DE	I, LVCMOS	Driver enable pin: When a DE pin is low, the corresponding driver output is disabled. When a DE pin is high, the corresponding driver output is enabled. There is a 300 kΩ pulldown resistor on each DE pin.
6	DI	I, LVCMOS	Driver input pin.
5	GND	Power	Ground pin.
10, 11, 14, 15	A	O, M-LVDS	Non-inverting driver output pins.
9, 12, 13, 16	B	O, M-LVDS	Inverting driver output pins.
4	V_{DD}	Power	Power supply pin, +3.3V ± 0.3V
7	N/C	N/A	NO CONNECT pin.

Absolute Maximum Ratings (*Note 4*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Supply Voltage	−0.3V to +4V
LVCMOS Input Voltage	−0.3V to (V_{DD} + 0.3V)
M-LVDS Output Voltage	−1.9V to +5.5V
M-LVDS Output Short Circuit Current Duration	Continuous
Junction Temperature	+140°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range	
Soldering (4 sec.)	+260°C
Maximum Package Power Dissipation @ +25°C	
MA Package	2.21W
Derate MA Package	19.2 mW/°C above +25°C
Package Thermal Resistance (4-Layer, 2 oz. Cu, JEDEC)	
θ_{JA}	+52°C/W
θ_{JC}	+19°C/W

ESD Susceptibility	
HBM (*Note 1*)	≥8 kV
MM (*Note 2*)	≥250V
CDM (*Note 3*)	≥1250V

Note 1: Human Body Model, applicable std. JESD22-A114C

Note 2: Machine Model, applicable std. JESD22-A115-A

Note 3: Field Induced Charge Device Model, applicable std. JESD22-C101-C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage, V_{DD}	3.0	3.3	3.6	V
Voltage at Any Bus Terminal (Separate or Common-Mode)	−1.4		+3.8	V
LVTTL Input Voltage High V_{IH}	2.0		V_{DD}	V
LVTTL Input Voltage Low V_{IL}	0		0.8	V
Operating Free Air Temperature T_A	−40	+25	+85	°C

DC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified. (*Note 5*, *Note 6*, *Note 7*, *Note 10*)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVCMOS DC Specifications						
V_{IH}	High-Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low-Level Input Voltage		GND		0.8	V
I_{IH}	High-Level Input Current	V_{IH} = 3.6V	-15	±1	15	µA
I_{IL}	Low-Level Input Current	V_{IL} = 0V	-15	±1	15	µA
V_{CL}	Input Clamp Voltage	I_{IN} = -18 mA	-1.5			V
M-LVDS DC Specifications						
$\|V_{AB}\|$	Differential Output Voltage Magnitude	R_L = 50Ω, C_L = 5 pF Figures 1, 3	480		650	mV
ΔV_{AB}	Change in Differential Output Voltage Magnitude Between Logic States		−50		50	mV
$V_{OS(SS)}$	Steady-State Common-Mode Output Voltage	Figures 1, 2 R_L = 50Ω	0.30	1.6	2.10	V
$\|\Delta V_{OS(SS)}\|$	Change in Steady-State Common-Mode Output Voltage Between Logic States		0		50	mV
$V_{A(OC)}$	Maximum Steady-State Open-Circuit Output Voltage	*Figure 4*	0		2.4	V
$V_{B(OC)}$	Maximum Steady-State Open-Circuit Output Voltage		0		2.4	V
$V_{P(H)}$	Voltage Overshoot, Low-to-High Level Output (*Note 8*)	R_L = 50Ω, C_L = 5 pF C_D = 0.5 pF Figures 6, 7			$1.2V_{SS}$	V
$V_{P(L)}$	Voltage Overshoot, High-to-Low Level Output (*Note 8*)		$-0.2V_{SS}$			V
I_{OS}	Output Short-Circuit Current (*Note 9*)	*Figure 5*	-43		43	mA
I_A	Driver High-Impedance Output Current	V_A = 3.8V, V_B = 1.2V	0		32	µA
		V_A = 0V or 2.4V, V_B = 1.2V	−20		20	µA
		V_A = −1.4V, V_B = 1.2V	−32		0	µA
I_B	Driver High-Impedance Output Current	V_A = 3.8V, V_B = 1.2V	0		32	µA
		V_A = 0V or 2.4V, V_B = 1.2V	−20		20	µA
		V_A = −1.4V, V_B = 1.2V	−32		0	µA
I_{AB}	Driver High-Impedance Output Differential Curent (I_A − I_B)	V_A = V_B, −1.4V ≤ V ≤ 3.8V	−4		4	µA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{A(OFF)}$	Driver High-Impedance Output Power-Off Current	V_A = 3.8V, V_B = 1.2V DE_n = 0V 0V ≤ V_{DD} ≤ 1.5V	0		32	µA
		V_A = 0V or 2.4V, V_B = 1.2V DE_n = 0V 0V ≤ V_{DD} ≤ 1.5V	−20		20	µA
		V_A = −1.4V, V_B = 1.2V DE_n = 0V 0V ≤ V_{DD} ≤ 1.5V	−32		0	µA
$I_{B(OFF)}$	Driver High-Impedance Output Power-Off Current	V_A = 3.8V, V_B = 1.2V DE_n = 0V 0V ≤ V_{DD} ≤ 1.5V	0		32	µA
		V_A = 0V or 2.4V, V_B = 1.2V DE_n = 0V 0V ≤ V_{DD} ≤ 1.5V	−20		20	µA
		V_A = −1.4V, V_B = 1.2V DE_n = 0V 0V ≤ V_{DD} ≤ 1.5V	−32		0	µA
$I_{AB(OFF)}$	Driver High-Impedance Output Power-Off Current ($I_{A(OFF)}$ − $I_{B(OFF)}$)	V_A = V_B, −1.4V ≤ V ≤ 3.8V DE_n = 0V 0V ≤ V_{DD} ≤ 1.5V	−4		4	µA
C_A	Driver Output Capacitance	V_{DD} = 0V		7.8		pF
C_B	Driver Output Capacitance			7.8		pF
C_{AB}	Driver Output Differential Capacitance			3		pF
$C_{A/B}$	Driver Output Capacitance Balance (C_A/C_B)			1		
I_{CCL}	Loaded Supply Current Enabled	R_L = 50Ω (All Outputs) DI = V_{DD} or GND DE_n = V_{DD} or GND (All Outputs)		65	75	mA
I_{CCZ}	No Load Supply Current Disabled	DI = V_{DD} or GND, DE_n = GND (All Outputs)		19	24	mA

Note 4: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

Note 5: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 6: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD}.

Note 7: Typical values represent most likely parametric norms for V_{DD} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 8: Specification is guaranteed by characterization and is not tested in production.

Note 9: Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

Note 10: C_L includes fixture capacitance and C_D includes probe capacitance.

Switching Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified. (*Note 11*, *Note 12*, *Note 18*)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Differential Propagation Delay High to Low	R_L = 50Ω C_L = 5 pF, C_D = 0.5 pF Figures 6, 7	1.8	3.9	6.5	ns
t_{PLH}	Differential Propagation Delay Low to High		1.8	3.9	6.5	ns
t_{SKD1}	Differential Pulse Skew $\lvert t_{PHL} - t_{PLH} \rvert$ (*Note 13*, *Note 14*)		0	25	100	ps
t_{SKD2}	Channel-to-Channel Skew (*Note 13*, *Note 15*)		0	70	250	ps
t_{SKD3}	Differential Part-to-Part Skew (*Note 13*, *Note 16*) (Constant T_A and VDD)		0	1.5	2	ns
t_{SKD4}	Differential Part-to-Part Skew (*Note 13*, *Note 17*)		0		4.7	ns
t_{TLH}	Rise Time (*Note 13*)		1.1	2.0	3.0	ns
t_{THL}	Fall Time (*Note 13*)		1.1	2.0	3.0	ns
t_{PHZ}	Disable Time High to Z	R_L = 50Ω C_L = 5 pF, C_D = 0.5 pF Figures 8, 9		6	11	ns
t_{PLZ}	Disable Time Low to Z			6	11	ns
t_{PZH}	Enable Time Z to High			6	11	ns
t_{PZL}	Enable Time Z to Low			6	11	ns
f_{MAX}	Maximum Operating Frequency (*Note 13*)		125			MHz

Note 11: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 12: Typical values represent most likely parametric norms for V_{DD} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 13: Specification is guaranteed by characterization and is not tested in production.

Note 14: t_{SKD1}, $\lvert t_{PLHD} - t_{PHLD} \rvert$, Pulse Skew, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

Note 15: t_{SKD2}, Channel-to-Channel Skew, is the difference in propagation delay (t_{PLHD} or t_{PHLD}) among all output channels.

Note 16: t_{SKD3}, Part-to-Part Skew, is defined as the difference between the minimum and maximum differential propagation delays. This specification applies to devices at the same V_{DD} and within 5°C of each other within the operating temperature range.

Note 17: t_{SKD4}, Part-to-Part Skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max – Min| differential propagation delay.

Note 18: C_L includes fixture capacitance and C_D includes probe capacitance.

Test Circuits and Waveforms

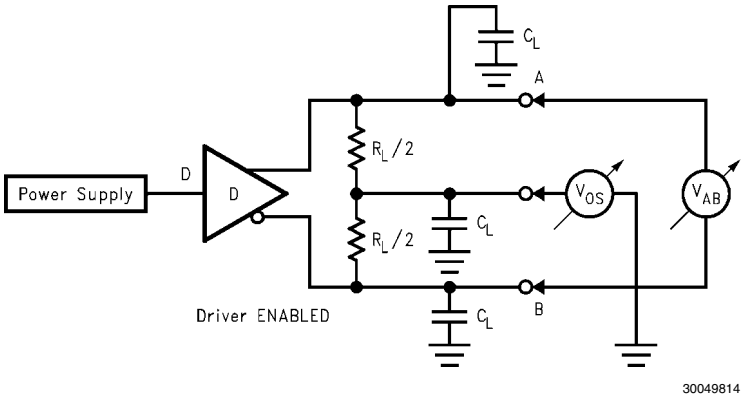


FIGURE 1. Differential Driver Test Circuit

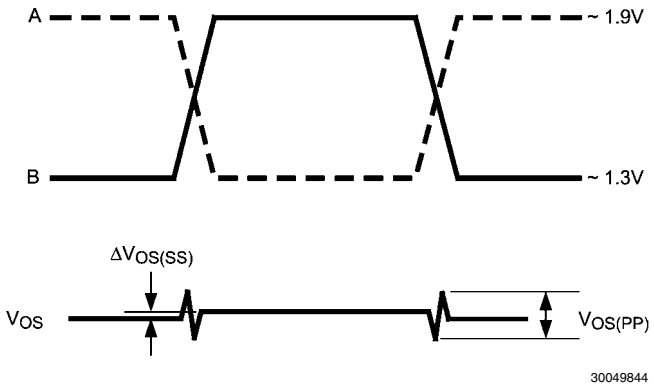


FIGURE 2. Differential Driver Waveforms

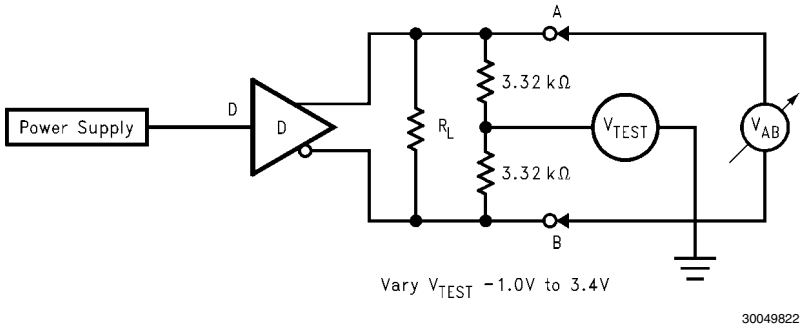


FIGURE 3. Differential Driver Full Load Test Circuit

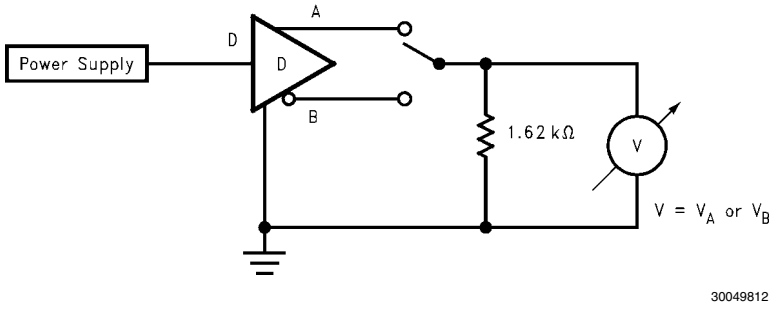


FIGURE 4. Differential Driver DC Open Test Circuit

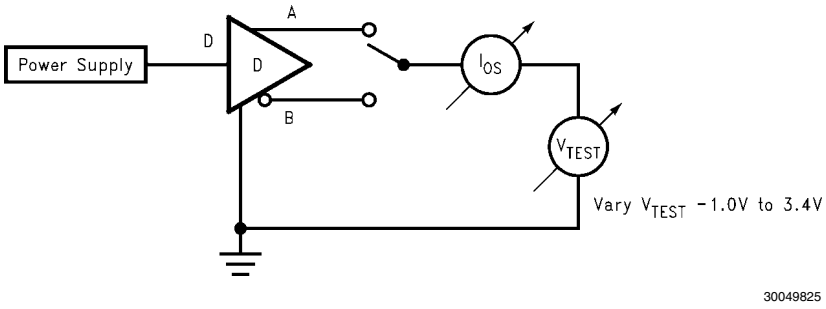


FIGURE 5. Differential Driver Short-Circuit Test Circuit

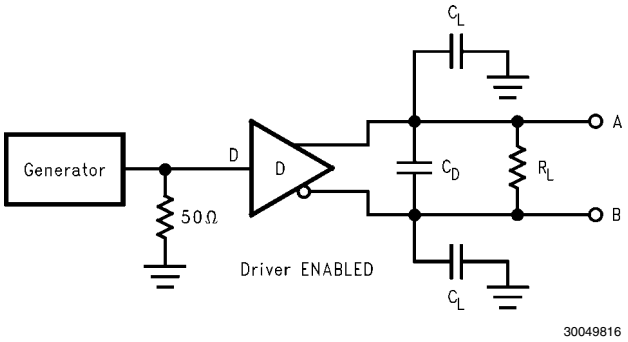


FIGURE 6. Driver Propagation Delay and Transition Time Test Circuit

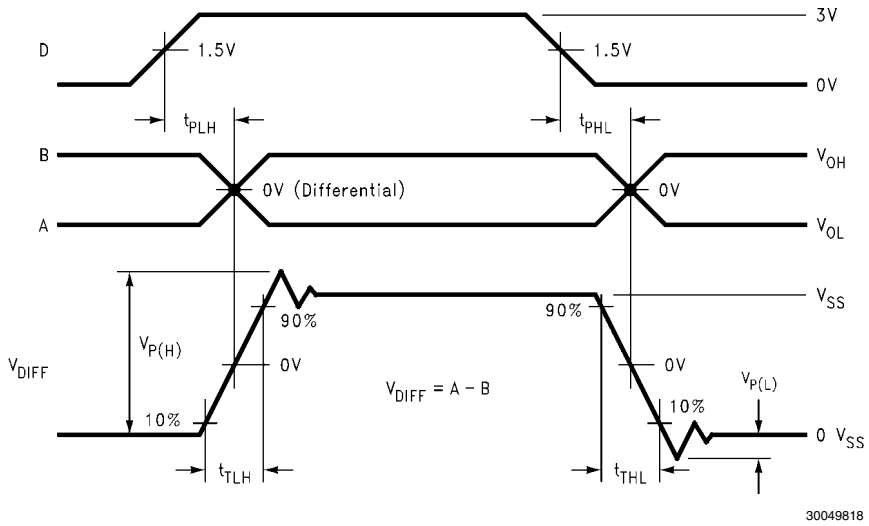


FIGURE 7. Driver Propagation Delays and Transition Time Waveforms

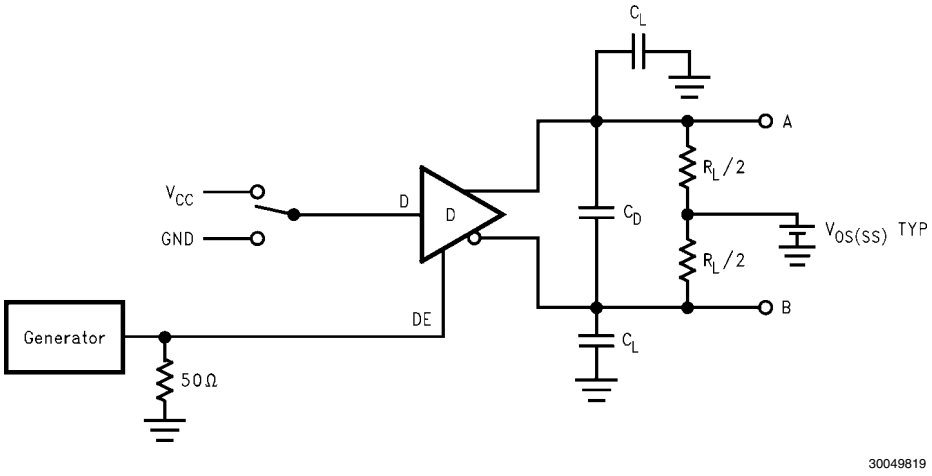


FIGURE 8. Driver TRI-STATE Delay Test Circuit

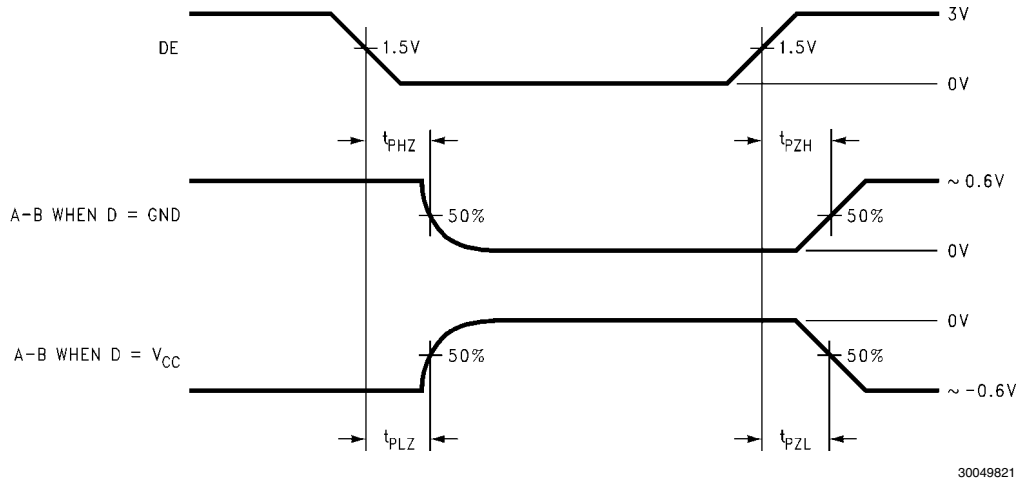
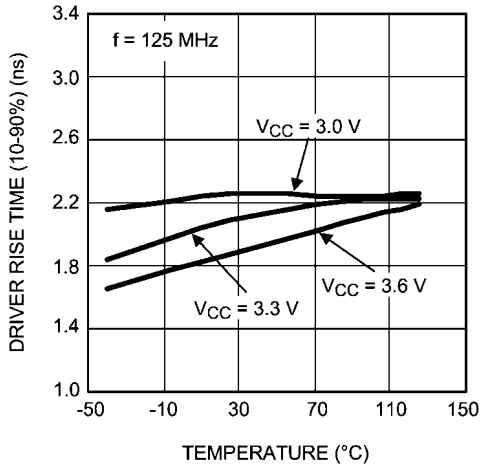


FIGURE 9. Driver TRI-STATE Delay Waveforms

Typical Performance Characteristics



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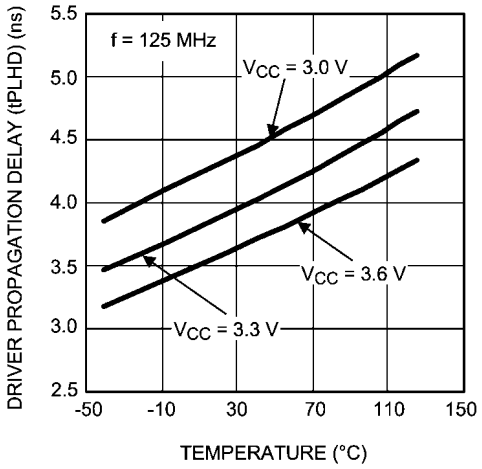
Driver Rise Time as a Function of Temperature



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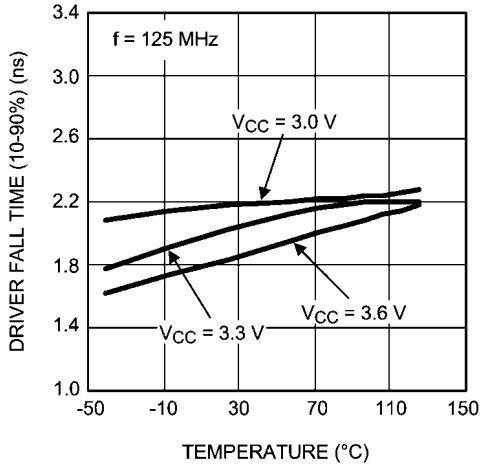
Driver Propagation Delay (tPLHD) as a Function of Temperature



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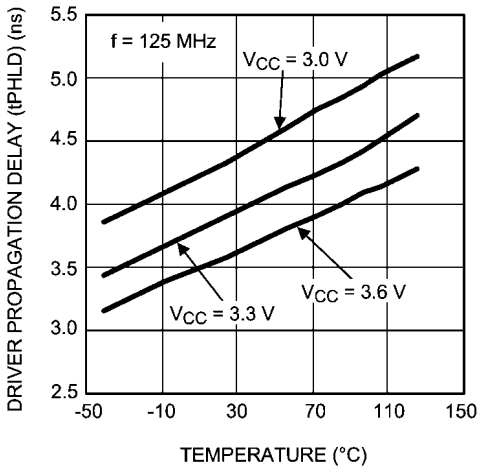
Driver Fall Time as a Function of Temperature



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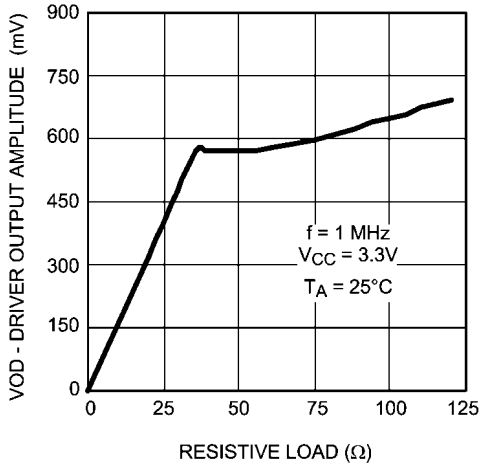
Driver Propagation Delay (tPHLD) as a Function of Temperature



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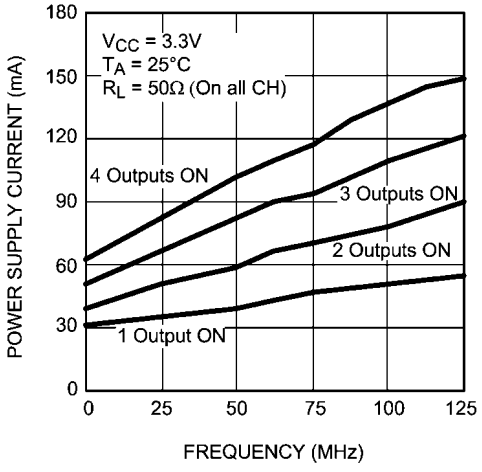
Driver Output Signal Amplitude as a Function of Resistive Load



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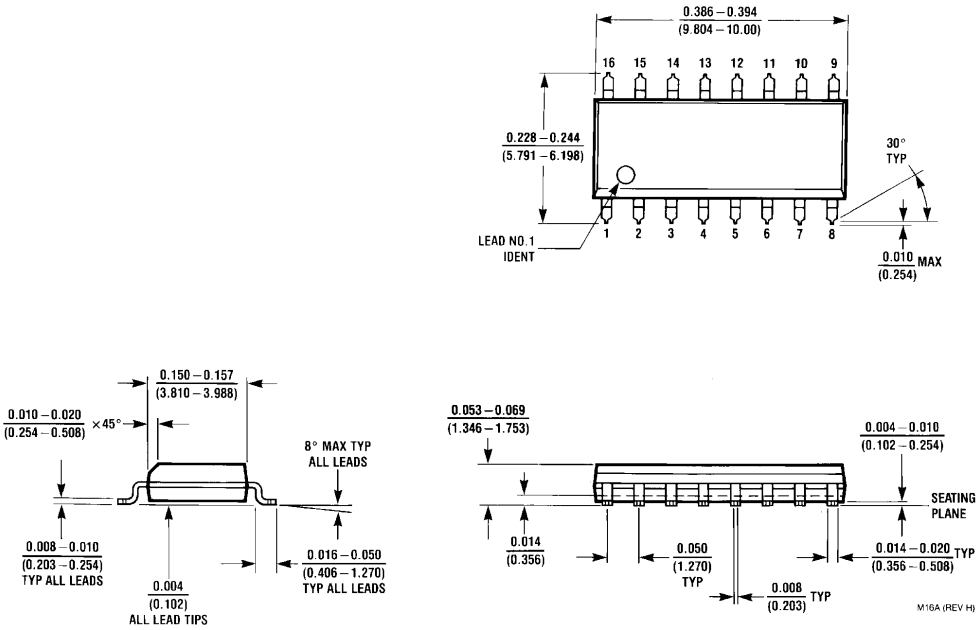
Driver Power Supply Current as a Function of Frequency

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead (0.150″ Wide) Molded Small Outline Package, JEDEC
Order Number DS91M124TMA
NS Package Number M16A

Notes

Notes

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LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy
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