

Single-Channel: 6N137, HCPL2601, HCPL2611 Dual-Channel: HCPL2630, HCPL2631 High Speed 10MBit/s Logic Gate Optocouplers

Features

- Very high speed – 10 MBit/s
- Superior CMR – 10 kV/μs
- Double working voltage-480V
- Fan-out of 8 over -40°C to +85°C
- Logic gate output
- Strobable output
- Wired OR-open collector
- U.L. recognized (File # E90700)

Applications

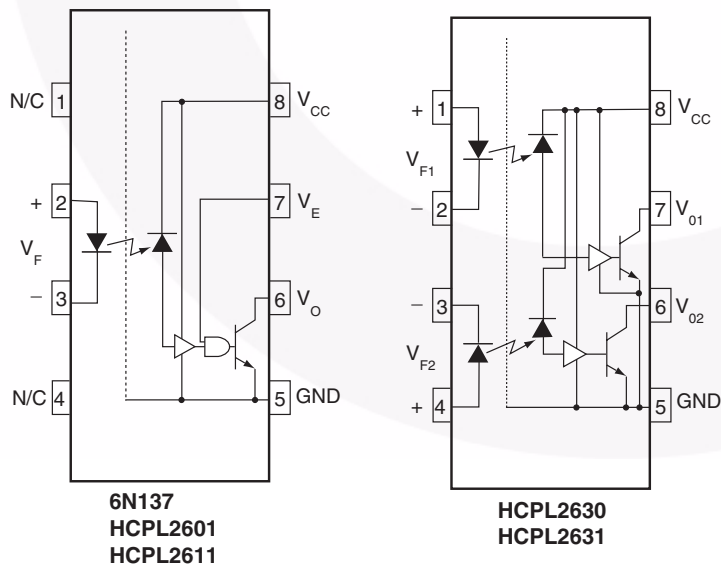
- Ground loop elimination
- LSTTL to TTL, LSTTL or 5-volt CMOS
- Line receiver, data transmission
- Data multiplexing
- Switching power supplies
- Pulse transformer replacement
- Computer-peripheral interface

Description

The 6N137, HCPL2601, HCPL2611 single-channel and HCPL2630, HCPL2631 dual-channel optocouplers consist of a 850 nm AlGaAs LED, optically coupled to a very high speed integrated photo-detector logic gate with a strobable output. This output features an open collector, thereby permitting wired OR outputs. The coupled parameters are guaranteed over the temperature range of -40°C to +85°C. A maximum input signal of 5mA will provide a minimum output sink current of 13mA (fan out of 8).

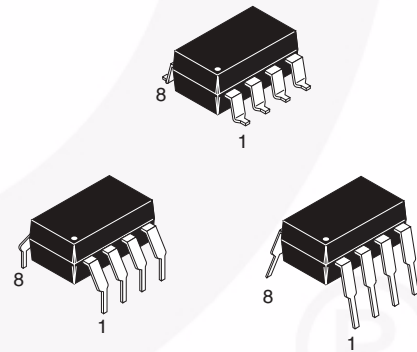
An internal noise shield provides superior common mode rejection of typically 10kV/μs. The HCPL2601 and HCPL2631 has a minimum CMR of 5kV/μs. The HCPL2611 has a minimum CMR of 10kV/μs.

Schematics



A 0.1μF bypass capacitor must be connected between pins 8 and 5⁽¹⁾.

Package Outlines



Truth Table (Positive Logic)

| Input | Enable | Output |
|-------|--------|--------|
| H | H | L |
| L | H | H |
| H | L | H |
| L | L | H |
| H | NC | L |
| L | NC | H |

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | | Value | Units |
|----------------------------|--|-----------------------------|----------------|------------------|
| T_{STG} | Storage Temperature | | -55 to +125 | $^\circ\text{C}$ |
| T_{OPR} | Operating Temperature | | -40 to +85 | $^\circ\text{C}$ |
| T_{SOL} | Lead Solder Temperature (for wave soldering only)* | | 260 for 10 sec | $^\circ\text{C}$ |
| EMITTER | | | | |
| I_F | DC/Average Forward | Single Channel | 50 | mA |
| | Input Current | Dual Channel (Each Channel) | 30 | |
| V_E | Enable Input Voltage Not to Exceed V_{CC} by more than 500mV | Single Channel | 5.5 | V |
| V_R | Reverse Input Voltage | Each Channel | 5.0 | V |
| P_I | Power Dissipation | Single Channel | 100 | mW |
| | | Dual Channel (Each Channel) | 45 | |
| DETECTOR | | | | |
| V_{CC} (1 minute max) | Supply Voltage | | 7.0 | V |
| I_O | Output Current | Single Channel | 50 | mA |
| | | Dual Channel (Each Channel) | 50 | |
| V_O | Output Voltage | Each Channel | 7.0 | V |
| P_O | Collector Output | Single Channel | 85 | mW |
| | Power Dissipation | Dual Channel (Each Channel) | 60 | |

*For peak soldering reflow, please refer to the Reflow Profile on page 11.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Min. | Max. | Units |
|----------|----------------------------|------|----------|------------------|
| I_{FL} | Input Current, Low Level | 0 | 250 | μA |
| I_{FH} | Input Current, High Level | *6.3 | 15 | mA |
| V_{CC} | Supply Voltage, Output | 4.5 | 5.5 | V |
| V_{EL} | Enable Voltage, Low Level | 0 | 0.8 | V |
| V_{EH} | Enable Voltage, High Level | 2.0 | V_{CC} | V |
| T_A | Low Level Supply Current | -40 | +85 | $^\circ\text{C}$ |
| N | Fan Out (TTL load) | | 8 | |

*6.3mA is a guard banded value which allows for at least 20% CTR degradation. Initial input current threshold value is 5.0mA or less.

Electrical Characteristics ($T_A = 0$ to 70°C unless otherwise specified)**Individual Component Characteristics**

| Symbol | Parameter | Test Conditions | Min. | Typ.* | Max. | Unit | |
|---------------------------|-------------------------------------|---|----------------|---|------|----------------------|----|
| EMITTER | | | | | | | |
| V_F | Input Forward Voltage | $I_F = 10\text{mA}$ $T_A = 25^\circ\text{C}$ | | | 1.8 | V | |
| | | | | 1.4 | 1.75 | | |
| B_{VR} | Input Reverse Breakdown Voltage | $I_R = 10\mu\text{A}$ | 5.0 | | | V | |
| C_{IN} | Input Capacitance | $V_F = 0, f = 1\text{MHz}$ | | 60 | | pF | |
| $\Delta V_F / \Delta T_A$ | Input Diode Temperature Coefficient | $I_F = 10\text{mA}$ | | -1.4 | | mV/ $^\circ\text{C}$ | |
| DETECTOR | | | | | | | |
| I_{CCH} | High Level Supply Current | $V_{CC} = 5.5\text{V}, I_F = 0\text{mA}, V_E = 0.5\text{V}$ | Single Channel | | 7 | 10 | mA |
| | | | Dual Channel | | 10 | 15 | |
| I_{CCL} | Low Level Supply Current | | Single Channel | $V_{CC} = 5.5\text{V}, I_F = 10\text{mA}$ | 9 | 13 | mA |
| | | | Dual Channel | $V_E = 0.5\text{V}$ | 14 | 21 | |
| I_{EL} | Low Level Enable Current | $V_{CC} = 5.5\text{V}, V_E = 0.5\text{V}$ | | -0.8 | -1.6 | mA | |
| I_{EH} | High Level Enable Current | $V_{CC} = 5.5\text{V}, V_E = 2.0\text{V}$ | | -0.6 | -1.6 | mA | |
| V_{EH} | High Level Enable Voltage | $V_{CC} = 5.5\text{V}, I_F = 10\text{mA}$ | 2.0 | | | V | |
| V_{EL} | Low Level Enable Voltage | $V_{CC} = 5.5\text{V}, I_F = 10\text{mA}^{(3)}$ | | | 0.8 | V | |

Switching Characteristics ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5\text{V}$, $I_F = 7.5\text{mA}$ unless otherwise specified)

| Symbol | AC Characteristics | Test Conditions | Min. | Typ.* | Max. | Unit |
|-----------------------|---|---|--------------------|-------|--------|------------------|
| T_{PLH} | Propagation Delay Time to Output HIGH Level | $R_L = 350\Omega, C_L = 15\text{pF}^{(4)}$ (Fig. 12) $T_A = 25^\circ\text{C}$ | 20 | 45 | 75 | ns |
| | | | | | 100 | |
| T_{PHL} | Propagation Delay Time to Output LOW Level | $T_A = 25^\circ\text{C}^{(5)}$ $R_L = 350\Omega, C_L = 15\text{pF}$ (Fig. 12) | 25 | 45 | 75 | ns |
| | | | | | 100 | |
| $ T_{PHL} - T_{PLH} $ | Pulse Width Distortion | $(R_L = 350\Omega, C_L = 15\text{pF})$ (Fig. 12) | | 3 | 35 | ns |
| t_r | Output Rise Time (10–90%) | $R_L = 350\Omega, C_L = 15\text{pF}^{(6)}$ (Fig. 12) | | 50 | | ns |
| t_f | Output Rise Time (90–10%) | $R_L = 350\Omega, C_L = 15\text{pF}^{(7)}$ (Fig. 12) | | 12 | | ns |
| t_{ELH} | Enable Propagation Delay Time to Output HIGH Level | $I_F = 7.5\text{mA}, V_{EH} = 3.5\text{V}, R_L = 350\Omega, C_L = 15\text{pF}^{(8)}$ (Fig. 13) | | 20 | | ns |
| t_{EHL} | Enable Propagation Delay Time to Output LOW Level | $I_F = 7.5\text{mA}, V_{EH} = 3.5\text{V}, R_L = 350\Omega, C_L = 15\text{pF}^{(9)}$ (Fig. 13) | | 20 | | ns |
| ICM_H | Common Mode Transient Immunity (at Output HIGH Level) | $T_A = 25^\circ\text{C}, IV_{CM} = 50\text{V}$ (Peak), $I_F = 0\text{mA}, V_{OH}$ (Min.) = 2.0V, $R_L = 350\Omega^{(10)}$ (Fig. 14) | 6N137, HCPL2630 | | 10,000 | V/ μs |
| | | | HCPL2601, HCPL2631 | | 5000 | |
| | | $ IV_{CM} = 400\text{V}$ | HCPL2611 | | 10,000 | |
| ICM_L | Common Mode Transient Immunity (at Output LOW Level) | $R_L = 350\Omega, I_F = 7.5\text{mA}, V_{OL}$ (Max.) = 0.8V, $T_A = 25^\circ\text{C}^{(11)}$ (Fig. 14) | 6N137, HCPL2630 | | 10,000 | V/ μs |
| | | | HCPL2601, HCPL2631 | | 5000 | |
| | | $ IV_{CM} = 400\text{V}$ | HCPL2611 | | 10,000 | |

Electrical Characteristics (Continued)**Transfer Characteristics** ($T_A = -40$ to $+85^\circ\text{C}$ unless otherwise specified)

| Symbol | DC Characteristics | Test Conditions | Min. | Typ.* | Max. | Unit |
|----------|---------------------------|--|------|-------|------|---------------|
| I_{OH} | HIGH Level Output Current | $V_{CC} = 5.5\text{V}$, $V_O = 5.5\text{V}$, $I_F = 250\mu\text{A}$, $V_E = 2.0\text{V}^{(2)}$ | | | 100 | μA |
| V_{OL} | LOW Level Output Current | $V_{CC} = 5.5\text{V}$, $I_F = 5\text{mA}$, $V_E = 2.0\text{V}$, $I_{CL} = 13\text{mA}^{(2)}$ | | .35 | 0.6 | V |
| I_{FT} | Input Threshold Current | $V_{CC} = 5.5\text{V}$, $V_O = 0.6\text{V}$, $V_E = 2.0\text{V}$, $I_{OL} = 13\text{mA}$ | | 3 | 5 | mA |

Isolation Characteristics ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ unless otherwise specified.)

| Symbol | Characteristics | Test Conditions | Min. | Typ.* | Max. | Unit |
|-----------|---|---|------|-----------|------|---------------|
| I_{I-O} | Input-Output Insulation Leakage Current | Relative humidity = 45%, $T_A = 25^\circ\text{C}$, $t = 5\text{s}$, $V_{I-O} = 3000\text{VDC}^{(12)}$ | | | 1.0* | μA |
| V_{ISO} | Withstand Insulation Test Voltage | $RH < 50\%$, $T_A = 25^\circ\text{C}$, $I_{I-O} \leq 2\mu\text{A}$, $t = 1\text{min.}^{(12)}$ | 2500 | | | V_{RMS} |
| R_{I-O} | Resistance (Input to Output) | $V_{I-O} = 500\text{V}^{(12)}$ | | 10^{12} | | Ω |
| C_{I-O} | Capacitance (Input to Output) | $f = 1\text{MHz}^{(12)}$ | | 0.6 | | pF |

*All Typicals at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$

Notes:

- The V_{CC} supply to each optoisolator must be bypassed by a $0.1\mu\text{F}$ capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package V_{CC} and GND pins of each device.
- Each channel.
- Enable Input – No pull up resistor required as the device has an internal pull up resistor.
- t_{PLH} – Propagation delay is measured from the 3.75mA level on the HIGH to LOW transition of the input current pulse to the 1.5V level on the LOW to HIGH transition of the output voltage pulse.
- t_{PHL} – Propagation delay is measured from the 3.75mA level on the LOW to HIGH transition of the input current pulse to the 1.5V level on the HIGH to LOW transition of the output voltage pulse.
- t_r – Rise time is measured from the 90% to the 10% levels on the LOW to HIGH transition of the output pulse.
- t_f – Fall time is measured from the 10% to the 90% levels on the HIGH to LOW transition of the output pulse.
- t_{ELH} – Enable input propagation delay is measured from the 1.5V level on the HIGH to LOW transition of the input voltage pulse to the 1.5V level on the LOW to HIGH transition of the output voltage pulse.
- t_{EHL} – Enable input propagation delay is measured from the 1.5V level on the LOW to HIGH transition of the input voltage pulse to the 1.5V level on the HIGH to LOW transition of the output voltage pulse.
- CM_H – The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the HIGH state (i.e., $V_{OUT} > 2.0\text{V}$). Measured in volts per microsecond ($\text{V}/\mu\text{s}$).
- CM_L – The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the LOW output state (i.e., $V_{OUT} < 0.8\text{V}$). Measured in volts per microsecond ($\text{V}/\mu\text{s}$).
- Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together, and Pins 5, 6, 7 and 8 shorted together.

Typical Performance Curves

Fig.1 Low Level Output Voltage vs. Ambient Temperature

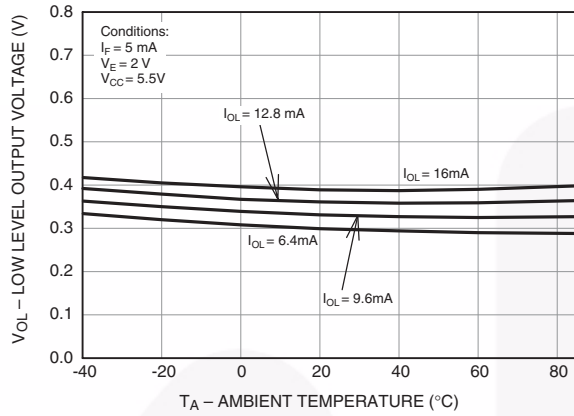


Fig. 2 Input Diode Forward Voltage vs. Forward Current

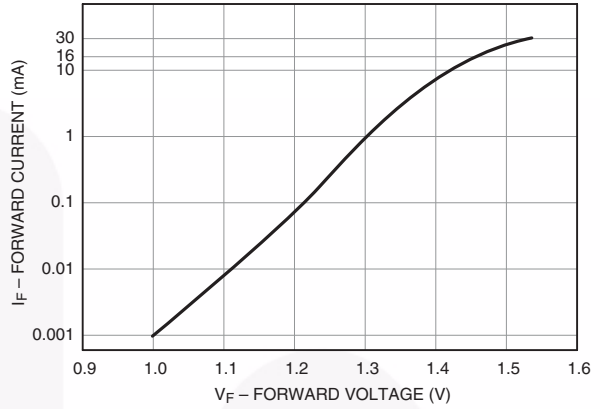


Fig.3 Switching Time vs. Forward Current

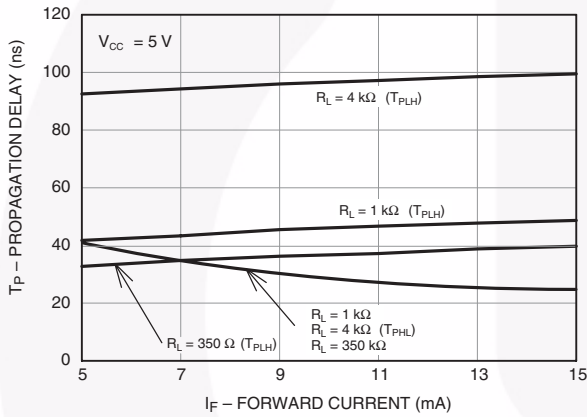


Fig. 4 Low Level Output Current vs. Ambient Temperature

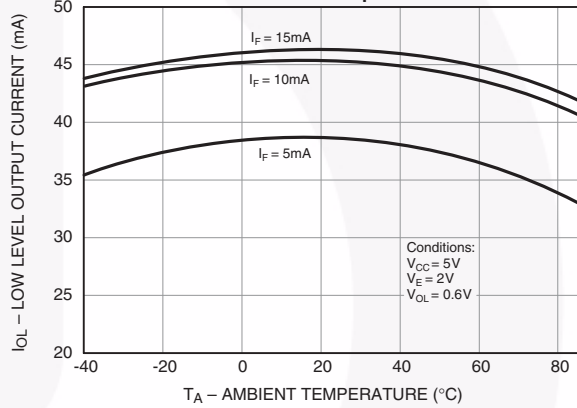


Fig. 5 Input Threshold Current vs. Ambient Temperature

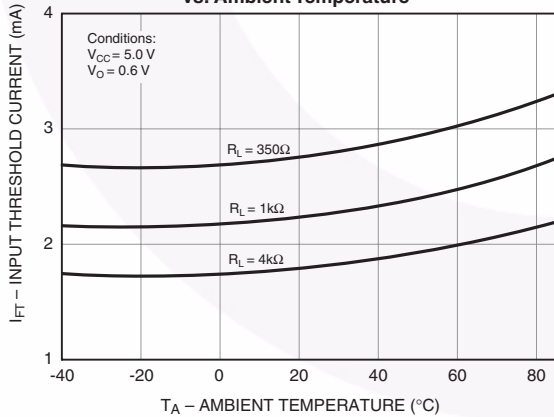
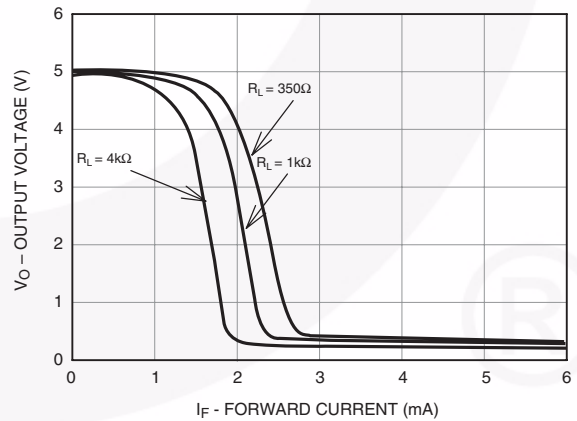


Fig. 6 Output Voltage vs. Input Forward Current



Typical Performance Curves (Continued)

Fig. 7 Pulse Width Distortion vs. Temperature

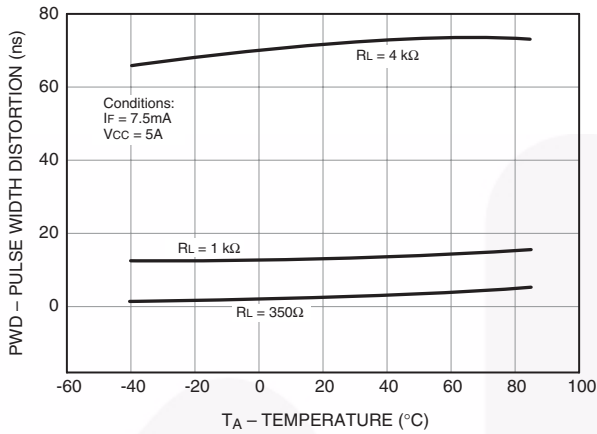


Fig. 8 Rise and Fall Time vs. Temperature

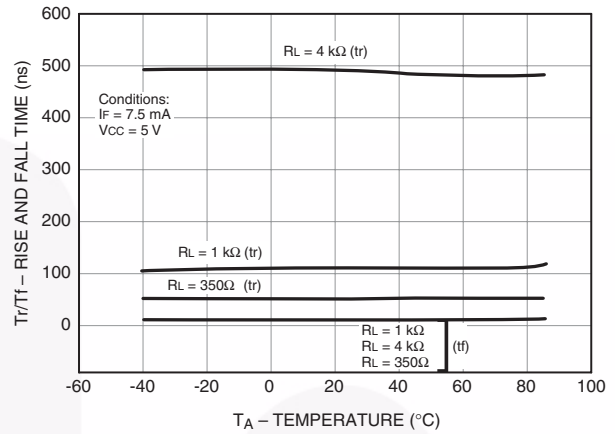


Fig. 9 Enable Propagation Delay vs. Temperature

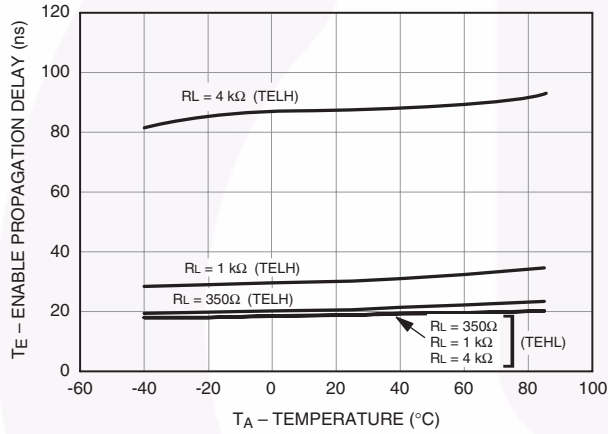


Fig. 10 Switching Time vs. Temperature

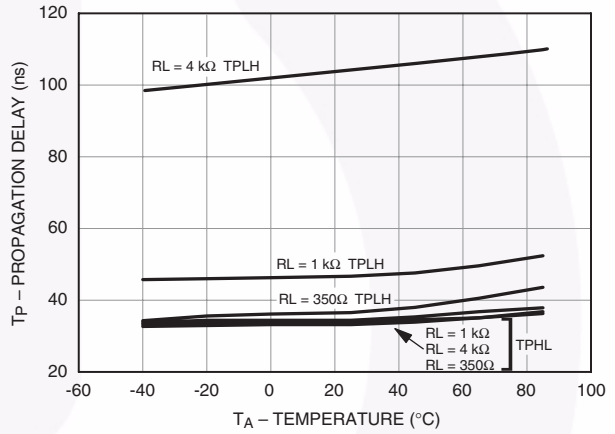
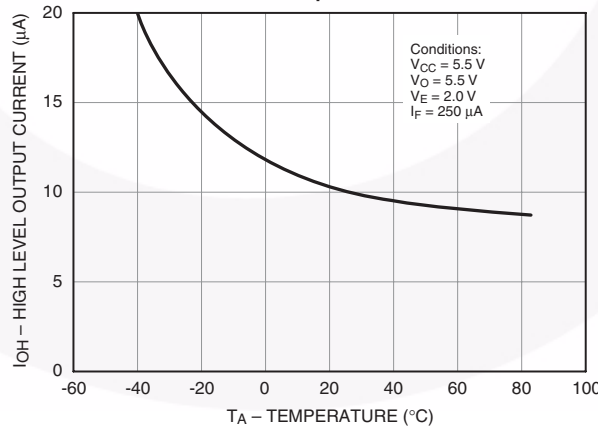


Fig. 11 High Level Output Current vs. Temperature



Test Circuits

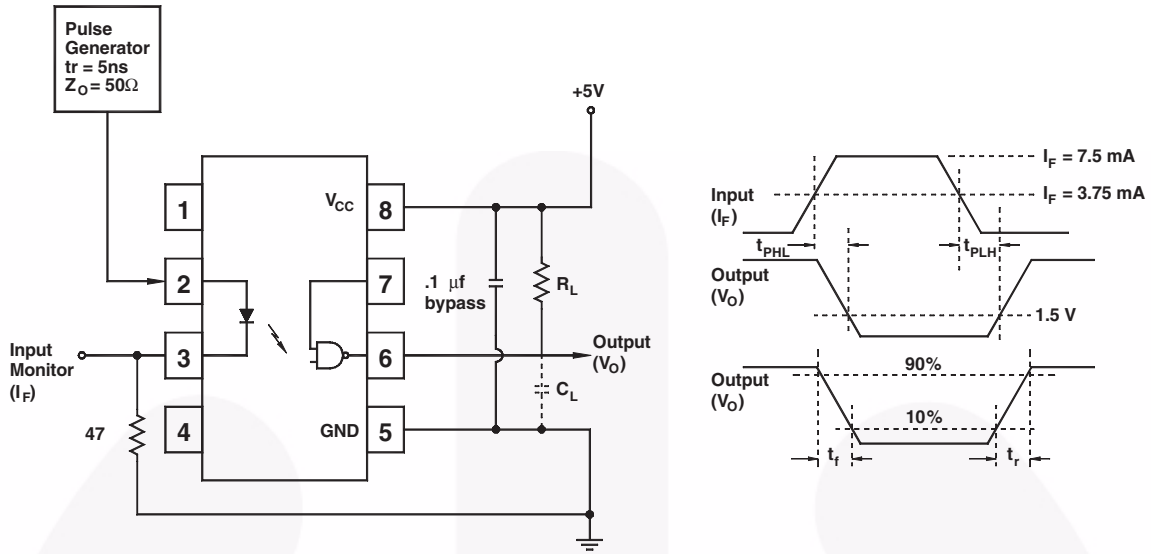


Fig. 12 Test Circuit and Waveforms for t_{PLH} , t_{PHL} , t_r and t_f

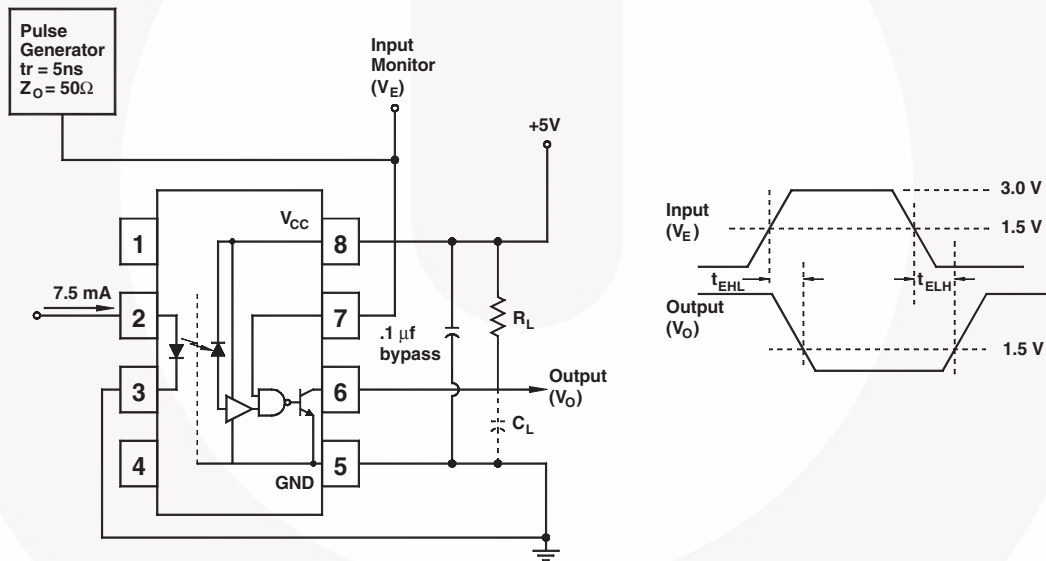


Fig. 13 Test Circuit t_{EHL} and t_{ELH}

Test Circuits (Continued)

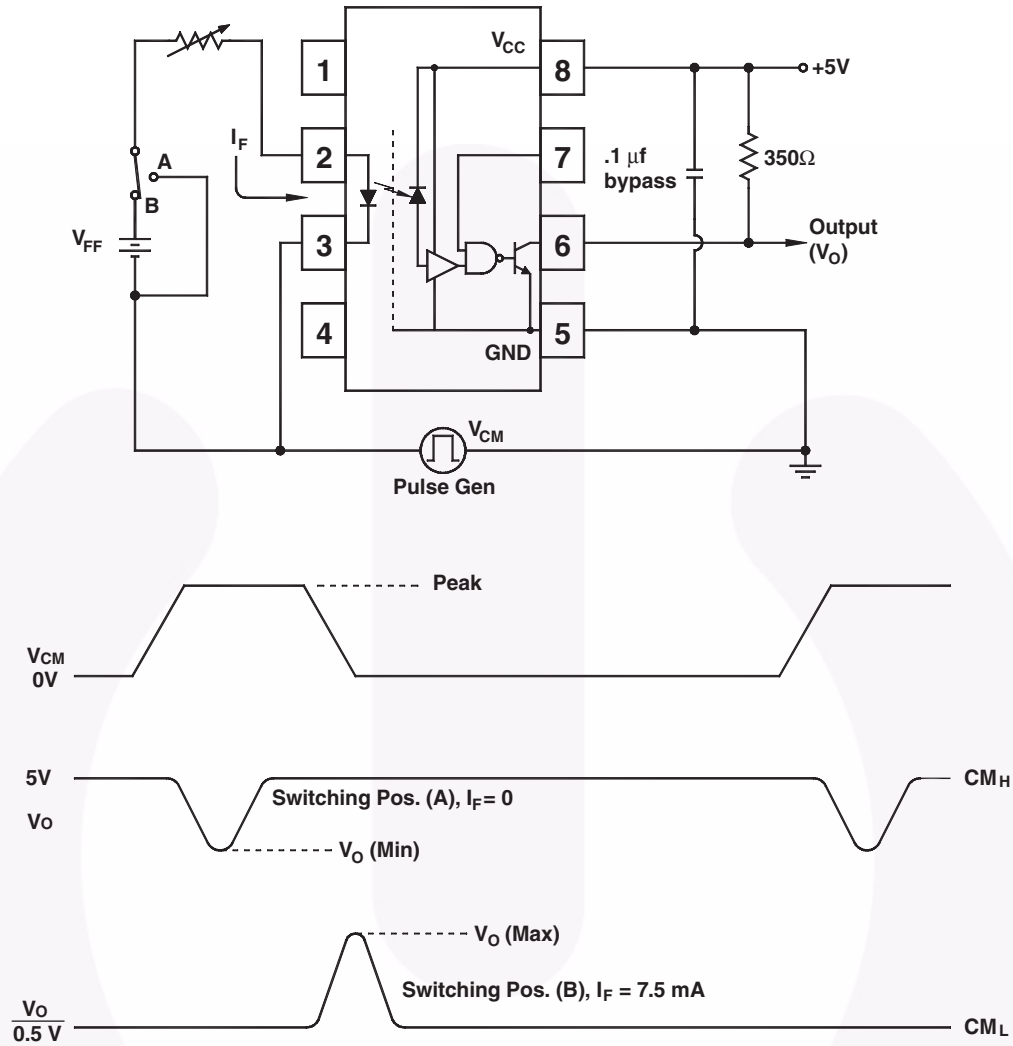
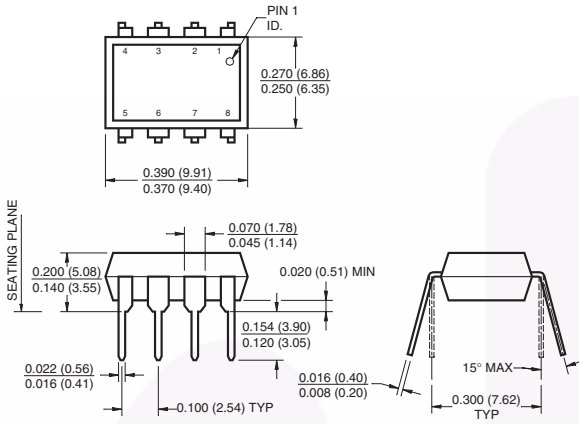


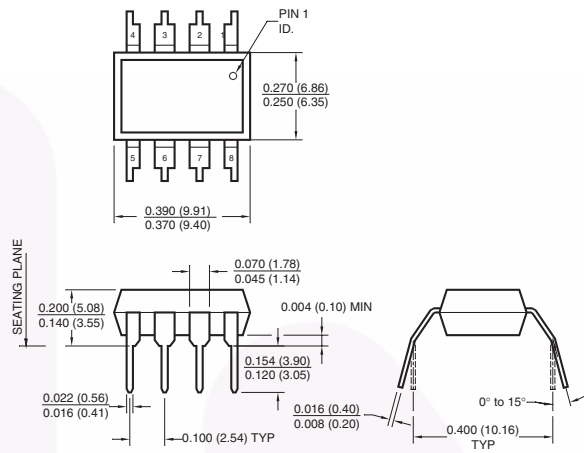
Fig. 14 Test Circuit Common Mode Transient Immunity

Package Dimensions

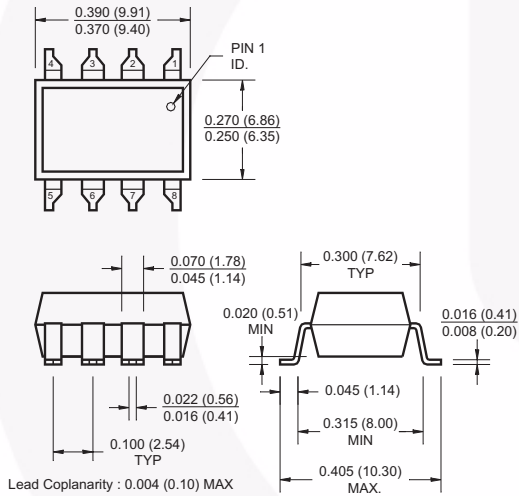
Through Hole



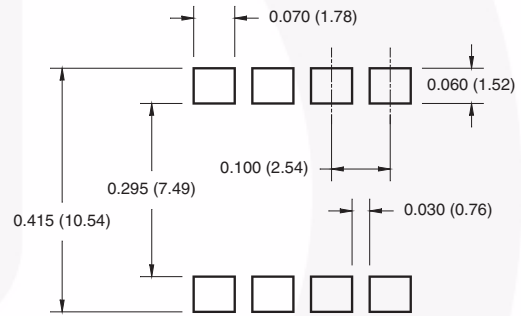
0.4" Lead Spacing



Surface Mount



8-Pin DIP – Land Pattern



Note:

All dimensions are in inches (millimeters)

Ordering Information

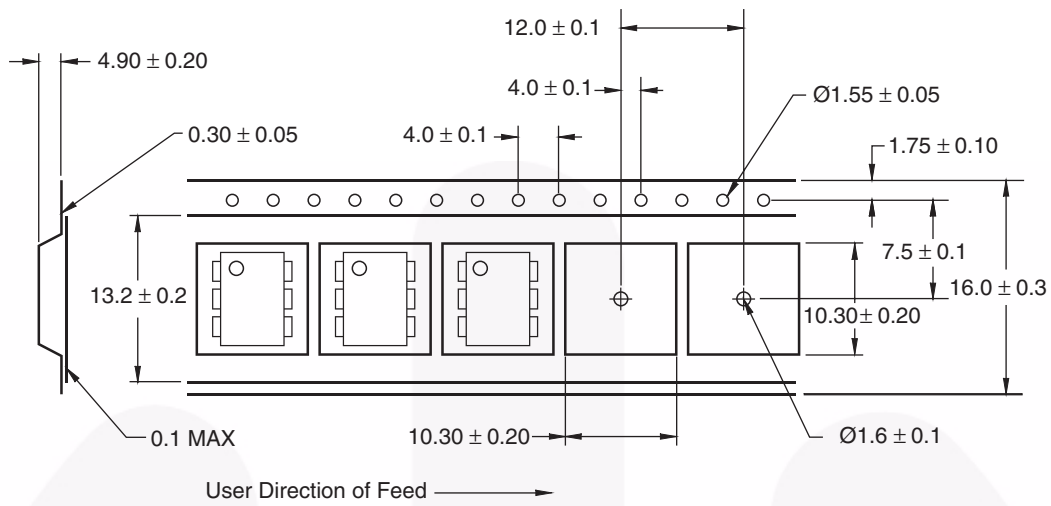
| Option | Example Part Number | Description |
|--------|---------------------|---------------------------------------|
| S | 6N137S | Surface Mount Lead Bend |
| SD | 6N137SD | Surface Mount; Tape and Reel |
| W | 6N137W | 0.4" Lead Spacing |
| V | 6N137V | VDE0884 |
| WV | 6N137WV | VDE0884; 0.4" Lead Spacing |
| SV | 6N137SV | VDE0884; Surface Mount |
| SDV | 6N137SDV | VDE0884; Surface Mount; Tape and Reel |

Marking Information

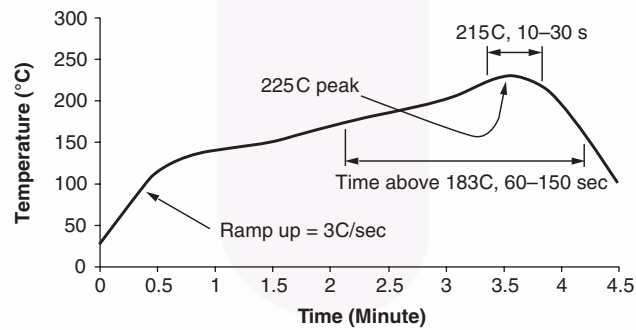


| Definitions | |
|-------------|--|
| 1 | Fairchild logo |
| 2 | Device number |
| 3 | VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table) |
| 4 | Two digit year code, e.g., '03' |
| 5 | Two digit work week ranging from '01' to '53' |
| 6 | Assembly package code |

Tape Specifications



Reflow Profile





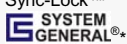


- Peak reflow temperature: 225C (package surface temperature)
- Time of temperature higher than 183C for 60-150 seconds
- One time soldering reflow is recommended



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| CorePLUS™ | Green FPS™ | QFET® | TinyBoost™ |
| CorePOWER™ | Green FPS™ e-Series™ | QS™ | TinyBuck™ |
| CROSSVOL™ | Gmax™ | Quiet Series™ | TinyCalc™ |
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| Dual Cool™ | MegaBuck™ | SignalWise™ | TinyPWM™ |
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| EfficientMax™ | MicroFET™ | SMART START™ | TriFault Detect™ |
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|--------------------------|-----------------------|---|
| Advance Information | Formative / In Design | Datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
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| No Identification Needed | Full Production | Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design. |
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