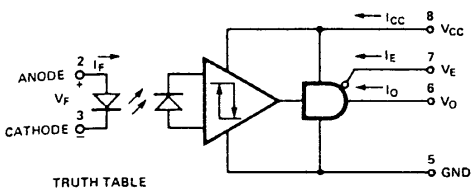
942-285

HEWLETT PACKARD

20 M BAUD HIGH CMR LOGIC GATE OPTOCOUPLER

HCPL-2400 HCPL-2411

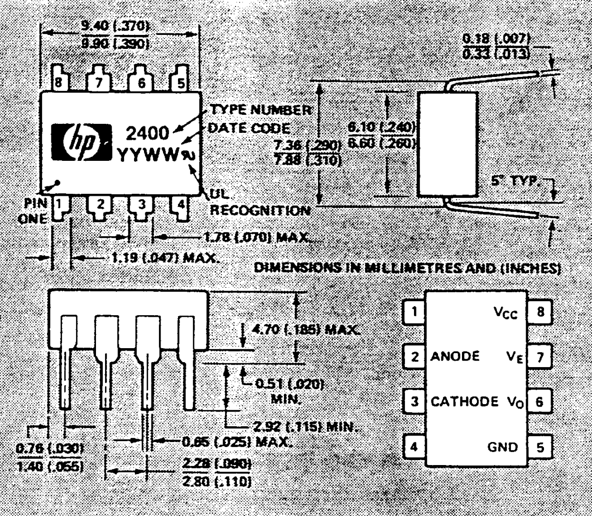
SCHEMATIC



TRUTH TABLE
(POSITIVE LOGIC)

INPUT	ENABLE	OUTPUT
H	L	L
L	L	H
H	H	Z
L	H	Z

OUTLINE DRAWING



Features

- HIGH SPEED: 40 MBd TYPICAL DATA RATE
- HIGH COMMON MODE REJECTION
- HCPL-2400 = 50 V_{CM}
- HCPL-2411 = 300 V_{CM}
- AC PERFORMANCE GUARANTEED OVER TEMPERATURE
- COMPATIBLE WITH TTL, STTL, LSTTL, AND HCMOS LOGIC FAMILIES
- NEW, HIGH SPEED AlGaAs EMITTER
- THREE STATE OUTPUT (NO PULL-UP RESISTOR REQUIRED)
- HIGH POWER SUPPLY NOISE IMMUNITY
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 1440 Vac, 1 MINUTE AND 2500 Vac, 1 MINUTE (OPTION 010).
- HCPL-5400/1 COMPATIBILITY

Applications

- ISOLATION OF HIGH SPEED LOGIC SYSTEMS
- COMPUTER-PERIPHERAL INTERFACES
- ISOLATED BUS DRIVER (NETWORKING APPLICATIONS)
- SWITCHING POWER SUPPLIES
- GROUND LOOP ELIMINATION
- HIGH SPEED DISK DRIVE I/O
- DIGITAL ISOLATION FOR A/D, D/A CONVERSION
- PULSE TRANSFORMER REPLACEMENT

Description

The HCPL-2400/11 high speed optocouplers combine an 820 nm AlGaAs photon emitting diode with a high speed photon detector. This combination results in very high data rate capability and low input current. The three state output eliminates the need for a pull-up resistor and allows for direct drive of data buses. The hysteresis provides typically 0.25 mA of differential mode noise immunity and minimizes the potential for output signal chatter. Improved power supply rejection minimizes the need for special power supply bypassing precautions.

The electrical and switching characteristics of the HCPL-2400/11 are guaranteed over the temperature range of 0°C to 70°C.

The HCPL-2400/11 are compatible with TTL, STTL, LSTTL and HCMOS logic families. When Schottky type TTL devices (STTL) are used, a data rate performance of 20 MBd over temperature is guaranteed when using the application circuit of Figure 13. Typical data rates are 40 MBd.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.75	5.25	Volts
Input Current (High)	$I_{F(ON)}$	4	8	mA
Input Voltage (Low)	$V_{F(OFF)}$	—	0.8	Volts
Enable Voltage (Low)	V_{EL}	0	0.8	Volts
Enable Voltage (High)	V_{EH}	2.0	V_{CC}	Volts
Operating Temperature	T_A	0	70°	°C
Fan Out	N		5	TTL Loads

OPTOCOUPLERS

Absolute Maximum Ratings

(No derating required up to 85° C)

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	−55	125	°C	
Operating Temperature	T_A	0	85	°C	
Lead Solder Temperature	260° C for 10 s. (1.6 mm below seating plane)				
Average Forward Input Current	I_F		10.0	mA	
Peak Forward Input Current	I_{FPK}		20.0	mA	9
Reverse Input Voltage	V_R		3.0	V	
Supply Voltage	V_{CC}	0	7.0	V	
Three State Enable Voltage	V_E	−0.5	10.0	V	
Average Output Collector Current	I_O	−25.0	25.0	mA	
Output Collector Voltage	V_O	−0.5	10.0	V	
Output Collector Power Dissipation	P_O		40.0	mW	

Electrical Characteristics

For $0° C \le T_A \le 70° C$, $4.75\ V \le V_{CC} \le 5.25\ V$, $4\ mA \le I_{F(ON)} \le 8\ mA$, $2.0\ V \le V_{EH} \le 5.25$, $0\ V \le V_{EL} \le 0.8\ V$, $0\ V \le V_{F(OFF)} \le 0.8\ V$ except where noted. All Typicals at $T_A = 25° C$, $V_{CC} = 5\ V$, $I_{F(ON)} = 5.0\ mA$, $V_{F(OFF)} = 0\ V$ except where noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Figure	Note
Logic Low Output Voltage	V_{OL}			0.5	Volts	I_{OL} = 8.0 mA (5 TTL Loads)		1	
Logic High Output Voltage	V_{OH}	2.4			Volts	I_{OH} = −4.0 mA		2	
Output Leakage Current	I_{OHH}			100	μA	V_O = 5.25 V	V_F = 0.8 V		
Logic High Enable Voltage	V_{EH}	2.0			Volts				
Logic Low Enable Voltage	V_{EL}			0.8	Volts				
Logic High Enable Current	I_{EH}			20	μA	V_E = 2.4 V			
				100	μA	V_E = 5.25 V			
Logic Low Enable Current	I_{EL}		−0.28	−0.4	mA	V_E = 0.4V			
Logic Low Supply Current	I_{CCL}		19	26	mA	V_{CC} = 5.25 V			
Logic High Supply Current	I_{CCH}		17	26	mA	V_E = 0 V			
High Impedance State Supply Current	I_{CCZ}		22	28	mA	V_{CC} = 5.25 V V_E = 5.25 V			
High Impedance State Output Current	I_{OZL}			20	μA	V_O = 0.4V	V_E = 2 V		
	I_{OZH}			20	μA	V_O = 2.4 V	V_E = 2 V		
	I_{OZH}			100	μA	V_O = 5.25 V			
Logic Low Short Circuit Output Current	I_{OSL}		52		mA	$V_O = V_{CC}$ = 5.25 V	I_F = 8 mA		1
Logic High Short Circuit Output Current	I_{OSH}		−45		mA	V_{CC} = 5.25 V	I_F = 0 mA, V_O = GND		1
Input Current Hysteresis	I_{HYS}		0.25		mA	V_{CC} = 5 V		3	
Input Forward Voltage	V_F	1.1	1.3	1.5	Volts	I_F = 5 mA, T_A = 25° C		4	
Input Reverse Breakdown Voltage	V_R	3.0	5.0		Volts	I_R = 10 μA, T_A = 25° C			
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		−1.44		mV/° C	I_F = 5 mA		4	
Input-Output Insulation	$I_{I\text{-}O}$			1	μA	45% RH, t = 5s, $V_{I\text{-}O}$ = 3kVdc, T_A = 25°C			2, 8
Option 010	V_{ISO}	2500			V_{RMS}	RH ≤ 50%, t = 1 min.			10
Input-Output Resistance	$R_{I\text{-}O}$		10^{12}		ohms	$V_{I\text{-}O}$ = 500 VDC			2
Input-Output Capacitance	$C_{I\text{-}O}$		0.6		pF	f = 1 MHz, $V_{I\text{-}O}$ = 0 V dc			2
Input Capacitance	C_{IN}		20		pF	f = 1 MHz, V_F = 0V, Pins 2 and 3			

Switching Characteristics

$0°C \le T_A \le 70°C$, $4.75\ V \le V_{CC} \le 5.25\ V$, $0.0\ V \le V_{EN} \le 0.8\ V$. $4\ mA \le I_F \le 8.0\ mA$. All Typicals $V_{CC} = 5\ V$, $T_A = 25°C$, $I_F = 5.0\ mA$ except where noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}			55	ns	$I_{F(ON)} = 7.0\ mA$	5, 6, 7	4
		15	33	60	ns		5, 6, 7	3
Propagation Delay Time to Logic High Output Level	t_{PLH}			55	ns	$I_{F(ON)} = 7.0\ mA$	5, 6, 7	4
		15	30	60	ns		5, 6, 7	3
Pulse Width Distortion	$\lvert t_{PHL} - t_{PLH} \rvert$		2	15	ns	$I_{F(ON)} = 7.0\ mA$	5, 8	4
			3	25	ns		5, 8	
Channel Distortion	Δt_{PHL}		8	25	ns		5	5
	Δt_{PLH}		8	25	ns		5	5
Output Rise Time	t_r		20		ns		5	
Output Fall Time	t_f		10		ns		5	
Output Enable Time to Logic High	t_{PZH}		15		ns		9, 10	
Output Enable Time to Logic Low	t_{PZL}		30		ns		9, 10	
Output Disable Time from Logic High	t_{PHZ}		20		ns		9, 10	
Output Disable Time from Logic Low	t_{PLZ}		15		ns		9, 10	
Logic High Common Mode Transient Immunity	$\lvert CM_H \rvert$ 2400	1000	10,000		V/μs	$V_{CM} = 50\ V$; $T_A = 25°C$, $I_F = 0$	11, 12	6
	2411	1000			V/μs	$V_{CM} = 300\ V$; $T_A = 25°C$, $I_F = 0$	11, 12	6
Logic Low Common Mode Transient Immunity	$\lvert CM_L \rvert$ 2400	1000	10,000		V/μs	$V_{CM} = 50\ V$; $T_A = 25°C$, $I_F = 4\ mA$	11, 12	6
	2411	1000			V/μs	$V_{CM} = 300\ V$; $T_A = 25°C$, $I_F = 4\ mA$	11, 12	6
Power Supply Noise Immunity	PSNI		0.5		V_{p-p}	$V_{CC} = 5.0\ V$, $48\ Hz \le F_{AC} \le 50\ MHz$		7

Notes:

1. Duration of output short circuit time not to exceed 10 ms.
2. Device considered a two terminal device: pins 1–4 shorted together, and pins 5–8 shorted together.
3. t_{PHL} propagation delay is measured from the 50% level on the rising edge of the input current pulse to the 1.5 V level on the falling edge of the output pulse. The t_{PLH} propagation delay is measured from the 50% level on the falling edge of the input current pulse to the 1.5 V level on the rising edge of the output pulse.
4. This specification simulates the worst case operating conditions of the HCPL-2400/11 over the recommended operating temperature and V_{CC} range with the suggested applications circuit of Figure 13.
5. Channel distortion describes the worst case variation of propagation delay from one part to another at identical operating conditions.
6. CM_H is the maximum slew rate of common mode voltage that can be sustained with the output voltage in the logic high state ($V_{O(MIN)} > 2.0\ V$). CM_L is the maximum slew rate of common mode voltage that can be sustained with the output voltage in the logic low state ($V_{O(MAX)} < 0.8\ V$).
7. Power Supply Noise Immunity is the peak to peak amplitude of the ac ripple voltage on the V_{CC} line that the device will withstand and still remain in the desired logic state. For desired logic high state, $V_{OH(MIN)} > 2.0\ V$, and for desired logic low state, $V_{OL(MAX)} < 0.8$ volts.
8. This is a proof test. This rating is equally validated by a 2500 V ac, 1 second test per UL E55 361.
9. Peak Forward Input Current pulse width < 50 μs at 1 KHz maximum repetition rate.
10. See Option 010 data sheet for more information.

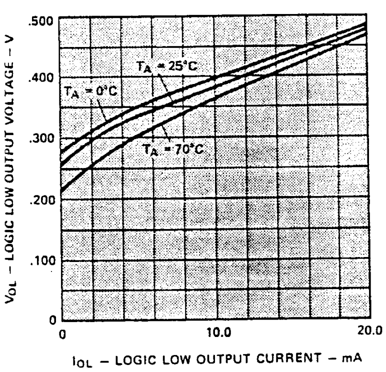


Figure 1. Typical Logic Low Output Voltage vs. Logic Low Output Current

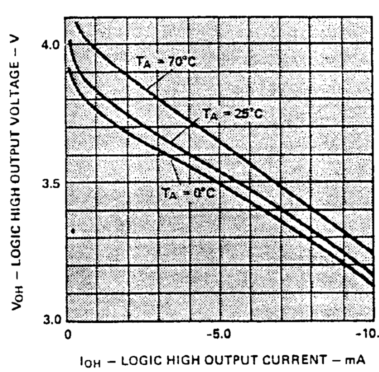


Figure 2. Typical Logic High Output Voltage vs. Logic High Output Current

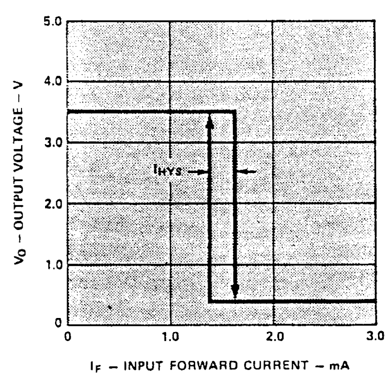


Figure 3. Typical Output Voltage vs. Input Forward Current

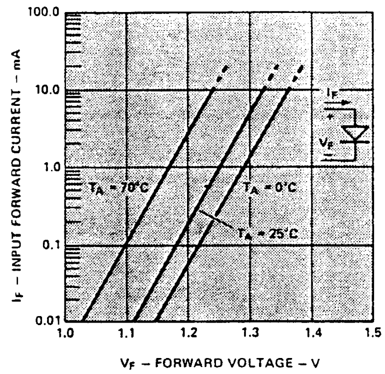


Figure 4. Typical Diode Input Forward Current Characteristic

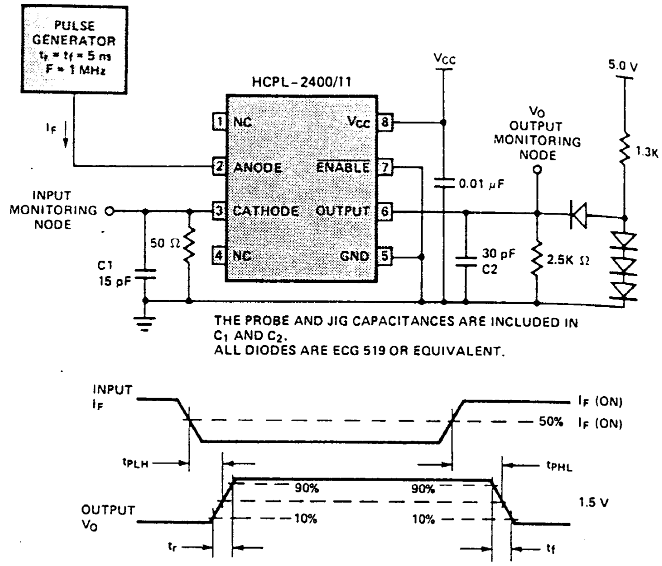


Figure 5. Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f

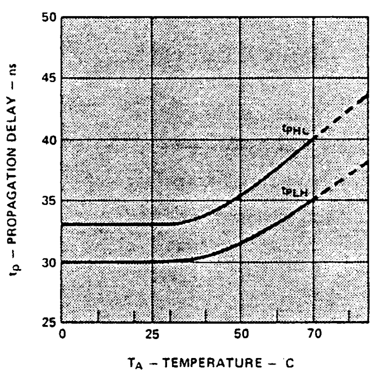


Figure 6. Typical Propagation Delay vs. Ambient Temperature

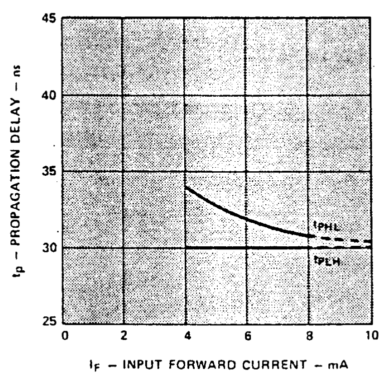


Figure 7. Typical Propagation Delay vs. Input Forward Current

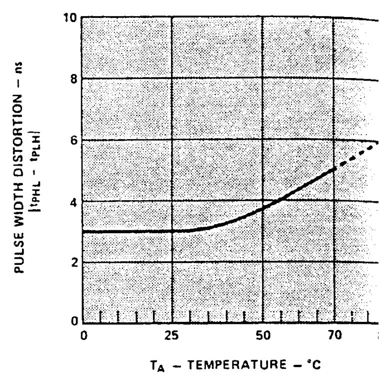
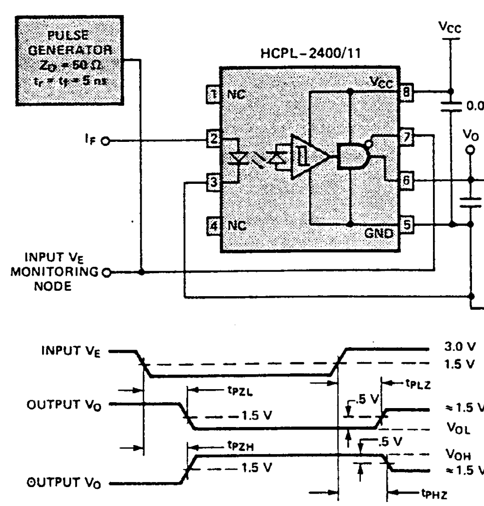


Figure 8. Typical Pulse Width Distortion vs. Ambient Temperature



	S_1	S_2
t_{PHZ}	CLOSED	CLOSED
t_{PZH}	OPEN	CLOSED
t_{PLZ}	CLOSED	CLOSED
t_{PZL}	CLOSED	OPEN

ALL DIODES ARE ECG 519 OR EQUIVALENT
C1 = 30 pF INCLUDING PROBE AND JIG CAPACITANCE.

Figure 9. Test Circuit for t_{PHZ}, t_{PZH}, t_{PLZ} and t_{PZL}.

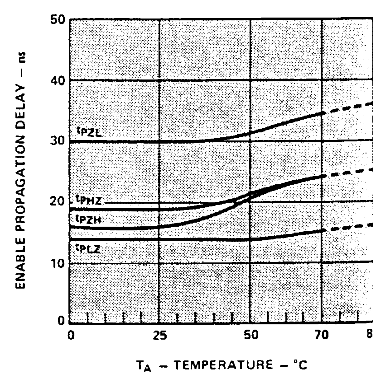
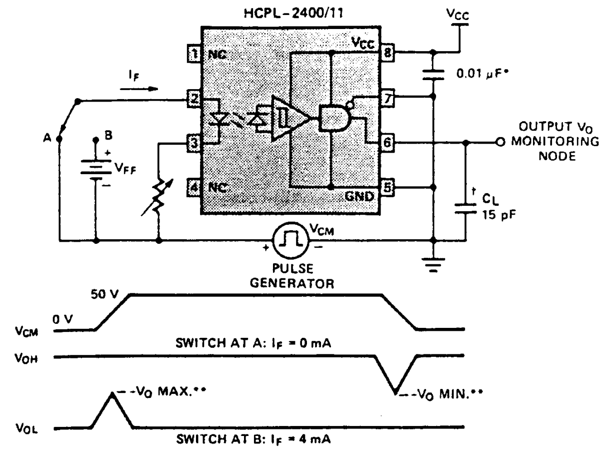


Figure 10. Typical Enable Propagation Delay vs. Ambient Temperature



*MUST BE LOCATED < 1 cm FROM DEVICE UNDER TEST.
**SEE NOTE 6.
† C_L IS APPROXIMATELY 15 pF, WHICH INCLUDES PROBE AND STRAY WIRING CAPACITANCE.

Figure 11. Test Diagram for Common Mode Transient Immunity and Typical Waveforms

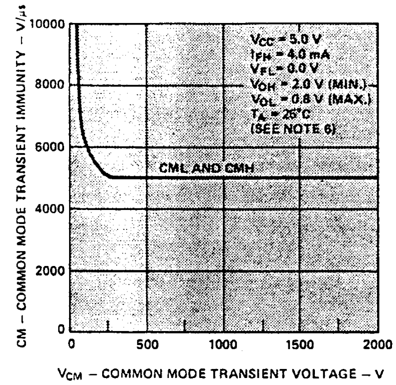


Figure 12. Typical Common Mode Transient Immunity vs. Common Mode Transient Voltage

Applications

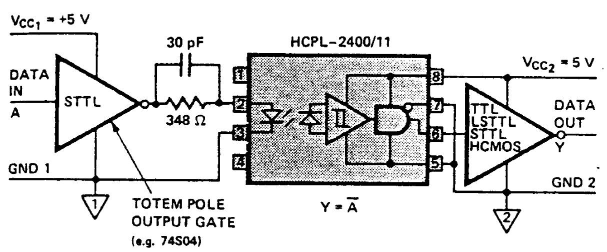


Figure 13. Recommended 20 MBd HCPL-2400/11 Interface Circuit

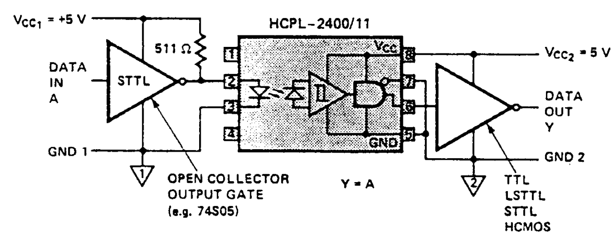


Figure 14. Alternative HCPL-2400/11 Interface Circuit

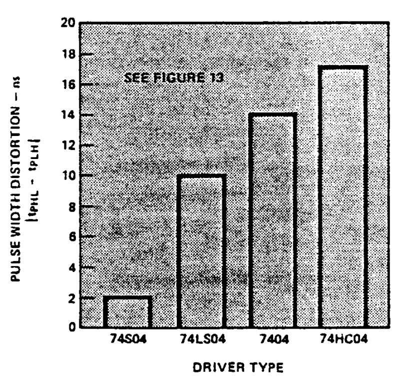


Figure 15. Typical Pulse Width Distortion vs. Input Driver Logic Family

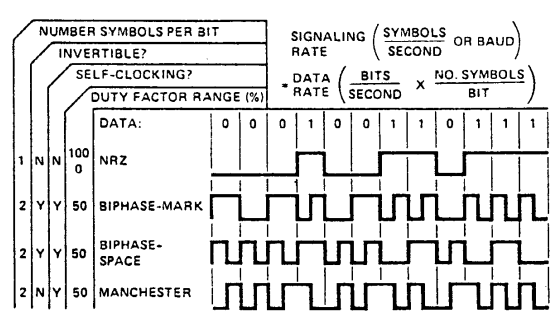


Figure 16. Modulation Code Selections

Data Rate, Pulse-Width Distortion, and Channel Distortion Definitions

In the world of data communications, a bit is defined as the smallest unit of information a computer operates with. A bit is either a Logic 1 or Logic 0, and is interpreted by a number of coding schemes. For example, a bit can be represented by one symbol through the use of NRZ code, or can contain two symbols in codes such as Biphase or Manchester (see Figure 16). The bit rate capability of a system is expressed in terms of bits/second (b/s) and the symbol rate is expressed in terms of Baud (symbols/second). For NRZ code, the bit rate capability equals the Baud capability because the code contains one symbol per bit of information. For Biphase and Manchester codes, the bit rate capability is equal to one half of the Baud capability, because there are two symbols per bit.

Propagation delay is a figure of merit which describes the finite amount of time required for a system to translate information from input to output when shifting logic levels. Propagation delay from low to high (t_{PLH}) specifies the amount of time required for a system's output to change from a Logic 0 to a Logic 1, when given a stimulus at the input. Propagation delay from high to low (t_{PHL}) specifies the amount of time required for a system's output to change from a Logic 1 to a Logic 0, when given a stimulus at the input (see Figure 5).

When t_{PLH} and t_{PHL} differ in value, pulse width distortion results. Pulse width distortion is defined as $|t_{PHL}-t_{PLH}|$ and determines the maximum data rate capability of a distortion-limited system. Maximum pulse width distortion on the order of 20–30% is typically used when specifying the maximum data rate capabilities of systems. The exact figure depends on the particular application (RS-232, PCM, T-1, etc.).

Channel distortion, (Δt_{PHL}, Δt_{PLH}), describes the worst case variation of propagation delay from device to device at identical operating conditions. Propagation delays tend to shift as operating conditions change, and channel distortion specifies the uniformity of that shift. Specifying a maximum value for channel distortion is helpful in parallel data transmission applications where the synchronization of signals on the parallel lines is important.

The HCPL-2400/11 optocouplers offer the advantages of specified propagation delay (t_{PLH}, t_{PHL}), pulse-width distortion ($|t_{PLH}-t_{PHL}|$), and channel distortion (Δt_{PLH}, Δt_{PHL}) over temperature, input forward current, and power supply voltage ranges.

Applications Circuits

A recommended application circuit for high speed operation is shown in Figure 13. Due to the fast current switching capabilities of Schottky family TTL logic (74STTL), data rates of 20 MBd are achievable from 0 to 70°C. the 74S04 totem-pole driver sources current to series-drive the input of the HCPL-2400/11 optocoupler. The 348Ω resistor limits the LED forward current. The 30 pF speed-up capacitor assists in the turn-on and turn-off of the LED, increasing the data rate capability of the circuit. On the output side, the following logic can be directly driven by the output of the HCPL-2400/11 since a pull-up resistor is not required. If desired, a non-inverting buffer may be substituted on either the input or the output side to change the circuit function from Y = A to Y = A. This circuit satisfies all recommended operating conditions.

An alternative circuit is shown in Figure 14, which utilizes a 74S05 open-collector inverter to shunt-drive the HCPL-2400/11 optocoupler. This circuit also satisfies all recommended operating conditions.

The HCPL-2400/11 optocouplers are compatible with other logic familes, such as TTL, LSTTL, and HCMOS. However, the output drive capabilities of Schottky family devices greatly exceed those associated with TTL, LSTTL, and HCMOS logic families, and are recommended in high data rate (20 MBd) applications where fast drive current transitions are required to operate the HCPL-2400/11 with minimum pulse-width distortion.

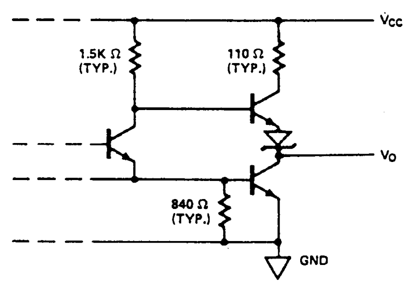


Figure 17. Typical HCPL-2400/11 Output Schematic