600MHz, Low Noise, AC Precision Fully Differential Input/Output Amplifier/Driver

FEATURES

- **Fully Differential Input and Output**
- **Low Noise: 1.5nV/√Hz Input-Referred**
- **Very Low Distortion ($2V_{P-P}$, 10MHz): –96dBc**
- **Closed loop –3dB Bandwidth: 600MHz**
- **Slew Rate: 700V/µs**
- Adjustable Output Common Mode Voltage
- Rail-to-Rail Output Swing
- Input Range Extends to Ground
- High Output Current: 65mA (Typ)
- 2.7V to 5.25V Supply Voltage Range
- Low Power Shutdown
- Tiny 3mm × 3mm × 0.75mm 16-Pin QFN Package

APPLICATIONS

- Differential Input A/D Converter Driver
- Single-Ended to Differential Conversion/Amplification
- Common Mode Level Translation
- Low Voltage, Low Noise, Signal Processing

DESCRIPTION

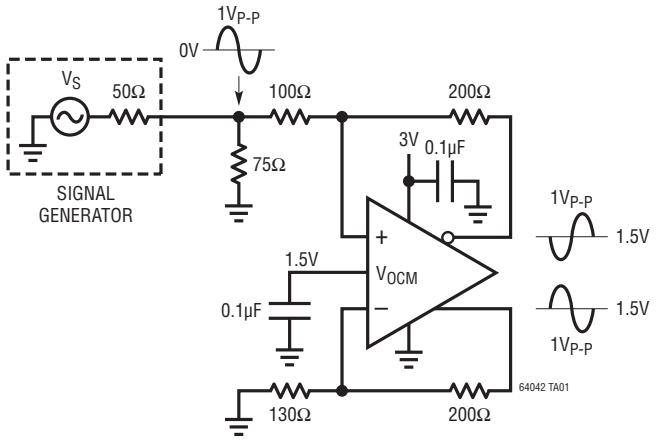
The LTC®6404-2 is an AC precision, very low noise, low distortion, fully differential input/output amplifier optimized for 3V, single supply operation. The LTC6404-2 is stable for gains exceeding 2V/V and has a closed-loop bandwidth extending from DC to 600MHz. A unity-gain stable LTC6404-1 is also available. In addition to the normal unfiltered outputs (OUT^+ and $OUT^–$), the LTC6404-2 has a built-in 88.5MHz differential single-pole lowpass filter and an additional pair of filtered outputs ($OUTF^+$, and $OUTF^–$). An input referred voltage noise of 1.5nV/√Hz makes the LTC6404-2 uniquely able to drive state-of-the-art 14- to 18-bit ADCs while operating on the same supply voltage, saving system cost and power. The LTC6404-2 is characterized, and maintains its performance for supplies as low as 2.7V. It draws only 29.8mA, and has a hardware shutdown feature which reduces current consumption to 250µA.

The LTC6404-2 is available in a compact 3mm × 3mm 16-pin leadless QFN package and operates over a –40°C to 125°C temperature range.

, LT, LTC and LTM are registered trademarks of Linear Technology Corporation.
All other trademarks are the property of their respective owners.

TYPICAL APPLICATION

Single-Ended Input to Differential Output with Common Mode Level Shifting



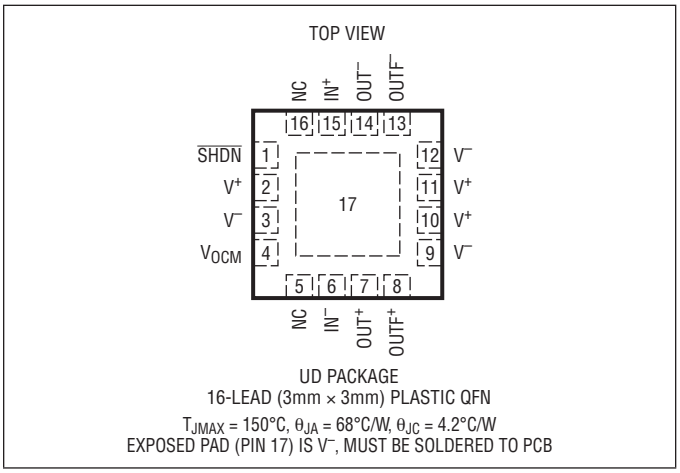
Downloaded from Elcodis.com electronic components distributor

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 5.5V
Input Voltage
(IN^+, IN^-, V_{OCM}, $\overline{SHDN}$) (Note 2) ..... V^+ to V^-
Input Current
(IN^+, IN^-, V_{OCM}, $\overline{SHDN}$) (Note 2) .....±10mA
Output Short-Circuit Duration (Note 3) ..... Indefinite
Output Current (Continuous)
($OUTF^+$, $OUTF^-$) DC + AC_{RMS}.....±40mA
Operating Temperature Range
(Note 4) ..... –40°C to 125°C
Specified Temperature Range
(Note 5) ..... –40°C to 125°C
Junction Temperature ..... 150°C
Storage Temperature Range..... –65°C to 150°C

PIN CONFIGURATION



UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 68°C/W, θ_{JC} = 4.2°C/W
EXPOSED PAD (PIN 17) IS V^-, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6404CUD-2#PBF	LTC6404CUD-2#TRPBF	LCLX	16-Lead (3mm × 3mm) Plastic QFN	0°C to 70°C
LTC6404IUD-2#PBF	LTC6404IUD-2#TRPBF	LCLX	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 85°C
LTC6404HUD-2#PBF	LTC6404HUD-2#TRPBF	LCLX	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

Downloaded from Elcodis.com electronic components distributor

LTC6404-2 DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3V, V^- = 0V, V_{CM} = V_{OCM} = V_{ICM} = Mid-Supply, $V_{\overline{SHDN}}$ = OPEN, R_I = 100Ω, R_F = 200Ω, R_L = OPEN, R_{BAL} = 100kΩ (See Figure 1) unless otherwise noted. V_S is defined as ($V^+ – V^-$). V_{OUTCM} = ($V_{OUT}^+ + V_{OUT}^-$)/2. V_{ICM} is defined as ($V_{IN}^+ + V_{IN}^-$)/2. $V_{OUTDIFF}$ is defined as ($V_{OUT}^+ – V_{OUT}^-$). V_{INDIFF} = ($V_{INP} – V_{INM}$).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OSDIFF}	Differential Offset Voltage (Input Referred)	V_S = 2.7V to 5.25V	●		±0.5	±2	mV
$\Delta V_{OSDIFF}/\Delta T$	Differential Offset Voltage Drift (Input Referred)	V_S = 2.7V to 5.25V	●		1		µV/°C
I_B	Input Bias Current (Note 6)	V_S = 2.7V to 5.25V	●	–60	–23	0	µA
$\Delta I_B/\Delta T$	Input Bias Current Drift (Note 6)	V_S = 2.7V to 5.25V			0.01		µA/°C
I_{OS}	Input Offset Current (Note 6)	V_S = 2.7V to 5.25V	●		±1	±10	µA
R_{IN}	Input Resistance	Common Mode Differential Mode			1000 3		kΩ kΩ
C_{IN}	Input Capacitance				1		pF
e_n	Differential Input Referred Noise Voltage Density	f = 1MHz			1.5		nV/√Hz
i_n	Input Noise Current Density	f = 1MHz			3		pA/√Hz
e_{nVOCM}	Input Referred Common Mode Noise Voltage Density	f = 1MHz, Referred to V_{OCM} Pin			10.5		nV/√Hz
V_{ICMR} (Note 7)	Input Signal Common Mode Range	V_S = 3V V_S = 5V	● ●	0 0		1.6 3.6	V V
CMRRI (Note 8)	Input Common Mode Rejection Ratio (Input Referred) $\Delta V_{ICM}/\Delta V_{OSDIFF}$	V_S = 3V, ΔV_{ICM} = 0.75V V_S = 5V, ΔV_{ICM} = 1.25V			60 60		dB dB
CMRRIO (Note 8)	Output Common Mode Rejection Ratio (Input Referred) $\Delta V_{OCM}/\Delta V_{OSDIFF}$	V_S = 5V, ΔV_{OCM} = 1V			66		dB
PSRR (Note 9)	Differential Power Supply Rejection ($\Delta V_S/\Delta V_{OSDIFF}$)	V_S = 2.7V to 5.25V	●	60	94		dB
PSRRCM (Note 9)	Output Common Mode Power Supply Rejection ($\Delta V_S/\Delta V_{OSCM}$)	V_S = 2.7V to 5.25V	●	50	63		dB
G_{CM}	Common Mode Gain ($\Delta V_{OUTCM}/\Delta V_{OCM}$) Common Mode Gain Error	V_S = 5V, ΔV_{OCM} = 1V V_S = 5V, ΔV_{OCM} = 1V	● ●	 –0.6	1 –0.25	 0.1	V/V %
BAL	Output Balance ($\Delta V_{OUTCM}/\Delta V_{OUTDIFF}$)	$\Delta V_{OUTDIFF}$ = 2V Single-Ended Input Differential Input	 ● ●		 –60 –66	 –40 –40	 dB dB
V_{OSCM}	Common Mode Offset Voltage ($V_{OUTCM} – V_{OCM}$)	V_S = 2.7V to 5.25V	●		±10	±50	mV
$\Delta V_{OSCM}/\Delta T$	Common Mode Offset Voltage Drift	V_S = 2.7V to 5.25V			20		µV/°C
V_{OUTCMR} (Note 7)	Output Signal Common Mode Range (Voltage Range for the V_{OCM} Pin)	V_S = 3V V_S = 5V	● ●	1.1 1.1		2 4	V V
R_{INVOCM}	Input Resistance, V_{OCM} Pin		●	8	14	20	kΩ
V_{MID}	Voltage at the V_{OCM} Pin	V_S = 3V	●	1.45	1.5	1.55	V
V_{OUT}	Output Voltage, High, Either Output Pin (Note 10)	V_S = 3V, I_L = 0 V_S = 3V, I_L = –5mA V_S = 3V, I_L = –20mA	● ● ●		325 360 480	550 600 750	mV mV mV
		V_S = 5V, I_L = 0 V_S = 5V, I_L = –5mA V_S = 5V, I_L = –20mA	● ● ●		460 500 650	700 750 1000	mV mV mV
	Output Voltage, Low, Either Output Pin (Note 10)	V_S = 3V, I_L = 0 V_S = 3V, I_L = 5mA V_S = 3V, I_L = 20mA	● ● ●		120 140 200	230 260 350	mV mV mV
		V_S = 5V, I_L = 0 V_S = 5V, I_L = 5mA V_S = 5V, I_L = 20mA	● ● ●		175 200 285	320 350 550	mV mV mV

Downloaded from Elcodis.com electronic components distributor

LTC6404-2 DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3V, V^- = 0V, V_{CM} = V_{OCM} = V_{ICM} = Mid-Supply, $V_{\overline{SHDN}}$ = OPEN, R_I = 100Ω, R_F = 200Ω, R_L = OPEN, R_{BAL} = 100kΩ (See Figure 1) unless otherwise noted. V_S is defined as ($V^+ – V^-$). V_{OUTCM} = ($V_{OUT}^+ + V_{OUT}^-$)/2. V_{ICM} is defined as ($V_{IN}^+ + V_{IN}^-$)/2. $V_{OUTDIFF}$ is defined as ($V_{OUT}^+ – V_{OUT}^-$). V_{INDIFF} = ($V_{INP} – V_{INM}$).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{SC}	Output Short-Circuit Current, Either Output Pin (Note 11)	V_S = 2.7V V_S = 3V V_S = 5V	● ● ●	±35 ±40 ±55	±60 ±65 ±85		mA mA mA
A_{VOL}	Large-Signal Voltage Gain	V_S = 3V			90		dB
V_S	Supply Voltage Range		●	2.7		5.25	V
I_S	Supply Current	V_S = 2.7V, $V_{\overline{SHDN}}$ = V_S – 0.6V V_S = 3V, $V_{\overline{SHDN}}$ = V_S – 0.6V V_S = 5V, $V_{\overline{SHDN}}$ = V_S – 0.6V	● ● ●		29.7 29.8 30.4	38.5 38.5 39.5	mA mA mA
$I_{\overline{SHDN}}$	Supply Current in Shutdown	V_S = 2.7V, $V_{\overline{SHDN}}$ = V_S – 2.1V V_S = 3V, $V_{\overline{SHDN}}$ = V_S – 2.1V V_S = 5V, $V_{\overline{SHDN}}$ = V_S – 2.1V	● ● ●		0.22 0.25 0.35	1 1 2	mA mA mA
V_{IL}	$\overline{SHDN}$ Input Logic Low	V_S = 2.7V to 5V	●			V^+ – 2.1	V
V_{IH}	$\overline{SHDN}$ Input Logic High	V_S = 2.7V to 5V	●	V^+ – 0.6			V
$R_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Input Impedance	V_S = 5V, $V_{\overline{SHDN}}$ = 2.9V to 0V	●	38	66	94	kΩ
t_{ON}	Turn-On Time	V_S = 3V, $V_{\overline{SHDN}}$ = 0.5V to 3V			750		ns
t_{OFF}	Turn-Off Time	V_S = 3V, $V_{\overline{SHDN}}$ = 3V to 0.5V			300		ns

LTC6404-2 AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3V, V^- = 0V, V_{CM} = V_{OCM} = V_{ICM} = Mid-Supply, $V_{\overline{SHDN}}$= OPEN, R_I = 100Ω, R_F = 200Ω, R_L = 200Ω (See Figure 2) unless otherwise noted. V_S is defined ($V^+ – V^-$). V_{OUTCM} = ($V_{OUT}^+ + V_{OUT}^-$)/2. V_{ICM} is defined as ($V_{IN}^+ + V_{IN}^-$)/2. $V_{OUTDIFF}$ is defined as ($V_{OUT}^+ – V_{OUT}^-$). V_{INDIFF} = ($V_{INP} – V_{INM}$).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SR	Slew Rate	V_S = 3V to 5V			700		V/µs
GBW	Gain-Bandwidth Product	V_S = 3V to 5V, R_F = 500Ω, R_I = 100Ω, f_{TEST} = 500MHz			900		MHz
f_{3dB}	–3dB Frequency (See Figure 2)	V_S = 3V to 5V	●	300	600		MHz
HD_{SEIN}	10MHz Distortion	V_S = 3V, $V_{OUTDIFF}$ = $2V_{P-P}$ Single-Ended Input 2nd Harmonic 3rd Harmonic			 –95 –96		 dBc dBc
HD_{DIFFIN}	10MHz Distortion	V_S = 3V, $V_{OUTDIFF}$ = $2V_{P-P}$ Differential Input 2nd Harmonic 3rd Harmonic			 –98 –99		 dBc dBc
IMD_{10M}	3rd Order IMD at 10MHz f1 = 9.5MHz, f2 = 10.5MHz	V_S = 3V, $V_{OUTDIFF}$ = $2V_{P-P}$			–100		dBc
$OIP3_{10M}$	OIP3 at 10MHz (Note 12)				53		dBm
t_S	Settling Time 2V Step at Output	1% Settling 0.1% Settling 0.01% Settling			9 12 15		ns ns ns
NF	Noise Figure, R_S = 50Ω	f = 10MHz			10		dB
$f_{3dBFILTER}$	Differential Filter 3dB Bandwidth				88.5		MHz

Downloaded from Elcodis.com electronic components distributor

LTC6404-2 ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs IN^+, IN^- are protected by a pair of back-to-back diodes. If the differential input voltage exceeds 1.4V, the input current should be limited to less than 10mA. Input pins (IN^+, IN^-, V_{OCM}, and $\overline{SHDN}$) are also protected by steering diodes to either supply. If the inputs should exceed either supply voltage, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely. Long term application of output currents in excess of the absolute maximum ratings may impair the life of the device.

Note 4: The LTC6404C/LTC6404I are guaranteed functional over the operating temperature range –40°C to 85°C. The LTC6404H is guaranteed functional over the operating temperature range –40°C to 125°C.

Note 5: The LTC6404C is guaranteed to meet specified performance from 0°C to 70°C. The LTC6404C is designed, characterized, and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LTC6404I is guaranteed to meet specified performance from –40°C to 85°C. The LTC6404H is guaranteed to meet specified performance from –40°C to 125°C.

Note 6: Input bias current is defined as the average of the input currents flowing into Pin 6 and Pin 15 (IN^-, and IN^+). Input offset current is defined as the difference of the input currents flowing into Pin 15 and Pin 6 ($I_{OS} = I_B^+ – I_B^-$)

Note 7: Input common mode range is tested using the test circuit of Figure 1 by measuring the differential gain with a ±1V differential output with V_{ICM} = mid-supply, and with V_{ICM} at the input common mode range limits listed in the Electrical Characteristics table, verifying the differential gain has not deviated from the mid supply common mode input case by more than 1%, and the common mode offset (V_{OSCM}) has not deviated from the zero bias common mode offset by more than ±20mV.

The voltage range for the output common mode range is tested using the test circuit of Figure 1 by applying a voltage on the V_{OCM} pin and testing at both mid supply and at the Electrical Characteristics table limits to verify that the the common mode offset (V_{OSCM}) has not deviated by more than ±20mV from the mid supply case.

Note 8: Input CMRR is defined as the ratio of the change in the input common mode voltage at the pins IN^+ or IN^- to the change in differential input referred voltage offset. Output CMRR is defined as the ratio of the change in the voltage at the V_{OCM} pin to the change in differential input referred voltage offset. These specifications are strongly dependent on feedback ratio matching between the two outputs and their respective inputs, and is difficult to measure actual amplifier performance. See “The Effects of Resistor Pair Mismatch” in the General Applications Section of this datasheet. For a better indicator of actual amplifier performance independent of feedback component matching, refer to the PSRR specification.

Note 9: Differential power supply rejection (PSRR) is defined as the ratio of the change in supply voltage to the change in differential input referred voltage offset. Common mode power supply rejection (PSRRCM) is defined as the ratio of the change in supply voltage to the change in the common mode offset, $V_{OUTCM} – V_{OCM}$.

Note 10: This parameter is pulse tested. Output swings are measured as differences between the output and the respective power supply rail.

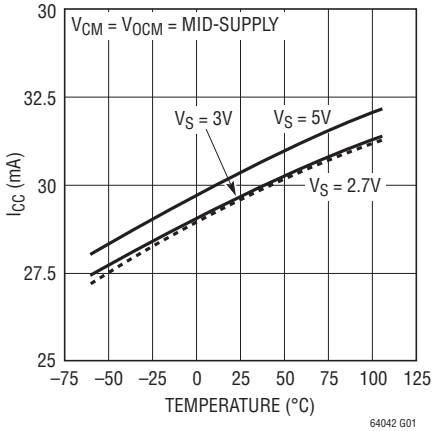
Note 11: This parameter is pulse tested. Extended operation with the output shorted may cause junction temperatures to exceed the 125°C limit and is not recommended. See Note 3 for more details.

Note 12: Since the LTC6404-2 is a voltage feedback amplifier with low output impedance, a resistive load is not required when driving an ADC. Therefore, typical output power is very small. In order to compare the LTC6404-2 with amplifiers that require 50Ω loads, the output voltage swing of the LTC6404-2 driving an ADC is converted into an effective OIP3 as if the LTC6404-2 were driving a 50Ω load.

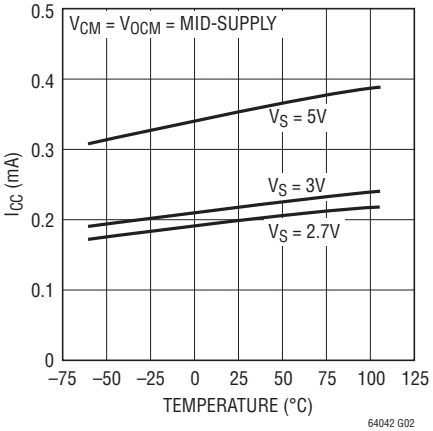
Downloaded from Elcodis.com electronic components distributor

TYPICAL PERFORMANCE CHARACTERISTICS

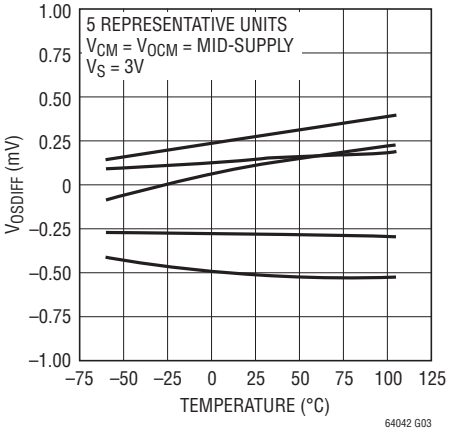
Active Supply Current vs Temperature



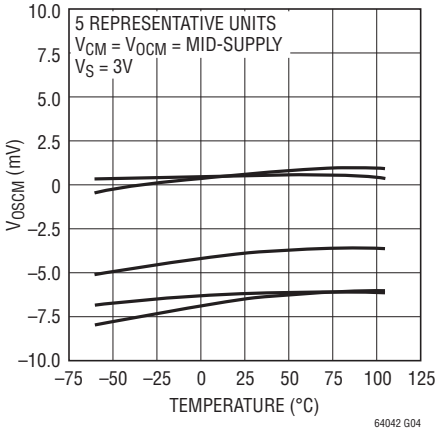
Shutdown Supply Current vs Temperature



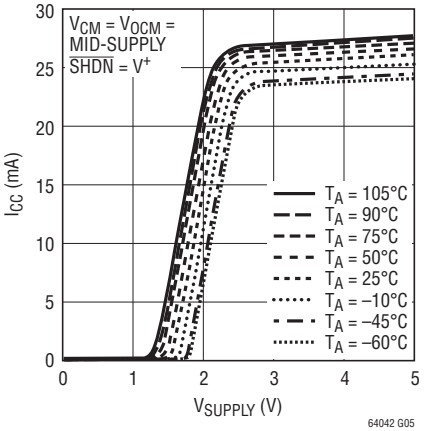
Differential Voltage Offset (Input Referred) vs Temperature



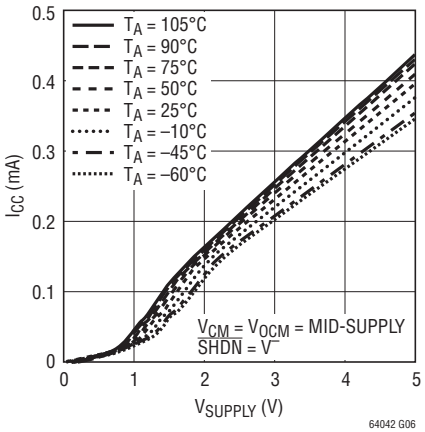
Common Mode Voltage Offset vs Temperature



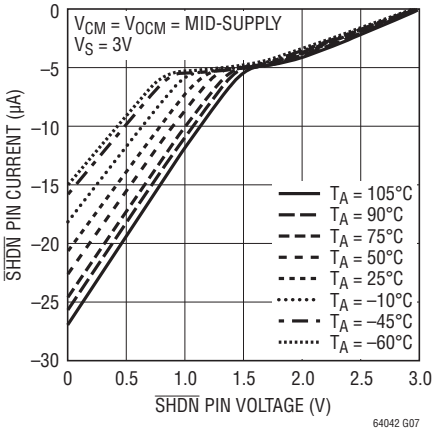
Active Supply Current vs Supply Voltage and Temperature



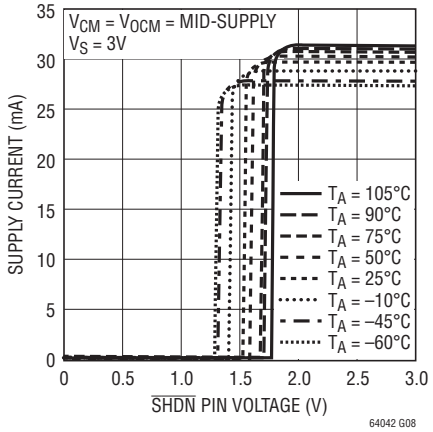
SHDN Supply Current vs Supply Voltage and Temperature



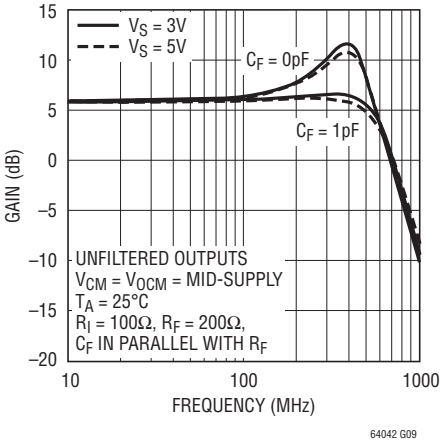
SHDN Pin Current vs SHDN Pin Voltage and Temperature



Supply Current vs SHDN Pin Voltage and Temperature



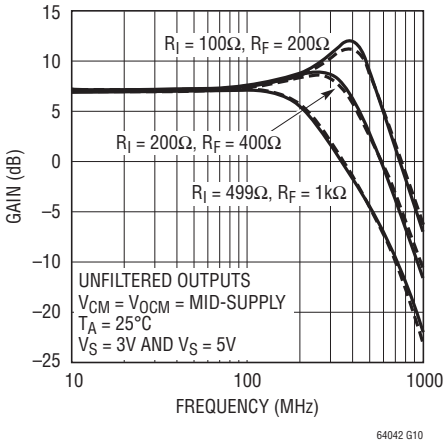
Small Signal Frequency Response



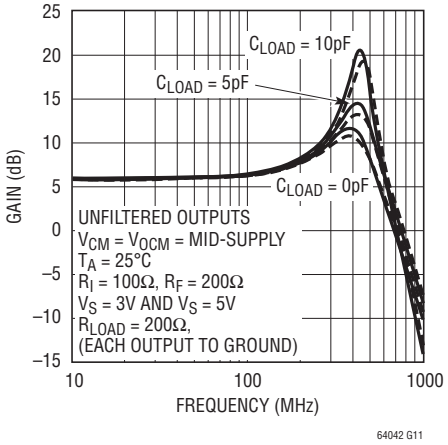
Downloaded from Elcodis.com electronic components distributor

TYPICAL PERFORMANCE CHARACTERISTICS

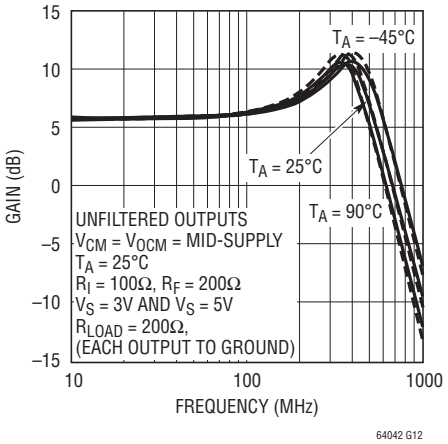
Small Signal Frequency Response vs Gain Setting Resistor Values



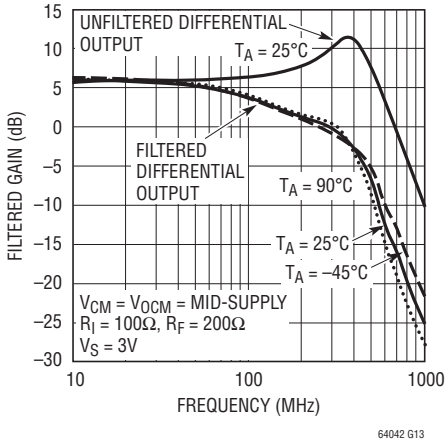
Small Signal Frequency Response vs C_{LOAD}



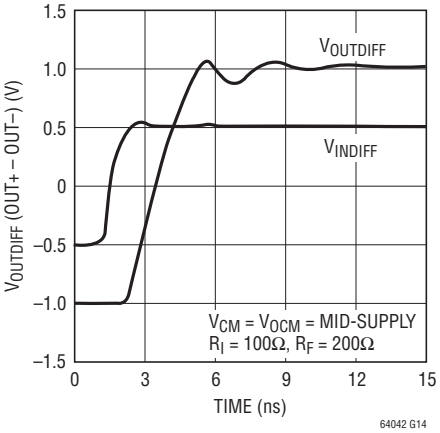
Small Signal Frequency Response vs Temperature



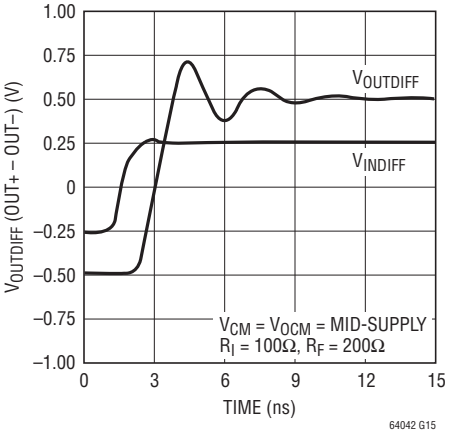
Small Signal Frequency Response vs Temperature



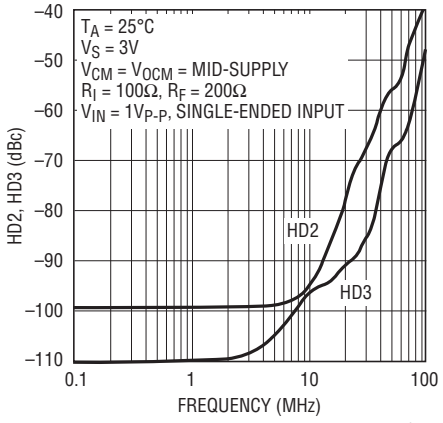
Large Signal Step Response



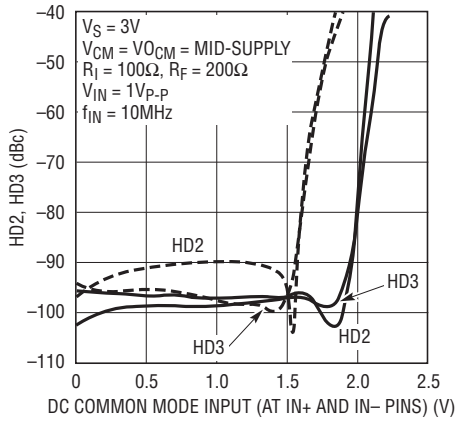
Small Signal Step Response



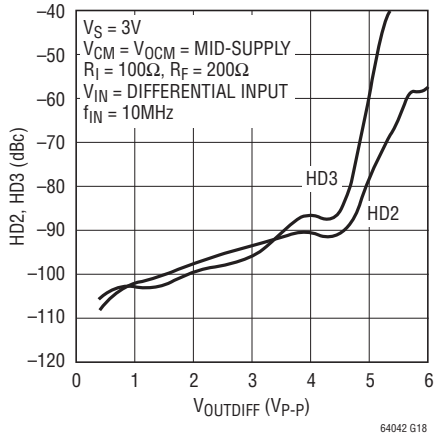
Distortion vs Frequency



Distortion vs Input Common Mode Voltage



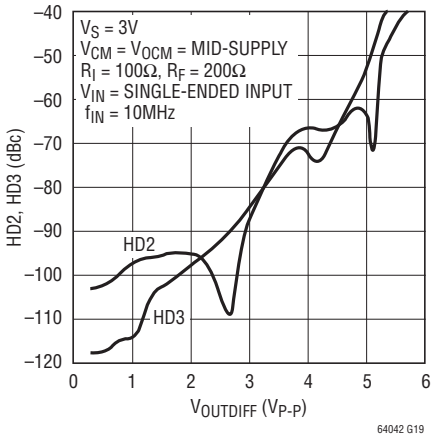
Distortion vs Output Amplitude



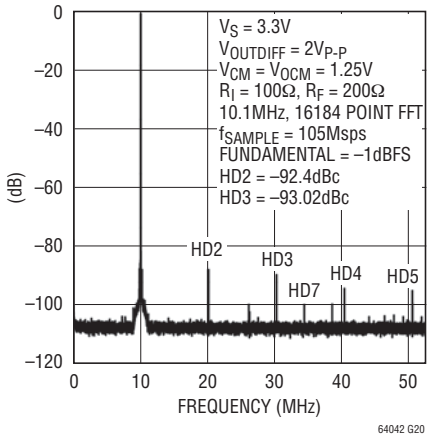
Downloaded from Elcodis.com electronic components distributor

TYPICAL PERFORMANCE CHARACTERISTICS

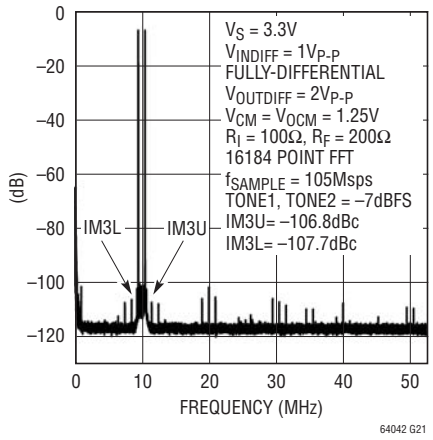
Distortion vs Output Amplitude



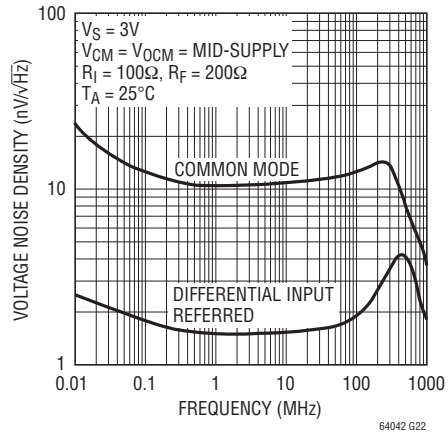
LTC6404-2 Driving LTC2207 16-Bit ADC (Single Tone)



LTC6404-2 Driving LTC2207 16-Bit ADC (Two Tones)



Voltage Noise Density vs Frequency



PIN FUNCTIONS

$\overline{\text{SHDN}}$ (Pin 1): When $\overline{\text{SHDN}}$ is floating or directly tied to V^+, the LTC6404-2 is in the normal (active) operating mode. When Pin 1 is pulled a minimum of 2.1V below V^+, the LTC6404-2 enters into a low power shutdown state. See Applications Information for more details.

V^+, V^- (Pins 2, 10, 11 and Pins 3, 9, 12): Power Supply Pins. Three pairs of power supply pins are provided to keep the power supply inductance as low as possible to prevent degradation of amplifier 2nd harmonic performance. See the Layout Considerations section for more detail.

V_{OCM} (Pin 4): Output Common Mode Reference Voltage. The voltage on the V_{OCM} pin sets the output common mode voltage level (which is defined as the average of the voltages on the OUT^+ and OUT^- pins). The V_{OCM} pin is the midpoint of an internal resistive voltage divider between the supplies, developing a (default) mid-supply voltage potential to maximize output signal swing. In general, the V_{OCM} pin can be over-driven by an external voltage source/reference capable of driving the input impedance presented by the V_{OCM} pin. On the LTC6404-2, the V_{OCM}

Downloaded from Elcodis.com electronic components distributor

PIN FUNCTIONS

pin has an input resistance of approximately 14k to a mid-supply potential. The V_{OCM} pin should be bypassed with a high quality ceramic bypass capacitor of at least 0.01µF, (with symmetrical split supplies, connect directly to a low impedance, low noise ground plane) to minimize common mode noise from being converted to differential noise by impedance mismatches both externally and internally to the IC.

NC (Pins 5, 16): No Connection. These pins are not connected internally.

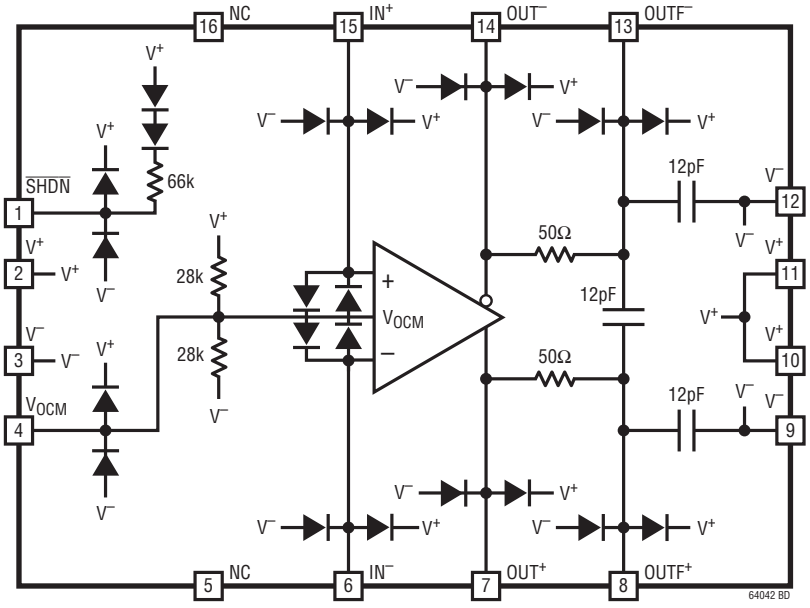
OUT⁺, OUT⁻ (Pins 7, 14): Unfiltered Output Pins. Besides driving the feedback network, each pin can drive an additional 50Ω to ground with typical short circuit current limiting of ±65mA. Each amplifier output is designed to drive a load capacitance of 10pF. This basically means the amplifier can drive 10pF from each output to ground or 5pF differentially. Larger capacitive loads should be decoupled with at least 25Ω resistors in series with each output. For long term device reliability, it is recommended that the continuous (DC + AC_{RMS}) output current be limited to under ±50mA.

OUTF⁺, OUTF⁻ (Pins 8, 13): Filtered Output Pins. These pins have a series 50Ω resistor connected between the filtered and unfiltered outputs and three 12pF capacitors. Both OUTF⁺, and OUTF⁻ have 12pF to V⁻, plus an additional 12pF differentially between OUTF⁺ and OUTF⁻. This filter creates a differential low pass frequency response with a –3dB bandwidth of 88.5MHz. For long term device reliability, it is recommended that the continuous (DC + AC_{RMS}) output current be limited to under ±40mA.

IN⁺, IN⁻ (Pins 15, 6): Non-Inverting and Inverting Input pins of the amplifier, respectively. For best performance, it is highly recommended that stray capacitance be kept to an absolute minimum by keeping printed circuit connections as short as possible, and if necessary, stripping back nearby surrounding ground plane away from these pins.

Exposed Pad (Pin 17): Tie the pad to V⁻ (Pins 3, 9, and 12). If split supplies are used, do not tie the pad to ground.

BLOCK DIAGRAM



Downloaded from Elcodis.com electronic components distributor

APPLICATIONS INFORMATION

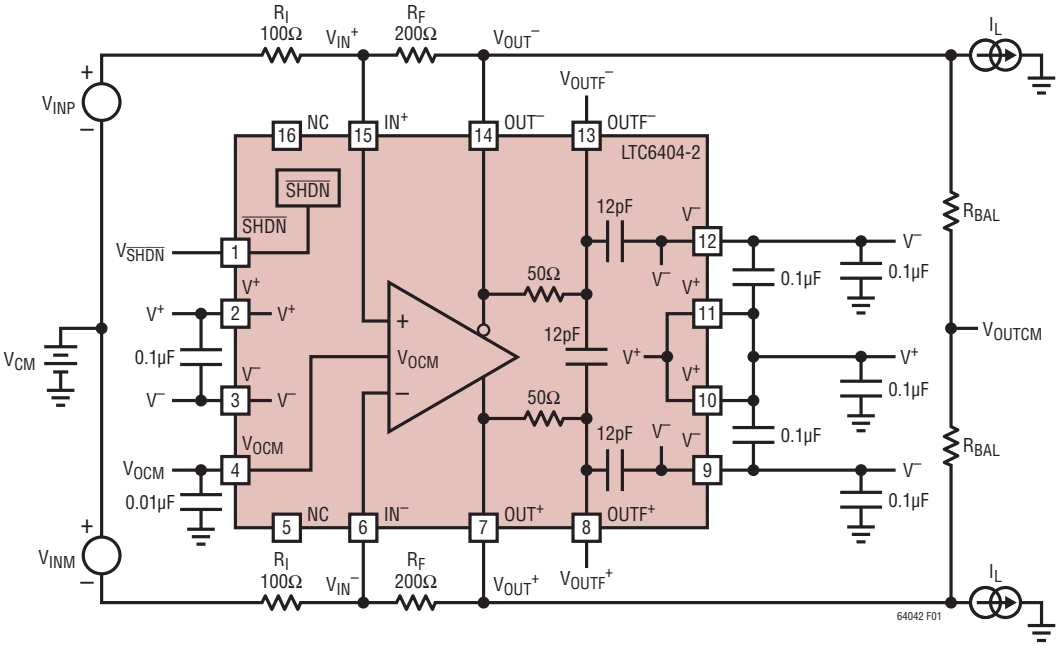


Figure 1. DC Test Circuit

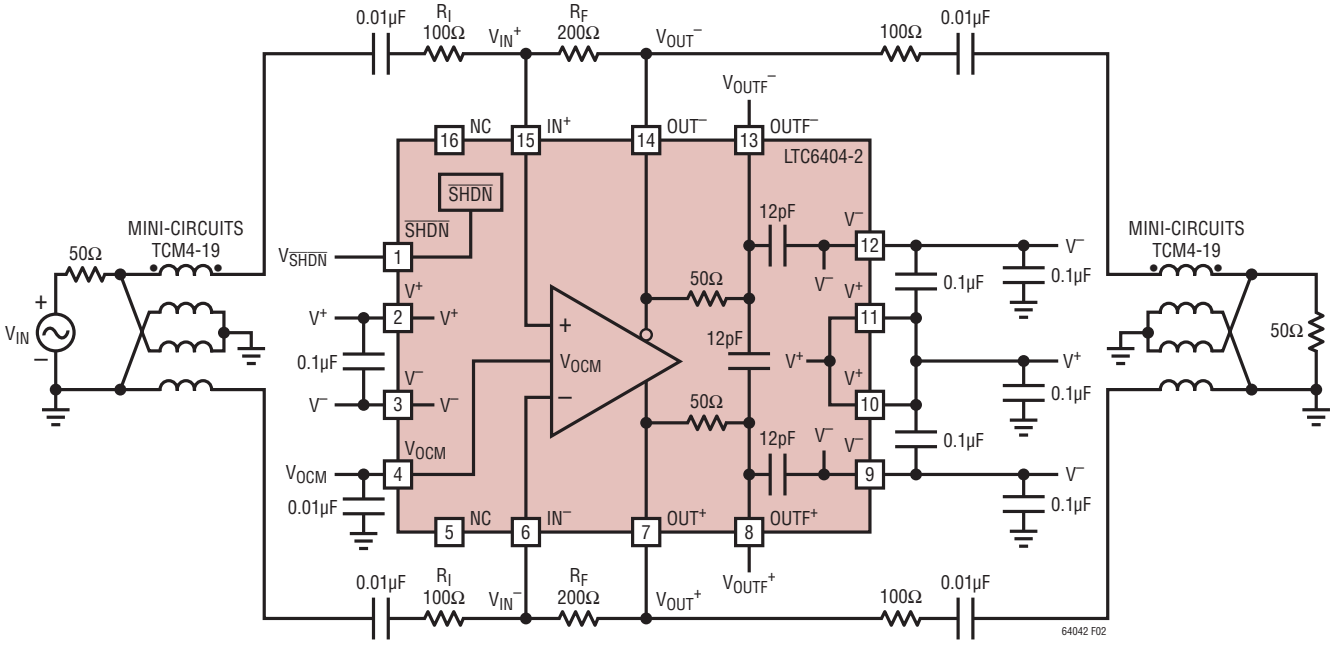


Figure 2. AC Test Circuit (–3dB BW Testing)

Downloaded from Elcodis.com electronic components distributor

APPLICATIONS INFORMATION

Functional Description

The LTC6404-2 is a small outline, wide band, low noise, and low distortion fully-differential amplifier with accurate output phase balancing. The LTC6404-2 is optimized to drive low voltage, single-supply, differential input analog-to-digital converters (ADCs). The LTC6404-2's output is capable of swinging rail-to-rail on supplies as low as 2.7V, which makes the amplifier ideal for converting ground referenced, single-ended signals into DC level shifted differential signals in preparation for driving low voltage, single-supply, differential input ADCs. Unlike traditional op amps which have a single output, the LTC6404-2 has two outputs to process signals differentially. This allows for two times the signal swing in low voltage systems when compared to single-ended output amplifiers. The balanced differential nature of the amplifier also provides even-order harmonic distortion cancellation, and less susceptibility to common mode noise (i.e. power supply noise). The LTC6404-2 can be used as a single ended input to differential output amplifier, or as a differential input to differential output amplifier.

The LTC6404-2's output common mode voltage, defined as the average of the two output voltages, is independent of the input common mode voltage, and is adjusted by applying a voltage on the V_{OCM} pin. If the pin is left open, there is an internal resistive voltage divider that develops a potential halfway between the V^+ and V^- pins. Whenever this pin is not hard tied to a low impedance ground plane, it is recommended that a high quality ceramic cap is used to bypass the V_{OCM} pin to a low impedance ground plane (See Layout Considerations). The LTC6404-2's internal common mode feedback path forces accurate output phase balancing to reduce even order harmonics, and centers each individual output about the potential set by the V_{OCM} pin.

$$V_{OUTCM} = V_{OCM} = \frac{V_{OUT}^+ + V_{OUT}^-}{2}$$

The outputs (OUT^+ and OUT^-) of the LTC6404-2 are capable of swinging rail-to-rail. They can source or sink up to approximately 65mA of current.

Additional outputs ($OUTF^+$ and $OUTF^-$) are available that provide filtered versions of the OUT^+ and OUT^- outputs. An on-chip single pole RC passive filter bandlimits the filtered outputs to a –3dB frequency of 88.5MHz. The user has a choice of using the unfiltered outputs, the filtered outputs, or modifying the filtered outputs to adjust the frequency response by adding additional components.

In applications where the full bandwidth of the LTC6404-2 is desired, the unfiltered outputs (OUT^+ and OUT^-) should be used. The unfiltered outputs OUT^+ and OUT^- are designed to drive 10pF to ground (or 5pF differentially). Capacitances greater than 10pF will produce excess peaking, and can be mitigated by placing at least 25Ω in series with the output.

Input Pin Protection

The LTC6404-2's input stage is protected against differential input voltages which exceed 1.4V by two pairs of series diodes connected in opposite directions between IN^+ and IN^- (Pins 6 and 15). In addition, the input pins have steering diodes to either power supply. If the input pair is over-driven, the current should be limited to 10mA to prevent damage to the IC. The LTC6404-2 also has steering diodes to either power supply on the V_{OCM}, and $\overline{SHDN}$ pins (Pins 4 and 1) and if forced to voltages which exceed either supply, they too, should be current limited to 10mA.

$\overline{SHDN}$ Pin

If the $\overline{SHDN}$ pin (Pin 1) is pulled 2.1V below the positive supply, circuitry is activated which powers down the LTC6404-2. The pin will have the Thevenin equivalent impedance of approximately 66kΩ to V^+. If the pin is left unconnected, an internal pull-up resistor of 150k will keep the part in normal active operation. Care should be taken to control leakage currents at this pin to under 1µA to prevent inadvertently putting the LTC6404-2 into shutdown. In shutdown, all biasing current sources are shut off, and the output pins, OUT^+ and OUT^-, will each

Downloaded from Elcodis.com electronic components distributor

APPLICATIONS INFORMATION

appear as open collectors with a non-linear capacitor in parallel and steering diodes to either supply. Because of the non-linear capacitance, the outputs still have the ability to sink and source small amounts of transient current if driven by significant voltage transients. The inputs (IN^+, and IN^-) appear as anti-parallel diodes which can conduct if voltage transients at the input exceed 1.4V. The inputs also have steering diodes to either supply. The turn-on and turn-off time between the shutdown and active states is typically less than 1µs.

General Amplifier Applications

As levels of integration have increased and correspondingly, system supply voltages decreased, there has been a need for ADCs to process signals differentially in order to maintain good signal to noise ratios. These ADCs are typically supplied from a single supply voltage which can be as low as 3V (2.7V min), and will have an optimal common mode input range near mid-supply. The LTC6404-2 makes interfacing to these ADCs easy by providing both single ended to differential conversion as well as common mode level shifting. The front page of this datasheet shows shows a typical application.

Referring to Figure 1, the gain to $V_{OUTDIFF}$ from V_{INM} and V_{INP} is:

$$V_{OUTDIFF} = V_{OUT}^+ - V_{OUT}^- \approx \frac{R_F}{R_I} \bullet (V_{INP} - V_{INM})$$

Note from the above equation, the differential output voltage ($VOUT^+ – VOUT^–$) is completely independent of input and output common mode voltages, or the voltage at the common mode pin. This makes the LTC6404-2 ideally suited for pre-amplification, level shifting and conversion of single ended signals to differential output signals to drive differential input ADCs.

Effects of Resistor Pair Mismatch

In the circuit of Figure 3, it is possible the gain setting resistors will not perfectly match. Assuming infinite open loop gain, the differential output relationship is given by the equation:

$$V_{OUTDIFF} = V_{OUT}^+ - V_{OUT}^- \cong \frac{R_F}{R_I} \bullet V_{INDIFF} + \frac{\Delta\beta}{\beta_{AVG}} \bullet V_{INCM} - \frac{\Delta\beta}{\beta_{AVG}} \bullet V_{OCM}$$

where:

R_F is the average of R_{F1}, and R_{F2}, and R_I is the average of R_{I1}, and R_{I2}.

β_{AVG} is defined as the average feedback factor (or gain) from the outputs to their respective inputs:

$$\beta_{AVG} = \frac{1}{2} \bullet \left(\frac{R_{I1}}{R_{I1} + R_{F1}} + \frac{R_{I2}}{R_{I2} + R_{F2}} \right)$$

$\Delta\beta$ is defined as the difference in feedback factors:

$$\Delta\beta = \frac{R_{I2}}{R_{I2} + R_{F2}} - \frac{R_{I1}}{R_{I1} + R_{F1}}$$

V_{INCM} is defined as the average of the two input voltages V_{INP} and V_{INM} (also called the source-referred input common mode voltage):

$$V_{INCM} = \frac{1}{2} \bullet (V_{INP} + V_{INM})$$

and V_{INDIFF} is defined as the difference of the input voltages:

$$V_{INDIFF} = V_{INP} - V_{INM}$$

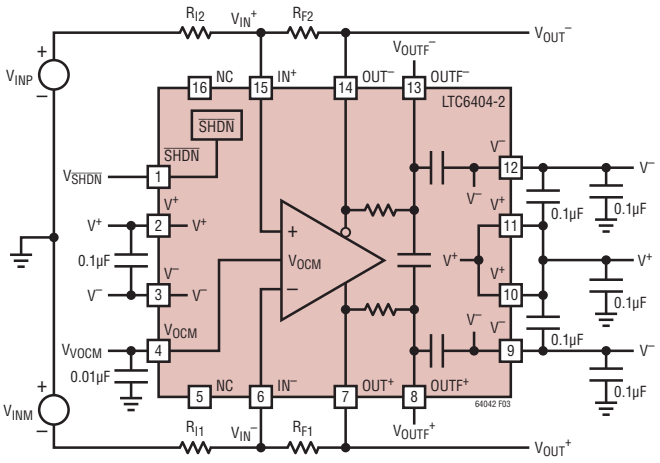


Figure 3. Basic Differential Amplifier with Feedback Resistor Pair Mismatch

Downloaded from Elcodis.com electronic components distributor

APPLICATIONS INFORMATION

When the feedback ratios mismatch ($\Delta\beta$), common mode to differential conversion occurs.

Setting the differential input to zero (V_{INDIFF} = 0), the degree of common mode to differential conversion is given by the equation:

$$V_{OUTDIFF} = V_{OUT}^{+} - V_{OUT}^{-}$$

$$\approx \left(V_{INCM} - V_{OCM}\right) \bullet \frac{\Delta\beta}{\beta_{AVG}} \Bigg|_{V_{INDIFF}=0}$$

In general, the degree of feedback pair mismatch is a source of common mode to differential conversion of both signals and noise. Using 1% resistors or better will mitigate most problems, and will provide about 41dB worst case of common mode rejection. Using 0.1% resistors will provide about 61dB of common mode rejection. A low impedance ground plane should be used as a reference for both the input signal source, and the V_{OCM} pin. A direct short of V_{OCM} to this ground or bypassing the V_{OCM} with a high quality 0.1µF ceramic capacitor to this ground plane, will further prevent common mode signals from being converted to differential.

There may be concern on how feedback ratio mismatch affects distortion. Distortion caused by feedback ratio mismatch using 1% resistors or better is negligible. However, in single supply level shifting applications where there is a voltage difference between the input common mode voltage and the output common mode voltage, resistor mismatch can make the apparent voltage offset of the amplifier appear higher than specified.

The apparent input referred offset induced by feedback ratio mismatch is derived from the following equation:

$$V_{OSDIFF(APPARENT)} \approx (V_{ICM} - V_{OCM}) \bullet \Delta\beta$$

Using the LTC6404-2 in a single supply application on a single 5V supply with 1% resistors, and the input common mode grounded, with the V_{OCM} pin biased at mid-supply, the worst case resistor mismatch can induce 22mV of apparent offset voltage. With 0.1% resistors, the worst case apparent offset reduces to 2.2mV.

Input Impedance and Loading Effects

The input impedance looking into the V_{INP} or V_{INM} input of Figure 1 depends on whether the sources V_{INP} and V_{INM} are fully differential. For balanced input sources (V_{INP} = $-V_{INM}$), the input impedance seen at either input is simply:

$$R_{INP} = R_{INM} = R_I$$

For single ended inputs, because of the signal imbalance at the input, the input impedance increases over the balanced differential case. The input impedance looking into either input is:

$$R_{INP} = R_{INM} = \frac{R_I}{\left(1 - \frac{1}{2} \bullet \left(\frac{R_F}{R_I + R_F}\right)\right)}$$

Input signal sources with non-zero output impedances can also cause feedback imbalance between the pair of feedback networks. For the best performance, it is recommended that the source's output impedance be compensated for. If input impedance matching is required by the source, R1 should be chosen (see Figure 4):

$$R1 = \frac{R_{INM} \bullet R_S}{R_{INM} - R_S}$$

According to Figure 4, the input impedance looking into the differential amp (R_{INM}) reflects the single ended source case, thus:

$$R_{INM} = \frac{R_I}{\left(1 - \frac{1}{2} \bullet \left(\frac{R_F}{R_I + R_F}\right)\right)}$$

R2 is chosen to balance R1 || R_S:

$$R2 = \frac{R_I \bullet R_S}{R_I + R_S}$$

Downloaded from Elcodis.com electronic components distributor

APPLICATIONS INFORMATION

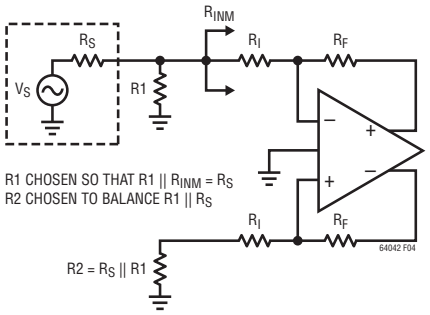


Figure 4. Optimal Compensation for Signal Source Impedance

Input Common Mode Voltage Range

The LTC6404-2's input common mode voltage (V_{ICM}) is defined as the average of the two input voltages, V_{IN}^+, and V_{IN}^-. It extends from V^- to 1.4V below V^+. The operating input common mode range depends on the circuit configuration (gain), V_{OCM} and V_{CM} (Refer to Figure 5). For fully differential input applications, where $V_{INP} = -V_{INM}$, the common mode input voltage is approximately:

$$V_{ICM} = \frac{V_{IN}^+ + V_{IN}^-}{2} \approx V_{OCM} \bullet \left(\frac{R_I}{R_I + R_F}\right) + V_{CM} \bullet \left(\frac{R_F}{R_F + R_I}\right)$$

With singled ended inputs, there is an input signal component to the input common mode voltage. Applying only

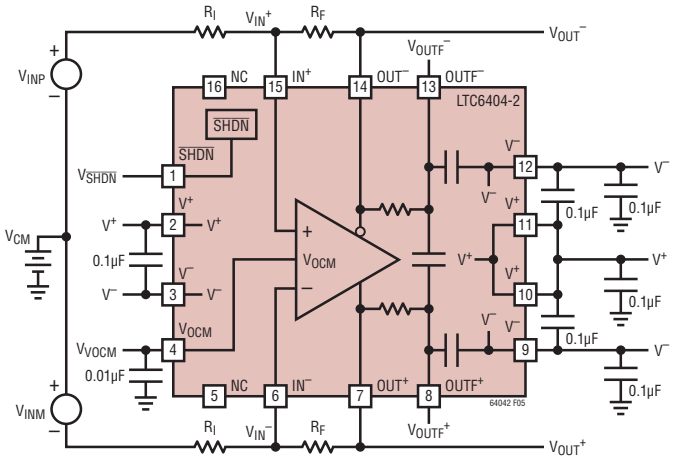


Figure 5. Circuit for Common Mode Range

V_{INP} (setting V_{INM} to zero), the input common voltage is approximately:

$$V_{ICM} = \frac{V_{IN}^+ + V_{IN}^-}{2} \approx V_{OCM} \bullet \left(\frac{R_I}{R_I + R_F}\right) + V_{CM} \bullet \left(\frac{R_F}{R_F + R_I}\right) + \frac{V_{INP}}{2} \bullet \left(\frac{R_F}{R_F + R_I}\right)$$

Output Common Mode Voltage Range

The output common mode voltage is defined as the average of the two outputs:

$$V_{OUTCM} = V_{OCM} = \frac{V_{OUT}^+ + V_{OUT}^-}{2}$$

The V_{OCM} pin sets this average by an internal common mode feedback loop which internally forces $V_{OUT}^+ = -V_{OUT}^-$. The output common mode range extends from 1.1V above V^- to 1V below V^+. The V_{OCM} pin sits in the middle of a voltage divider which sets the default mid-supply open circuit potential.

In single supply applications, where the LTC6404-2 is used to interface to an ADC, the optimal common mode input range to the ADC is often determined by the ADC's reference. If the ADC makes a reference available for setting the input common mode voltage, it can be directly tied to the V_{OCM} pin, but must be capable of driving the input impedance presented by the V_{OCM} as listed in the Electrical Characteristics Table. This impedance can be assumed to be connected to a mid-supply potential. If an external reference drives the V_{OCM} pin, it should still be bypassed with a high quality 0.01µF or larger capacitor to a low impedance ground plane to filter any thermal noise and to prevent common mode signals on this pin from being inadvertently converted to differential signals.

Output Filter Considerations and Use

Filtering at the output of the LTC6404-2 is often desired to provide either anti-aliasing or improved signal to noise ratio. To simplify this filtering, the LTC6404-2 includes an additional pair of differential outputs ($OUTF^+$ and $OUTF^-$)

Downloaded from Elcodis.com electronic components distributor

APPLICATIONS INFORMATION

which incorporate an internal lowpass filter network with a –3dB bandwidth of 88.5MHz (Figure 6).

These pins each have a DC output impedance of 50Ω. Internal capacitances are 12pF to V^- on each filtered output, plus an additional 12pF capacitor connected differentially between the two filtered outputs. This resistor/capacitor combination creates filtered outputs that look like a series 50Ω resistor with a 36pF capacitor shunting each filtered output to AC ground, providing a –3dB bandwidth of 88.5MHz, and a noise bandwidth of 139MHz. The filter cutoff frequency is easily modified with just a few external components. To increase the cutoff frequency, simply add 2 equal value resistors, one between OUT^+ and $OUTF^+$ and the other between OUT^- and $OUTF^-$ (Figure 7). These resistors, in parallel with the internal 50Ω resistor, lower the overall resistance and therefore increase filter bandwidth. For example, to double the filter bandwidth, add two external 50Ω resistors to lower the series filter resistance to 25Ω. The 36pF of capacitance remains unchanged, so filter bandwidth doubles. Keep in mind, the series resistance also serves to decouple the outputs from load capacitance including the onboard filter capacitors. The unfiltered outputs of the LTC6404-2 are designed to drive 10pF to ground or 5pF differentially, so care should be taken to not lower the effective impedance between OUT^+ and $OUTF^+$ or OUT^- and $OUTF^-$ below 25Ω.

To decrease filter bandwidth, add two external capacitors, one from $OUTF^+$ to ground, and the other from $OUTF^-$ to ground. A single differential capacitor connected between $OUTF^+$ and $OUTF^-$ can also be used, but since it is being driven differentially it will appear at each filtered output as a single-ended capacitance of twice the value. To halve the filter bandwidth, for example, two 36pF capacitors could be added (one from each filtered output to ground). Alternatively, one 18pF capacitor could be added between the filtered outputs, again halving the filter bandwidth. Combinations of capacitors could be used as well; a three capacitor solution of 12pF from each filtered output to ground plus a 12pF capacitor between the filtered outputs would also halve the filter bandwidth (Figure 8).

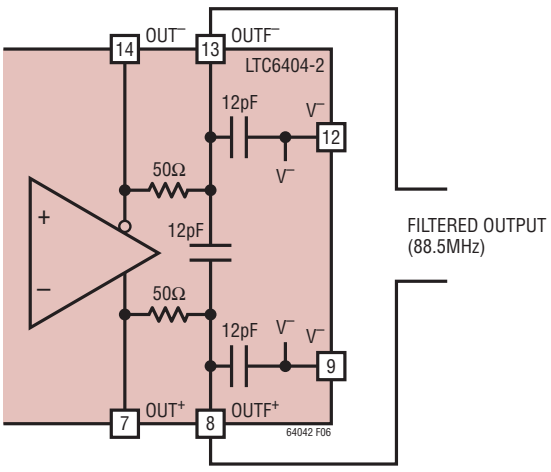


Figure 6. LTC6404-2 Internal Filter Topology

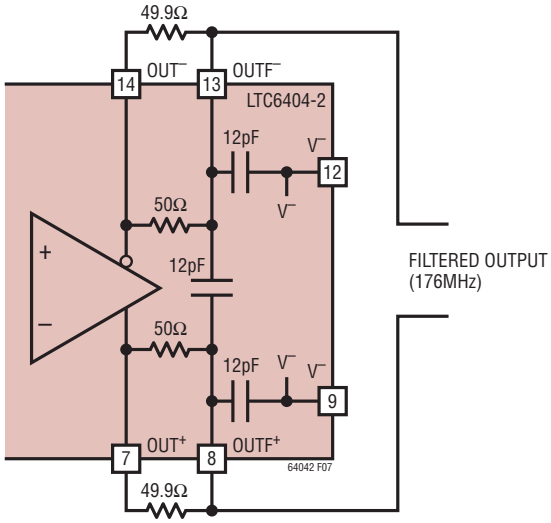


Figure 7. LTC6404-2 Filter Topology Modified for 2x Filter Bandwidth (2 External Resistors)

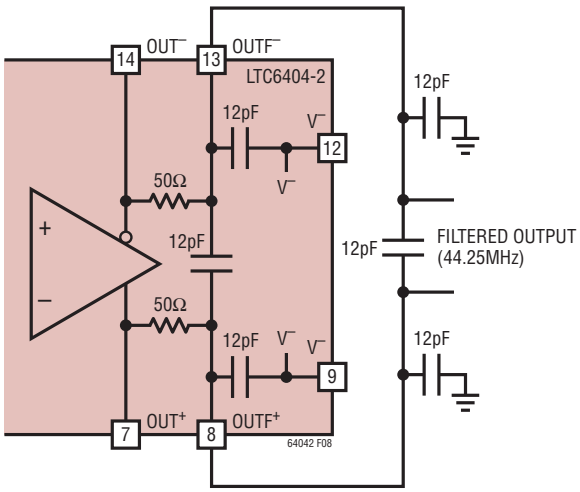


Figure 8. LTC6404-2 Filter Topology Modified for 1/2x Filter Bandwidth (3 External Capacitors)

Downloaded from Elcodis.com electronic components distributor

APPLICATIONS INFORMATION

Noise Considerations

The LTC6404-2's input referred voltage noise is on the order of 1.5nV/√Hz. Its input referred current noise is on the order of 3pA/√Hz. In addition to the noise generated by the amplifier, the feedback resistors also contribute noise. A noise model is shown in Figure 9. The output noise generated by both the amplifier and the feedback components is governed by the equation:

$$e_{no} = \sqrt{\left(e_{ni} \bullet \left(1+\frac{R_F}{R_I}\right)\right)^2 + 2 \bullet \left(I_n \bullet R_F\right)^2 + 2 \bullet \left(e_{nRI} \bullet \left(\frac{R_F}{R_I}\right)\right)^2 + 2 \bullet e_{nRF}{}^2}$$

A plot of this equation, and a plot of the noise generated by the feedback components for the LTC6404-2 is shown in Figure 10.

The LTC6404-2's input referred voltage noise contributes the equivalent noise of a 140Ω resistor. When the feedback network is comprised of resistors whose values are less than this, the LTC6404-2's output noise is voltage noise dominant (See Figure 10.):

$$e_{no} \approx e_{ni} \bullet \left(1+\frac{R_F}{R_I}\right)$$

Feedback networks with R_F values greater than about 400Ω will result in output noise which is resistor noise and amplifier current noise dominant.

$$e_{no} \approx \sqrt{2} \bullet \sqrt{\left(I_n \bullet R_F\right)^2 + \left(1+\frac{R_F}{R_I}\right) \bullet 4 \bullet k \bullet T \bullet R_F}$$

Lower R_F resistor values (<200Ω) always result in lower noise at the penalty of increased distortion due to increased loading of the feedback network on the output. Higher

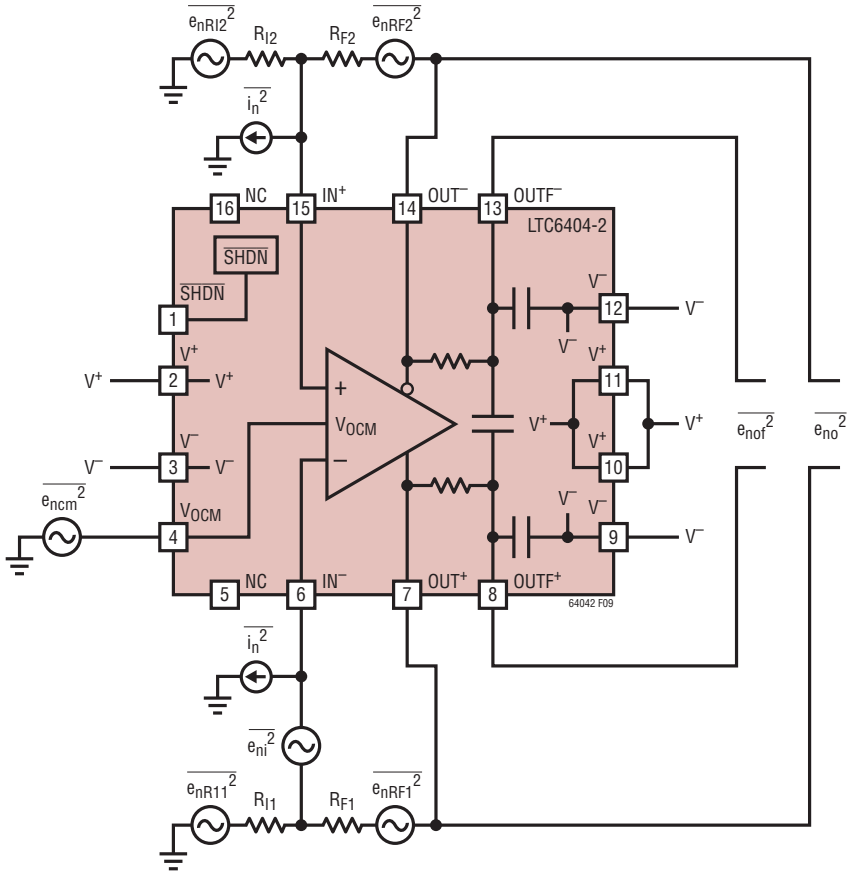


Figure 9. Noise Model of the LTC6404-2

Downloaded from Elcodis.com electronic components distributor

APPLICATIONS INFORMATION

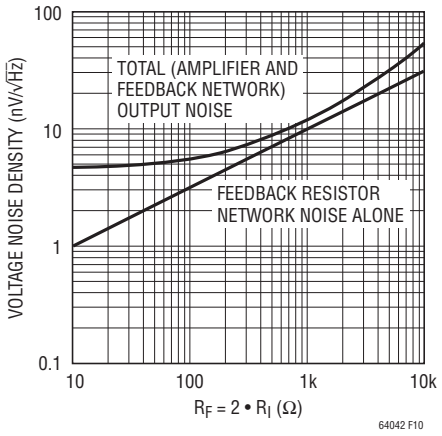


Figure 10. LTC6404-2 Output Spot Noise vs Spot Noise Contributed by Feedback Network Alone

R_F resistor values (but still less than 400Ω) will result in higher output noise, but improved distortion due to less loading on the output. The optimal feedback resistance for the LTC6404-2 is between R_F = 200Ω to 400Ω.

The differential filtered outputs $OUTF^+$ and $OUTF^-$ will have a little higher spot noise than the unfiltered outputs (due to the two 50Ω resistors which contribute 0.9nV/$\sqrt{Hz}$ each), but actually will provide superior Signal-to-Noise in noise bandwidths exceeding 139MHz due to the noise-filtering function the filter provides.

Layout Considerations

Because the LTC6404-2 is a very high speed amplifier, it is sensitive to both stray capacitance and stray inductance. Three pairs of power supply pins are provided to keep the power supply inductance as low as possible to prevent degradation of amplifier 2nd Harmonic performance. It is critical that close attention be paid to supply bypassing. For single supply applications (Pins 3, 9 and 12 grounded) it is recommended that 3 high quality 0.1µF surface mount ceramic bypass capacitors be placed between pins 2 and 3, between pins 11and 12, and between pins10 and 9 with direct short connections. Pins 3, 9 and 10 should be tied directly to a low impedance ground plane with minimal routing. For dual (split) power supplies, it is recommended that at least two additional high quality, 0.1µF ceramic capacitors are used to bypass pin V^+ to ground and V^- to ground, again with minimal routing. For driving large loads (<200Ω), additional bypass capacitance may be needed for optimal performance. Keep in mind that small geometry (e.g. 0603) surface mount ceramic capacitors have a much higher self resonant frequency than do leaded capacitors, and perform best in high speed applications.

Any stray parasitic capacitances to ground at the summing junctions IN^+, and IN^- should be kept to an absolute minimum even if it means stripping back the ground plane away from any trace attached to this node. This becomes especially true when the feedback resistor network uses resistor values >400Ω in circuits with $R_F = 2 \bullet R_I$. Excessive peaking in the frequency response can be mitigated by adding small amounts of feedback capacitance (~1pF) around R_F. Always keep in mind the differential nature of the LTC6404-2, and that it is critical that the load impedances seen by both outputs (stray or intended) should be as balanced and symmetric as possible. This will help preserve the natural balance of the LTC6404-2, which minimizes the generation of even order harmonics, and preserves the rejection of common mode signals and noise.

It is highly recommended that the V_{OCM} pin be either hard tied to a low impedance ground plane (in split supply applications), or bypassed to ground with a high quality ceramic capacitor whose value exceeds 0.01µF. This will help stabilize the common mode feedback loop as well as prevent thermal noise from the internal voltage divider and other external sources of noise from being converted to differential noise due to divider mismatches in the feedback networks. It is also recommended that the resistive feedback networks be comprised of 1% resistors (or better) to enhance the output common mode rejection. This will also prevent V_{OCM} referred common mode noise of the common mode amplifier path (which cannot be filtered) from being converted to differential noise, degrading the differential noise performance.

Feedback factor mismatch has a weak effect on distortion. Using 1% or better resistors should prevent mismatch from impacting amplifier linearity. However, in single supply level shifting applications where there is a voltage difference between the input common mode voltage and the output common mode voltage, resistor mismatch can

Downloaded from Elcodis.com electronic components distributor

APPLICATIONS INFORMATION

make the apparent voltage offset of the amplifier appear worse than specified.

In general, the apparent input referred offset induced by feedback factor mismatch is given by the equation:

$$V_{OSDIFF(APPARENT)} \approx (V_{INCM} - V_{OCM}) \bullet \Delta\beta$$

where

$$\Delta\beta = \frac{R_{I2}}{R_{I2} + R_{F2}} - \frac{R_{I1}}{R_{I1} + R_{F1}}$$

Interfacing the LTC6404-2 to A/D Converters

The LTC6404-2's rail-to-rail output and fast settling time make the LTC6404-2 ideal for interfacing to low voltage, single supply, differential input ADCs. The sampling process of ADCs create a sampling glitch caused by switching in the sampling capacitor on the ADC front end which momentarily "shorts" the output of the amplifier as charge is transferred between the amplifier and the sampling cap. The amplifier must recover and settle from this load transient before this acquisition period ends for a valid representation of the input signal. In general, the LTC6404-2 will settle much more quickly from these periodic load impulses than from a 2V input step, but it is a good idea to either use the filtered outputs to drive the ADC (Figure 11 shows an example of this), or to place a discrete R-C filter network between the differential unfiltered outputs of the LTC6404-2 and the input of the ADC to help absorb the charge transfer required during the ADC sampling process. The capacitance of the filter network serves as a charge reservoir to provide high frequency charging during the sampling process, while the two resistors of the filter network are used to dampen and attenuate any charge kickback from the ADC. The selection of the R-C time constant is trial and error for a given ADC, but the following guidelines are recommended: Choosing too large of a resistor in the decoupling network (leaving insufficient settling time) will create a voltage divider between the dynamic input impedance of the ADC and the decoupling resistors. Choosing too small of a resistor will possibly prevent the resistor from properly damping the load transient caused by the sampling process, prolonging the time required for settling. 16-bit applications typically require a minimum of 11 R-C time constants. It is recommended that the capacitor chosen have a high quality dielectric (for example, C0G multilayer ceramic).

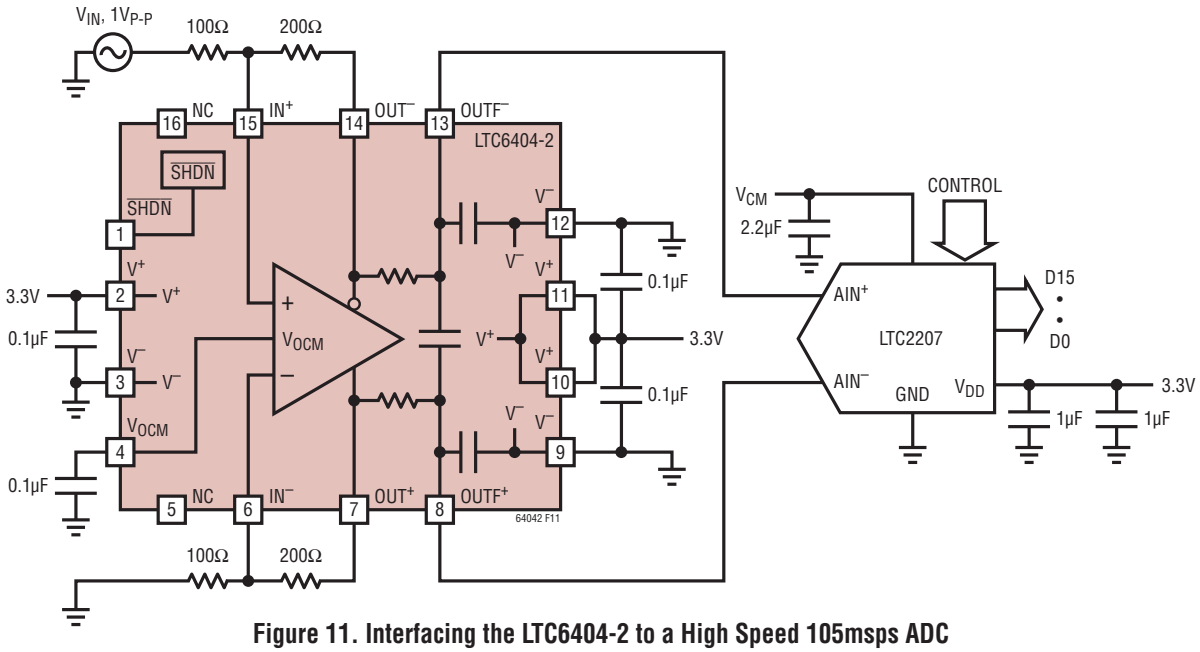
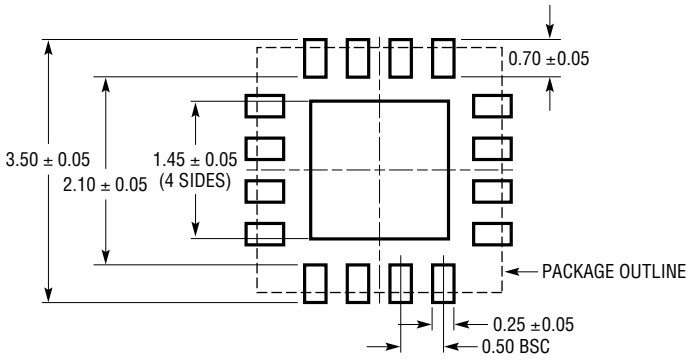


Figure 11. Interfacing the LTC6404-2 to a High Speed 105msps ADC

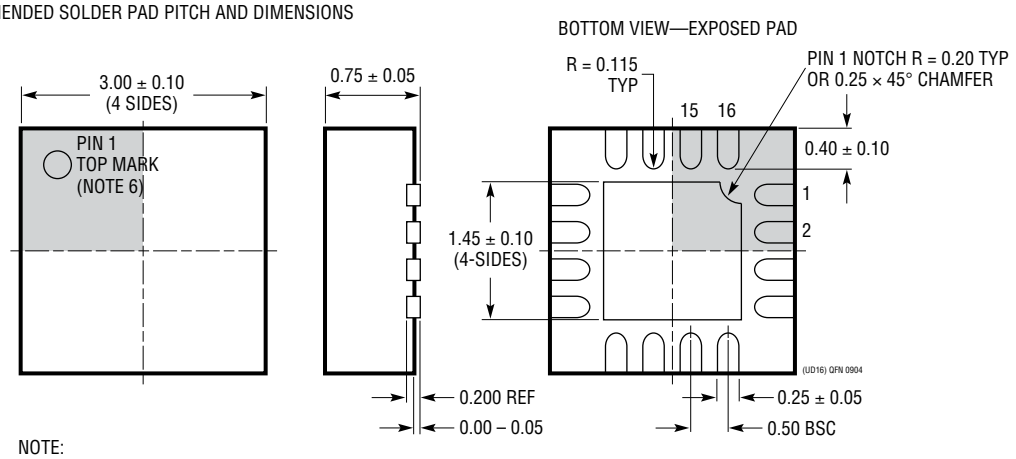
Downloaded from Elcodis.com electronic components distributor

PACKAGE DESCRIPTION

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1691)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

Downloaded from Elcodis.com electronic components distributor

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1809/LT1810	Single/Dual 180MHz, 350V/µs Rail-to-Rail Input and Output Low Distortion Op Amps	180MHz, 350V/µs Slew Rate, Shutdown
LTC1992/LTC1992-x	Fully Differential Input/Output Amplifiers	Programmable Gain or Fixed Gain (G = 1, 2, 5, 10)
LT1994	Low Noise, Low Distortion Fully differential Input/Output Amplifier/Driver	Low Distortion, $2V_{P-P}$, 1MHz: –94dBc, 13mA, Low Noise: $3nV/\sqrt{Hz}$
LTC6400-20	1.8GHz Low Noise, Low Distortion ADC Driver for up to 300MHz	A_V = 20dB, Z_{IN} = 200Ω, $I_{S(MAX)}$ = 105mA at 25°C
LTC6401-20	1.4GHz Low Noise, Low Distortion ADC Driver	A_V = 20dB, Z_{IN} = 200Ω, $I_{S(MAX)}$ = 62mA at 25°C
LTC6402-12	300MHz Low Distortion, Low Noise Differential Amplifier/ADC Driver	A_V = 12V/V, NF = 15dB, OIP3 = 43dBm at 20MHz
LTC6404-1	600MHz Low Noise Rail-to-Rail Output Differential ADC Driver	Unity Gain Stable
LTC6406	3GHz Low Noise, Rail-to-Rail Input Differential ADC Driver	$e_n = 1.6nV/\sqrt{Hz}$, I_S=18mA
LT6600-2.5	Very Low Noise, Fully Differential Amplifier and 2.5MHz Filter	86dB S/N with 3V Supply, SO-8 Package
LT6600-5	Very Low Noise, Fully Differential Amplifier and 5MHz Filter	82dB S/N with 3V Supply, SO-8 Package
LT6600-10	Very Low Noise, Fully Differential Amplifier and 10MHz Filter	82dB S/N with 3V Supply, SO-8 Package
LT6600-20	Very Low Noise, Fully Differential Amplifier and 20MHz Filter	76dB S/N with 3V Supply, SO-8 Package

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
LT 0208 • PRINTED IN USA
© LINEAR TECHNOLOGY CORPORATION 2008

Downloaded from Elcodis.com electronic components distributor