*Product Preview*

## System Basis Chip Lite with Low Speed Fault Tolerant CAN Interface

The MC33889 is a monolithic integrated circuit combining many functions frequently used by automotive ECUs. It incorporates a low speed fault tolerant CAN physical interface.

Main features:
- Vdd1: 5V Low drop voltage regulator, current limitation, over temperature detection, monitoring and reset function. Total current capability 200mA.
- V2: Tracking function of Vdd1 regulator. Control circuitry for external bipolar ballast transistor for high flexibility in choice of peripheral voltage and current supply.
- Four operational modes: normal, stand-by, stop and sleep modes.
- Low stand-by current consumption in stop and sleep modes
- Built in Low speed 125KBaud fault tolerant CAN physical interface, compatible with Motorola MC33388.
- External high voltage wake-up input, associated with HS1 Vbat switch
- 150mA output current capability for HS1 Vbat switch allowing drive of external switches pull up resistors or relays
- Vsup monitoring and failure detection
- DC Operating voltage from 5 to 27V
- 40V maximum transient voltage
- Programmable software time out and window watchdog
- Separate outputs for Watchdog time out signal (WDOGB) and Reset (Reset).
- Wake up capabilities: wake up input, programmable cyclic sense, forced wake up, CAN interface, SPI (CSB pin) and stop mode over current.
- Interface with MCU through 4 Mhz SPI.
- SO28WB package with thermal enhanced lead frame.

### PC33889
PASS3

### System Basis Chip Lite

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



**DW SUFFIX**
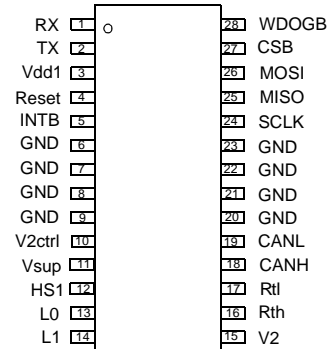PLASTIC PACKAGE
CASE 751F
SO-28

### PIN CONNECTIONS

| | | | |
|---|---|---|---|
| RX | 1 | 28 | WDOGB |
| TX | 2 | 27 | CSB |
| Vdd1 | 3 | 26 | MOSI |
| Reset | 4 | 25 | MISO |
| INTB | 5 | 24 | SCLK |
| GND | 6 | 23 | GND |
| GND | 7 | 22 | GND |
| GND | 8 | 21 | GND |
| GND | 9 | 20 | GND |
| V2ctrl | 10 | 19 | CANL |
| Vsup | 11 | 18 | CANH |
| HS1 | 12 | 17 | Rtl |
| L0 | 13 | 16 | Rth |
| L1 | 14 | 15 | V2 |

**Simplified Block Diagram**
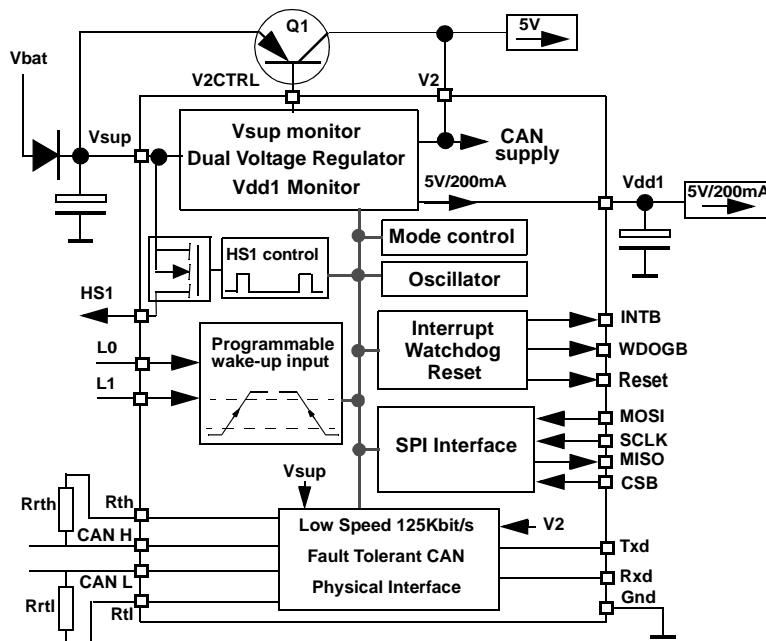


### ORDERING INFORMATION

| Device | Operating Temperature Range | Package |
|---|---|---|
| PC33889DW | T$_A$ = -40 to 125°C | SO-28 |

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## 1    MAXIMUM RATINGS

| Ratings | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **ELECTRICAL RATINGS** | | | | | |
| Supply Voltage at Vsup<br>- Continuous voltage<br>- Transient voltage (Load dump) | Vsup<br>Vsup | -0.3 | | 27<br>40 | V |
| Logic Inputs (Rx, Tx, MOSI, MISO, CSB, SCLK, Reset, WDOGB, INTB) | Vlog | - 0.3 | | Vdd1+0.3 | V |
| Output current Vdd1 | I | | Internally limited | | A |
| HS1<br>- voltage<br>- output current | V<br>I | -0.2 | Internally limited | Vsup+0.3 | V<br>A |
| ESD voltage (HBM 100pF, 1.5k)<br>- CANL, CANH, Rtl, Rth, HS1, L0, L1<br>- All other pins | Vesdh | -4<br>-2 | | 4<br>2 | kV |
| ESD voltage (Machine Model) All pins | Vesdm | -200 | | 200 | V |
| L0, L1<br>- DC Input voltage<br>- DC Input current<br>- Transient input current (according to ISO7637 specification) and with external component tbd. | Vwu DC | -0.3<br>-2<br>tbd | | 40<br>2<br>tbd | V<br>mA<br>mA |
| CAN related pins: CANH, CANL, RTL, RTH, Tx, Rx (refer to CAN section) | | | | | |
| **THERMAL RATINGS** | | | | | |
| Junction Temperature | $T_j$ | - 40 | | +150 | °C |
| Storage Temperature | $T_s$ | - 55 | | +165 | °C |
| Ambient Temperature (for info only) | $T_a$ | - 40 | | +125 | °C |
| Thermal resistance junction to gnd pin (note 1) | Rthj/p | | | 20 | °C/W |

Note 1: gnd pins 6,7,8,9,20, 21, 22, 23.

**Figure 1. Transient test pulse for L0 and L1 inputs**
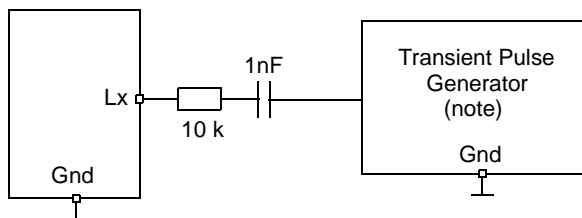


note: Waveform in accordance to ISO7637 part1, test pulses 1, 2, 3a and 3b.

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## 2 ELECTRICAL CHARACTERISTICS

($V_{sup}$ From 5.5V to 18V and $T_j$ from -40°C to 125°C) unless otherwise noted. For all pins except can related pins

| Description | Symbol | Characteristics | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| **Vsup pin (Device power supply)** | | | | | | |
| Nominal DC Voltage range | Vsup | 5.5 | | 18 | V | |
| Extended DC Voltage range 1 | Vsup-ex1 | 4.5 | | 5.5 | V | Reduced functionality (note 1) |
| Extended DC Voltage range 2 | Vsup-ex2 | 18 | | 27 | V | (note 3) |
| Input Voltage during Load Dump | VsupLD | | | 40 | V | Load dump situation |
| Input Voltage during jump start | VsupJS | | | 27 | V | Jump start situation |
| Supply Current in Sleep Mode (note 2,4) | Isup (sleep1) | | 75 | tbd | uA | Vdd1 & V2 off, Vsup<12V, oscillator running (note 5) excluding CAN current |
| Supply Current in Sleep Mode (note 2,4) | Isup (sleep2) | | 60 | tdb | uA | Vdd1 & V2 off, Vsup<12V oscillator not running (note5) excluding CAN current, |
| Supply current in sleep mode (note 2,4) | Isup (sleep3) | | 150 | tbd | uA | Vdd1 & V2 off, Vsup>12V oscillator running (note 5) excluding CAN current |
| Supply Current in Stand-by Mode (note 2,4) | Isup(stdby) | | | 15 | mA | Iout at Vdd1 =10mA, CAN recessive state or disabled |
| Supply Current in Normal Mode (note 2) | Isup(norm) | | | 15 | mA | Iout at Vdd1 =10mA, CAN recessive state or disabled |
| Supply Current in Stop mode (note 2,4) I out Vdd1 <2mA | Isup (stop1) | | 120 | tbd | uA | Vdd1 on (note 6), Vsup<12V oscillator running (note 5) excluding CAN current, |
| Supply Current in Stop mode (note 2,4) Iout Vdd1 < 2mA | Isup (stop2) | | 110 | tbd | uA | Vdd1 on (note 6), Vsup<12V oscillator not running (note 5) excluding CAN current |
| Supply Current in Stop mode (note 2,4) Iout Vdd1 < 2mA | Isup (stop3) | | 180 | tbd | uA | Vdd1 on (note6), Vsup>12 oscillator running (note 5) excluding CAN current |
| Supply Fail Flag internal threshold | Vthresh | 1.5 | 3 | 4 | V | |
| Supply Fail Flag hysteresis | Vdet hyst | | 1 | | V | guaranteed by design |
| Battery fall early warning threshold | BFew | 5.9 | 6.1 | 6.3 | V | In normal & standby mode |
| Battery fall early warning hysteresis | BFewh | 0.1 | 0.2 | 0.3 | V | In normal & standby mode, guaranteed by design |

note 1: Vdd1>4V, reset high, logic pin high level reduced, device is functional.
note 2: current measured at Vsup pin.
note 3: Device is fully functional. All modes available and operating, Watchdog, HS1 turn ON turn OFF, CAN cell operating, L0 and L1 inputs operating, SPI read write operation. Over temperature may occur.
note 4: Excluding the CAN cell current. An additional 30uA typical must be added to specified value.
note 5: Oscillator running means "Forced Wake Up" or "Cyclic Sense" or "Software Watchdog" timer activated.
note 6: Vdd is ON with2mA typical output current capability.

**Vdd1 (external 5V output for MCU supply). Idd1 is the total regulator output current. Vdd specification with external capacitor C>=22uF and ESR<1O ohm.**

| | | | | | | |
|---|---|---|---|---|---|---|
| Vdd1 Output Voltage | Vdd1out | 4,9 | 5 | 5,1 | V | Idd1 from 2 to 200mA 5.5V< Vsup <27V |
| Vdd1 Output Voltage | Vdd1out | 4 | | | V | Idd1 from 2 to 200mA 4.5V< Vsup <5.5V |
| Drop Voltage Vsup>Vddout | Vdd1drop | | 0.2 | 0,5 | V | Idd1 = 200mA |
| Drop Voltage Vsup>Vddout, limited output current | Vdd1dp2 | | 0,1 | 0,25 | V | Idd1 = 50mA 4.5V< Vsup <27V |
| Idd1 Output Current | Idd1 | 200 | 270 | 350 | mA | Internally limited |
| Vdd1 Output Voltage in stop mode | Vddstop | 4,75 | 5,00 | 5,25 | V | Iout < 2mA |

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($V_{sup}$ From 5.5V to 18V and $T_j$ from -40°C to 125°C) unless otherwise noted. For all pins except can related pins

| Description | Symbol | Characteristics | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Idd1 stop output current to wake up SBC | Idd1s-wu1 | 2 | 3.5 | 5 | mA | Selectable by SPI. Default value after reset. |
| Idd1 stop output current to wake up SBC | Idd1s-wu2 | 10 | 14 | 18 | mA | Selectable by SPI |
| Idd1 over current wake deglitcher (with Idd1s-wu1 selected) | Idd1-dglt1 | 40 | 75 | 55 | us | Guaranteed by design |
| Idd1 over current wake deglitcher (with Idd1s-wu2 selected) | Idd1-dglt2 | | 150 | | us | Guaranteed by design |
| Thermal Shutdown | Tsd | 160 | | 190 | °C | Normal or standby mode |
| Over temperature pre warning | Tpw | 130 | | 160 | °C | VDDTEMP bit set |
| Temperature Threshold difference | Tsd-Tpw | 20 | | 40 | °C | |
| Reset threshold 1 | Rst-th1 | 4.5 | 4.6 | 4.7 | | Selectable by SPI. Default value after reset. |
| Reset threshold 2 | Rst-th2 | 4.1 | 4.2 | 4.3 | | Selectable by SPI |
| Reset duration | reset-dur | 0.85 | 1 | 2 | ms | |
| Vdd1 range for Reset Active | $Vdd_r$ | 1 | | | V | |
| Reset Delay Time | $t_d$ | 5 | | 20 | us | measured at 50% of reset signal. Guaranteed by design |
| Line Regulation | LR1 | | 5 | 25 | mV | $9V<V_{sup}<18$, $I_{dd}$=10mA |
| Line Regulation | LR2 | | 10 | 25 | mV | $5.5V<V_{sup}<27V$, $I_{dd}$=10mA |
| Load Regulation | LD | | 20 | 50 | mV | $1mA<I_{Idd}<200mA$ |
| Thermal stability | ThermS | | 5 | | mV | Vsup=13.5V, I=100mA |

**V2 tracking voltage regulator**
note 7: V2 specification with external capacitor
- option 1: C>=22uF and ESR<1O ohm
- option2: 1uF<C<22uF and ESR<10 ohm. In this case depending upon ballast transistor gain an additional resistor and capacitor network between emitter and base of PNP ballast transistor might be required.

| | | | | | | |
|---|---|---|---|---|---|---|
| V2 Output Voltage | V2 | 0.99 | 1 | 1.01 | Vdd1 | I2 from 2 to 200mA $5.5V< Vsup <27V$ |
| I2 output current (for information only) | I2 | 200 | | | mA | Depending upon external ballast transistor |
| V2 ctrl drive current | I2ctrl | tbd | 10 | tbd | mA | |

**Logic output pins (MISO)**

| | | | | | | |
|---|---|---|---|---|---|---|
| Low Level Output Voltage | Vol | | | 1.0 | V | I out = 1.5mA |
| High Level Output Voltage | Voh | Vdd1-0.9 | | | V | I out = -250uA |
| Tristated MISO Leakage Current | | -2 | | +2 | uA | $0V<V_{miso}<Vdd$ |

**Logic input pins (MOSI, SCLK, CSB)**

| | | | | | | |
|---|---|---|---|---|---|---|
| High Level Input Voltage | Vih | 0.7Vdd1 | | Vdd1+0.3 V | | |
| Low Level Input Voltage | Vil | -0.3 | | 0.3Vdd1 | V | |
| High Level Input Current on CSB | Iih | -100 | | -20 | uA | $V_i$=4V |
| Low Level Input Current CSB | Iil | -100 | | -20 | uA | $V_i$=1V |
| MOSI, SCLK Input Current | Iin | -10 | | 10 | uA | $0<V_{IN}<Vdd$ |

**Reset Pin (output pin only)**

| | | | | | | |
|---|---|---|---|---|---|---|
| High Level Output current | Ioh | | -250 | | uA | $0<V_{out}<0.7Vdd$ |
| Low Level Output Voltage ($I_0$=1.5mA) | Vol | 0 | | 0.9 | V | $5.5v<V_{sup}<27V$ |
| Low Level Output Voltage ($I_0$=tbd mA) | Vol | 0 | | 0.9 | V | $1v<V_{dd1}$ |
| Reset pull down current | Ipdw | 2.4 | | 5 | mA | |
| Reset Duration after Vdd High | reset-dur | 1 | | 2 | ms | |

**Wdogb output pin**

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($V_{sup}$ From 5.5V to 18V and $T_j$ from -40°C to 125°C) unless otherwise noted. For all pins except can related pins

| Description | Symbol | Characteristics | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Low Level Output Voltage ($I_0$=1.5mA) | Vol | 0 | | 0.9 | V | 5.5v<$V_{sup}$<27V |
| High Level Output Voltage ($I_0$=-250uA) | Voh | Vdd1-0.9 | | Vdd1 | | |
| **INT Pin** | | | | | | |
| Low Level Output Voltage ($I_0$=1.5mA) | Vol | 0 | | 0.9 | V | |
| High Level Output Voltage ($I_0$=-250uA) | Voh | Vdd1-0.9 | | Vdd1 | | |
| **HS1: 150mA High side output pin** | | | | | | |
| Rdson at Tj=25°C, and Iout -150mA | Rdson25 | | | 2.5 | Ohms | Vsup>9V |
| Rdson at Tj=125°C, and Iout -150mA | Rdson125 | | | 5 | Ohms | Vsup>9V |
| Rdson at Tj=125°C, and Iout -120mA | Ron125-2 | | 4 | 5.5 | Ohms | 5.5V<Vsup<9V |
| Output current limitation | Ilim | 200 | | 500 | mA | |
| Over temperature Shutdown | Ovt | 155 | | 190 | °C | |
| Leakage current | Ileak | | | 10 | uA | |
| Output Clamp Voltage at Iout= -1mA | Vcl | -1.5 | | -0.3 | V | no inductive load drive capability |
| Cyclic sense period (refer to SPI) | T1 | | | | ms | in sleep and stop modes |
| Cyclic sense On time (refer to SPI) | T2 | | 100 | | us | in sleep and stop modes |
| Timing accuracy (cyclic sense period and on time) | Tacc | -30 | | +30 | % | in sleep and stop mode |
| **L0 and L1 inputs** | | | | | | |
| L0 Negative Switching Threshold | Vth0n | 1.7<br>2<br>2 | tbd<br><br>tbd | 3<br>3<br>3.1 | V | 5.5V<Vsup<6V<br>6V<Vsup<18V<br>18V<Vsup<27V |
| L0 Positive Switching Threshold | Vth0p | 2.2<br>2.5<br>2.5 | tbd<br><br>tbd | 4<br>4<br>4.1 | V | 5.5V<Vsup<6V<br>6V<Vsup<18V<br>18V<Vsup<27V |
| L1 Negative Switching Threshold | Vth1n | 2<br>2.5<br>2.7 | 2.5<br>3<br>3.2 | 3<br>3.6<br>3.7 | V | 5.5V<Vsup<6V<br>6V<Vsup<18V<br>18V<Vsup<27V |
| L1 Positive Switching Threshold | Vth1p | 2.7<br>3<br>3.5 | 3.3<br>4<br>4.2 | 3.8<br>4.6<br>4.7 | V | 5.5V<Vsup<6V<br>6V<Vsup<18V<br>18V<Vsup<27V |
| Hysteresis | Vhyst | 0.6 | <br>tbd | 1.3 | V | 5.5V<Vsup<18V<br>18V<Vsup<27V |
| Input current | Iin | -10 | | 10 | uA | -0.2V < Vin < 40V |
| Wake up Filter Time (enable/disable option on L0 input) | | 8 | 20 | 38 | us | (If filter enable) |
| **DIGITAL INTERFACE TIMING** | | | | | | |
| SPI operation frequency | Freq | | | 4 | MHz | |
| SCLK Clock Period | $t_{pCLK}$ | 250 | | | ns | |
| SCLK Clock High Time | $t_{wSCLKH}$ | 125 | | | ns | |
| SCLK Clock Low Time | $t_{wSCLKL}$ | 125 | | | ns | |
| Falling Edge of CS to Rising Edge of SCLK | $t_{lead}$ | 100 | 50 | | ns | |
| Falling Edge of SCLK to Rising Edge of CS | $t_{lag}$ | 100 | 50 | | ns | |
| MOSI to Falling Edge of SCLK | $t_{SISU}$ | 40 | 25 | | ns | |
| Falling Edge of SCLK to MOSI | $t_{SIH}$ | 40 | 25 | | ns | |
| MISO Rise Time (CL = 220pF) | $t_{rSO}$ | | 25 | 50 | ns | |
| MISO Fall Time (CL = 220pF) | $t_{fSO}$ | | 25 | 50 | ns | |

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(V$_{sup}$ From 5.5V to 18V and T$_j$ from -40°C to 125°C) unless otherwise noted. For all pins except can related pins

| Description | Symbol | Characteristics | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Time from Falling or Rising Edges of CS to:<br>- MISO Low Impedance<br>- MISO High Impedance | t$_{SOEN}$<br>t$_{SODIS}$ | | | 50<br>50 | ns | |
| Time from Rising Edge of SCLK to MISO Data Valid | t$_{valid}$ | | | 50 | ns | 0.2 V1≤SO≥ 0.8V1,<br>C$_L$=200pF |

**STATE MACHINE TIMING**
**note 1: delay starts at rising edge of CSB (end of SPI command) and start of Turn on or Turn off of HS1 or V2.**

| Description | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Delay between CSB low to high transition (at end of SPI stop command) and Stop or sleep mode activation | Tcsb-stop | 18 | | 34 | us | Guaranteed by design detected by V2 off |
| Interrupt low level duration | Tint | 7 | 10 | 13 | us | SBC in stop mode |
| Internal oscillator frequency | Osc-f1 | | 100 | | kHz | All modes except Sleep and Stop, guaranteed by design |
| Internal low power oscillator frequency | Osc-f2 | | 100 | | kHz | Sleep and Stop modes, guaranteed by design |
| Watchdog period 1 | Wd1 | 8.58 | 9.75 | 10.92 | ms | Normal and standby modes |
| Watchdog period 2 | Wd2 | 39.6 | 45 | 50.4 | ms | Normal and standby modes |
| Watchdog period 3 | Wd3 | 88 | 100 | 112 | ms | Normal and standby modes |
| Watchdog period 4 | Wd4 | 308 | 350 | 392 | ms | Normal and standby modes |
| Watchdog period accuracy | F1acc | -12 | | 12 | % | Normal and standby modes |
| Normal request mode timeout | NRtout | 308 | 350 | 392 | ms | Normal request mode |
| Watchdog period 1 - stop | Wd1stop | 6.82 | 9.75 | 12.7 | ms | Stop mode |
| Watchdog period 2- stop | Wd2stop | 31.5 | 45 | 58.5 | ms | Stop mode |
| Watchdog period 3 - stop | Wd3stop | 70 | 100 | 130 | ms | Stop mode |
| Watchdog period 4 - stop | Wd4stop | 245 | 350 | 455 | ms | Stop mode |
| Stop mode watchdog period accuracy | F2acc | -30 | | 30 | % | Stop mode |
| Cyclic sense/FWU timing 1 | CSFWU1 | 3.22 | 4.6 | 5.98 | ms | Sleep and stop modes |
| Cyclic sense/FWU timing 2 | CSFWU2 | 6.47 | 9.25 | 12 | ms | Sleep and stop modes |
| Cyclic sense/FWU timing 3 | CSFWU3 | 12.9 | 18.5 | 24 | ms | Sleep and stop modes |
| Cyclic sense/FWU timing 4 | CSFWU4 | 25.9 | 37 | 48.1 | ms | Sleep and stop modes |
| Cyclic sense/FWU timing 5 | CSFWU5 | 51.8 | 74 | 96.2 | ms | Sleep and stop modes |
| Cyclic sense/FWU timing 6 | CSFWU6 | 66.8 | 95.5 | 124 | ms | Sleep and stop modes |
| Cyclic sense/FWU timing 7 | CSFWU7 | 134 | 191 | 248 | ms | Sleep and stop modes |
| Cyclic sense/FWU timing 8 | CSFWU8 | 271 | 388 | 504 | ms | Sleep and stop modes |
| Cyclic sense On time | Ton | 200 | 350 | 500 | us | in sleep and stop modes threshold and condition to be added |
| Cyclic sense/FWU timing accuracy | Tacc | -30 | | +30 | % | in sleep and stop mode |
| Delay between SPI command and HS1 turn on (note 1) | Ts-HSon | | | 22 | us | Normal or standby mode Vsup>9V |
| Delay between SPI command and HS1 turn off (note 1) | Ts-HSoff | | | 22 | us | Normal or standby mode Vsup>9V |
| Delay between SPI and V2 turn on (note 1) | Ts-V2on | 9 | | 22 | us | Standby mode |
| Delay between SPI and V2 turn off (note 1) | Ts-V2off | 9 | | 22 | us | Normal modes |
| Delay between Normal Request and Normal mode, after W/D trigger command | Ts-NR2N | 15 | 35 | 70 | us | Normal request mode |

| Delay between SPI and "CAN normal mode" | Ts-CANn | | | 10 | us | SBC Normal mode guaranteed by design |
|---|---|---|---|---|---|---|
| Delay between SPI and "CAN sleep mode" | Ts-CANs | | | 10 | us | SBC Normal mode guaranteed by design |
| Delay between CSB wake up (CSB low to high) and SBC normal request mode (Vdd1 on & reset high) | Tw-csb | 15 | 40 | 90 | us | SBC in stop mode |
| Delay between CSB wake up (CSB low to high) and first accepted SPI command | Tw-spi | 90 | | N/A | us | SBC in stop mode |
| Delay between INT pulse and 1st SPI command accepted | Ts-1stspi | 20 | | N/A | us | In stop mode after wake up |

**Figure 2. Timing Characteristics**

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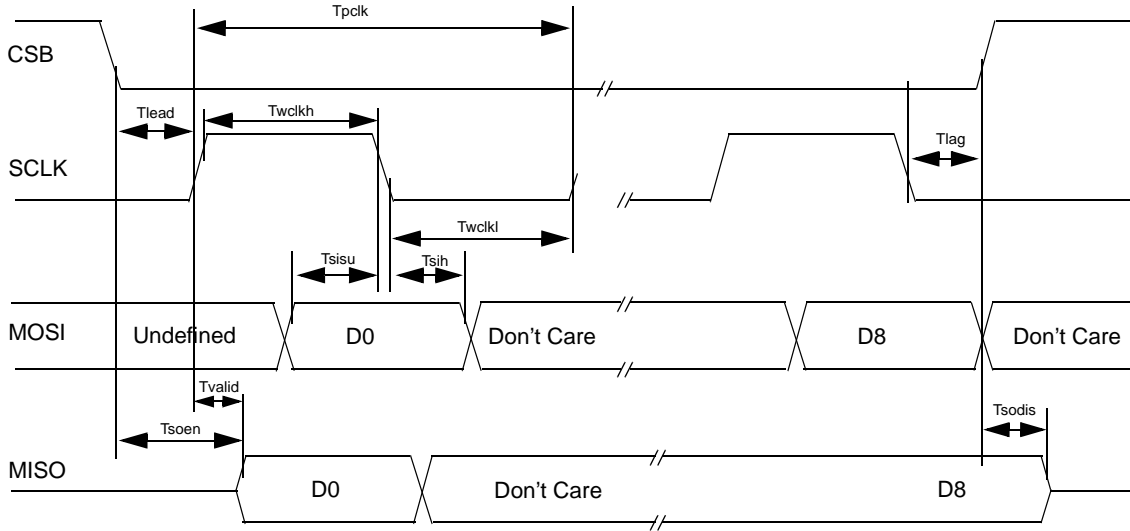
**Freescale Semiconductor, Inc.**

## 3 CAN MODULE SPECIFICATION (COMPATIBLE WITH MC33388)

ELECTRICAL RATINGS

| Ratings | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DC Voltage On Pins Tx, Rx | Vlogic | -0.3 | | $V_{DD1}$ + 0.3 | V |
| DC voltage at V2 (V2int) | V2int | 0 | | 5.25 | V |
| DC Voltage On Pins CANH, CANL | $V_{BUS}$ | -20 | | +27 | V |
| Transient Voltage At Pins CANH, CANL $0 < V_{2\text{-}int} < 5.5V$; $V_{sup} \geq 0$; T < 500ms | $V_{CANH}/V_{CANL}$ | -40 | | 40 | V |
| Transient Voltage On Pins CANH, CANL (Coupled Through 1nF Capacitor) | $V_{tr}$ | -150 | | 100 | V |
| DC Voltage On Pins Rth, Rtl | $V_{rtl}$, $V_{rth}$ | -0.3 | | +27 | V |
| Transient Voltage At Pins RtH, RtL $0 < V_{2\text{-}int} < 5.5V$; $V_{sup} \geq 0$; T < 500ms | $V_{RtH}/V_{RtL}$ | -0.3 | | 40 | V |
| RTH, RTL Termination Resistance | $R_t$ | 500 | | 16000 | ohm |

ELECTRICAL CHARACTERISTICS ($V_{sup}$ From 5.5V to 18V, V2int from 4.75 to 5.25V and $T_j$ from -40°C to 150°C unless otherwise noted).

| Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Supply current described below are the CAN module internal supply current from internal V2 (V2-int) and Vsup** | | | | | |
| Internal V2 Supply Current (CAN and SBC in Normal Mode). TX= 5V, CAN in Recessive State | $I_{V2\text{-}int}$ | 4 | 5.6 | 6.5 | mA |
| Internal V2 Supply Current (CAN and SBC in Normal Mode). TX = 0V, No Load, CAN in Dominant State | $I_{V2\text{-}int}$ | 4.2 | 5.8 | 6.7 | mA |
| Total supply Current (CAN in Receive Only Mode, SBC in Normal mode). Internal V2 = 5V; $V_{sup}$ = 12V | $I_{V2\text{-}int} + I_{SUP\text{-}int}$ | | 1 | 1.4 | mA |
| Internal V2 Supply Current (CAN in Bus TermVbat mode) $V_{sup}$ = 12V | $I_{V2\text{-}int}$ | | 36 | tbd | uA |
| **TX Pin** | | | | | |
| High Level Input Voltage | $V_{ih}$ | $0.7*V_{2\text{-}int}$ | | $V_{2\text{-}int}+0.3V$ | V |
| Low Level Input Voltage | $V_{il}$ | -0.3 | | $0.3 * V_{2\text{-}int}$ | V |
| TX High Level Input Current ($V_i$ = 4V) | $I_{TX}$ | -100 | -50 | -25 | uA |
| TX Low Level Input Current ($V_i$ = 1V) | $I_{TX}$ | -100 | -50 | -25 | uA |
| **RX Pin** | | | | | |
| High Level Output Voltage RX ($I_0$ = -250µA) | $V_{oh}$ | $V_{2\text{-}int}$ - 0.9 | | $V_{2\text{-}int}$ | V |
| Low Level Output Voltage ($I_0$ = 1.5mA) | $V_{ol}$ | 0 | | 0.9 | V |
| **CANH, CANL Pins** | | | | | |
| Differential Receiver, Recessive To Dominant Threshold (By Definition, $V_{diff}=V_{CANH}-V_{CANL}$) | $V_{diff1}$ | -3.2 | | -2.5 | V |

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| Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Differential Receiver, Dominant To Recessive Threshold (Bus Failures 1, 2, 5) | $V_{diff2}$ | -3.2 | | -2.5 | V |
| CANH Recessive Output Voltage TX = 5V; $R_{(RTH)}$ < 4k | $V_{CANH}$ | | | 0.2 | V |
| CANL Recessive Output Voltage TX =5V; $R_{(RTL)}$ < 4k | $V_{CANL}$ | $V_{2-int}$ - 0.2 | | | V |
| CANH Output Voltage, Dominant TX = 0V; $I_{CANH}$ = -40mA; Normal Operating Mode | $V_{CANH}$ | $V_{2-int}$ - 1.4 | | | V |
| CANL Output Voltage, Dominant TX = 0V; $I_{CANL}$ = 40mA; Normal Operating Mode | $V_{CANL}$ | | | 1.4 | V |
| CANH Output Current ($V_{CANH}$ = 0 ; TX = 0) | $I_{CANH}$ | 50 | 75 | 100 | mA |
| CANL Output Current ($V_{CANL}$ = 14V; TX = 0) | $I_{CANL}$ | 50 | 90 | 130 | mA |
| Detection Threshold For Short-circuit To Battery Voltage (Normal Mode) | $V_{CANH}$, $V_{CANL}$ | 7.3 | 7.9 | 8.9 | V |
| Detection Threshold For Short-circuit To Battery Voltage (Term Vbat Mode) | $V_{CANH}$ | $V_{BAT}$/2 +3 | | $V_{BAT}$ /2+5 | V |
| CANH Output Current (Term Vbat Mode; $V_{CANH}$ = 12V, Failure3) | | | 5 | 10 | uA |
| CANL Output Current (Term Vbat Mode; $V_{CANL}$ = 0V; $V_{BAT}$ = 12V, Failure 4) | $I_{CANL}$ | | 0 | 2 | uA |
| CANL Wake Up Voltage Threshold | $V_{wake,L}$ | 2.5 | 3 | 3.9 | V |
| CANH Wake Up Voltage Threshold | $V_{wake,H}$ | 1.2 | 2 | 2.7 | V |
| Wake Up Threshold Difference (Hysteresis) | $V_{wakeL}$-$V_{wakeH}$ | 0.2 | | | V |
| CANH Single Ended Receiver Threshold (Failures 4, 6, 7) | $V_{SE, CANH}$ | 1.5 | 1.85 | 2.15 | V |
| CANL Single Ended Receiver Threshold (Failures 3, 8) | $V_{SE, CANL}$ | 2.8 | 3.05 | 3.4 | V |
| CANL Pull Up Current (Normal Mode) | $I_{CANL,pu}$ | 45 | 75 | 90 | uA |
| CANH Pull Down Current (Normal Mode) | $I_{CANH,pd}$ | 45 | 75 | 90 | uA |
| Receiver Differential Input Impedance CANH / CANL | $R_{diff}$ | 100 | | 300 | kohm |
| Differential Receiver Common Mode Voltage Range | $V_{com}$ | -10 | | 10 | V |
| CANH To Ground Capacitance | $C_{CANH}$ | | | 50 | pF |
| CANL To Ground Capacitance | $C_{CANL}$ | | | 50 | pF |
| $C_{CANL}$ to $C_{CANH}$ Capacitor Difference (Absolute Value) | $DC_{can}$ | | | 10 | pF |

**RTH, RTL Pins**

| Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RTL to V2-int Switch On Resistance ($I_{out}$ < -10mA; Normal Operating Mode) | $R_{rtl}$ | 10 | 30 | 90 | ohms |
| RTL to BAT Switch Series Resistance (term Vbat Mode) | $R_{rtl}$ | 8 | 12.5 | 20 | kohm |
| RTH To Ground Switch On Resistance ($I_{out}$ <10mA; Normal Operating Mode) | $R_{rth}$ | 10 | 30 | 90 | ohm |

**Thermal Shutdown**

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| Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| CAN Module Thermal Shutdown | $T_{sd}$ | | 165 | | °C |

**AC CHARACTERISTICS** ($V_{sup}$ From 5.5V to 18V and $T_j$ from -40°C to 150°C unless otherwise noted)

| Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| CANL and CANH Slew Rates (10% to 90%). Rising or Falling Edges. Note 1.Recessive to Dominant state. | $T_{sldr}$ | 2 | | 8 | V/us |
| CANL and CANH Slew Rates (10% to 90%). Rising or Falling Edges. Note 1.Dominant to Recessive. Note 1. | $T_{slrd}$ | 2 | | 9 | V/us |
| Propagation Delay TX to RX Low. Note 2. | $T_{onRX}$ | | 1 | 1.6 | us |
| Propagation Delay TX to RX High. Note 2. | $T_{offRX}$ | | 1 | 1.6 | us |
| Min. Dominant Time For Wake-up On CANL or CANH (Term Vbat; $V_{SUP}$ = 12V) Guaranteed by design. | $T_{wake}$ | 8 | 16 | 30 | us |
| Failure 3 Detection Time (Normal Mode) | $T_{df3}$ | 10 | 30 | 80 | us |
| Failure 6 Detection Time (Normal Mode) | $T_{df6}$ | 50 | 200 | 500 | us |
| Failure 3 Recovery Time (Normal Mode) | $T_{dr3}$ | | 160 | | us |
| Failure 6 Recovery Time (Normal Mode) | $T_{dr6}$ | 150 | 200 | 1000 | us |
| Failure 4, 7, 8 Detection Time (Normal Mode) | $T_{df478}$ | 0.75 | 1.5 | 4 | ms |
| Failure 4, 7, 8 Recovery Time (Normal Mode) | $T_{dr478}$ | 10 | 30 | 60 | us |
| Failure 4, 7,8 Detection Time, (Term Vbat; $V_{SUP}$ = 12V) | $T_{dr47}$ | 0.8 | 1.2 | 8 | ms |
| Failure 3 Detection Time (Term Vbat; $V_{SUP}$ = 12V) | $T_{dr3}$ | | 3.84 | | ms |
| Failure 3a Detection Time (Term Vbat; $V_{SUP}$ = 12V) | $T_{dr3a}$ | | 2.3 | | ms |
| Failure 4, 7,8 Recovery Time (Term Vbat; $V_{SUP}$ = 12V) | $T_{dr47}$ | | 1.92 | | ms |
| Failure 3 Recovery Time (Term Vbat; $V_{SUP}$ = 12V) | $T_{dr3}$ | | 1.2 | | ms |
| Failure 3a Recovery Time (Term Vbat; $V_{SUP}$ = 12V) | $T_{dr3a}$ | | 1.92 | | ms |
| Edge Count Difference Between CANH and CANL for Failures 1, 2, 5 Detection (Failure bit set, Normal Mode) | $E_{cdf}$ | | 3 | | |
| Edge Count Difference Between CANH And CANL For Failures 1, 2, 5 Recovery (Normal Mode) | $E_{cdr}$ | | 3 | | |
| TX Permanent Dominant Timer Disable Time (Normal Mode And Failure Mode) | $t_{TX,d}$ | 0.75 | | 4 | ms |
| TX Permanent Dominant Timer Enable Time (Normal Mode And Failure Mode) | $t_{TX,e}$ | 10 | | 60 | us |

NOTE 1: Dominant to recessive slew rate is dependant upon the bus load characteristics.
NOTE 2: AC Characteristics measured according to schematic figure 3.
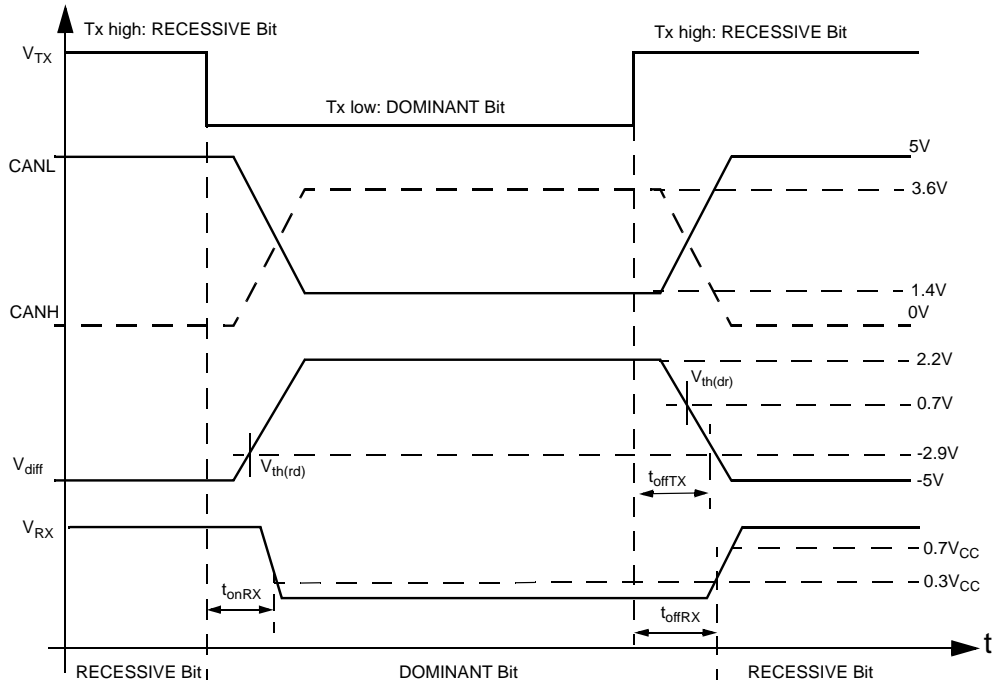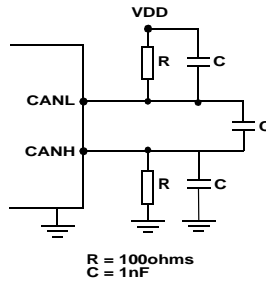
**Figure 3. Device Signal Waveforms**



**Figure 4. Test Circuit for AC Characteristics**



R = 100ohms
C = 1nF

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# 4 DEVICE DESCRIPTION

Introduction:

The MC33889 is an integrated circuit dedicated to automotive applications. It includes the following functions:

- One full protected voltage regulator with 200mA total output current capability.
- Driver for external path transistor for V2 regulator function.
- Reset, programmable watchdog function
- Four operational modes
- Wake up capabilities: Forced wake up, cyclic sense and wake up inputs, CAN and SPI
- Can low speed fault tolerant physical interface, compatible with Motorola MC33388D.

## 4.1 Device Supply

The device is supplied from the battery line through the Vsup pin. An external diode is required to protect against negative transients and reverse battery. It can operate from 4.5V and under the jump start condition at 27V DC. This pin sustains standard automotive voltage conditions such as load dump at 40V. When Vsup falls below 3V typical the MC33889 detects it and store the information into the SPI register, in a bit called "BATFAIL". This detection is available in all operation modes.

## 4.2 Vdd1 Voltage Regulator

Vdd1 Regulator is a 5V output voltage with total current capability of 200mA. It includes a voltage monitoring circuitry associated with a reset function. The Vdd1 regulator is fully protected against over current, short-circuit and has over temperature detection warning flags and shutdown with hysteresis.

## 4.3 V2 regulator

V2 Regulator circuitry is designed to drive an external path transistor in order to increase output current flexibility. Two pins are used: V2 and V2 ctrl. Output voltage is 5V and is realized by a tracking function of the Vdd1 regulator. Recommended ballast transistor is MJD32C. Other transistor might be used, however depending upon PNP gain an external resistor capacitor network might be connected between emitter and base of PNP. The use of external ballast is optional (refer to simplified typical application). State of V2 is reported into IOR register (if V2 is below 4.5V typical in case of over load or short circuit).

## 4.4 HS1 Vbat Switch Output

HS1 output is a 2 ohms typical switch from Vsup pin. It allows the supply of external switches and their associated pull up or pull down circuitry, in conjunction with the wake up input pins for example. Output current is limited to 200mA and HS1 is protected against short-circuit and has an over temperature shutdown (reported in IOR register). HS1 output is controlled from the internal register and SPI. It can be activated at regular intervals in sleep mode thanks to internal timer. It can also be permanently turned on in normal or stand-by modes to drive external loads such as relays or supply peripheral components. In case of inductive load drive external clamp circuitry must be added.

## 4.5 Functional Modes

The device has four modes of operation, stand-by, normal, stop and sleep modes. All modes are controlled by the SPI. An additional temporary mode called "normal request mode" is automatically accessed by the device (refer to state machine) after wake up events. Special mode and configuration are possible for software application debug and flash memory programming.

### 4.5.1 Normal mode:

In this mode both regulators are ON and this corresponds to the normal application operation. All functions are available in this mode (watchdog, wake up input reading through SPI, HS1 activation, CAN communication). The software watchdog is running and must be periodically cleared through SPI.

### 4.5.2 Standby mode:

Only the regulator 1 is ON. Regulator 2 is turned OFF by disabling the V2 ctrl pin. The CAN cell is not available, as powered from V2, other functions are available: wake up input reading through SPI, HS1 activation. The watchdog is running.

### 4.5.3 Sleep mode:

Regulators 1 and 2 are OFF. In this mode, the MCU is not powered. In this mode, the device can be awakened internally by cyclic sense via the wake up inputs pins and HS1 output, from the forced wake function, the CAN physical interface, and SPI (CSB pin).

### 4.5.4 Stop mode

Regulator 2 is turned OFF by disabling the V2 ctrl pin. The regulator 1 is activated in a special low power mode which allow to deliver 2 mA. The objective is to maintain the MCU of the application supplied while it is turned into power saving condition (i.e stop or wait mode).

Stop mode is entered through SPI. Stop mode is dedicated to power the Microcontroller when it is in low power mode (stop, pseudo stop, wait etc.). In these mode the MCU supply current is less than 1mA. The MCU can restart its software application very quickly, without the complete power up and reset sequence.

When the application is in stop mode (both MCU and SBC), the application can wake up from the SBC side (ex cyclic sense, forced wake up, CAN message, wake up inputs) or the MCU side (key wake up etc.).

When Stop mode is selected by SPI, stop mode becomes active 20us after end of SPI message. The "go to stop" instruction must be the last instruction executed by the MCU before going to low power mode.

In stop mode the Software watchdog can be "running" or "not running" depending upon selection by SPI. Refer to SPI description, RCR register bit WDSTOP. If W/D is enabled the SBC must be wake up before W/D time expired, otherwise a reset is generated. In stop mode, SBC wake up capability are identical as in sleep mode.

#### 4.5.4.1  Stop mode: wake up from SBC side, INT pin activation:

When application is in stop mode, it can wake up from the SBC side. When a wake up is detected by the SBC (ex CAN, Wake up input, forced wake up etc.) the SBC turns itself into Normal request mode and activated the Vdd1 main regulator. When the main regulator is fully active, then the wake up is signalled to the MCU through the INT pin. INT pin is pulled low for 10us and then returns high. Wake up event can be read through the SPI registers.

#### 4.5.4.2  Stop mode: wake up from MCU side:

When application is in stop mode, the wake up event may come to the MCU. In this case the MCU has to signal to the SBC that it has to go into Normal mode in order for the Vdd1 regulator to be able to deliver full current capability. This is done by a low to high transition of the CSB pin. CSB pin low to high activation has to be done as soon as possible after the MCU. The SBC generates a pulse at INTB pin. Alternatively the L0 and L1 inputs can also be used as wake up from stop mode.

#### 4.5.4.3  Stop mode current monitoring

If the current in stop mode exceed the Idd1s-wu threshold, the SBC jumps into Normal request mode, activated the Vdd1 main regulator and generate and interrupt to the MCU. This interrupt is not maskable and not bit are set into the INT register.

#### 4.5.4.4  Software watchdog in stop mode:

If watchdog is enabled (register MCR, bit WDSTOP set), the MCU has to wake up independently of the SBC before the end of the SBC watchdog time. In order to do this the MCU has to signal the wake to the SBC through the SPI wake up (CSB pin low to high transition to activated SPI wake up). Then the SBC wakes up and jump into the normal request mode. MCU has to configure the SBC to go to either normal or standby mode. The MCU can then decide to go back again to stop mode.

If no MCU wakes up occurs within the watchdog timing, the SBC will activate the reset pin and jump into the normal request mode. The MCU can then be initialized.

#### 4.5.5  Normal request mode:

This is a temporary mode automatically accessed by the device after a wake up event from sleep or stop mode or after device power up. In this mode the Vdd1 regulator is ON, V2 is off, the reset pin is high. As soon as the device enters the normal request mode an internal 350ms timer is started. During these 350ms the micro controller of the application must addressed the SBC via SPI and configure the watchdog register (TIM1 register). This is the condition for the SBC to leave the Normal request Mode and enter the Normal mode and to set the watchdog timer according to configuration done during the Normal Request mode.

"BATFAIL flag" is a bit which is triggered when Vsup is below 3V. This bit is set into the MCR register. It is reset by MCR register read.

### 4.6  Internal Clock

The device has an internal clock used to generate all timings (reset, watchdog, cyclic wake up, filtering time etc....).

### 4.7  Reset pin

A reset output is available in order to reset the microcontroller. The reset cause are:

- Vdd1 falling out of range: if Vdd1 fall below the reset threshold (parameter Rst-th), the reset pin is pull low until Vdd1 return to nominal voltage.

- Power on reset: at device power on or at device wake up from sleep mode, the reset is maintained low until Vdd1 is within its operation range.

- Watchdog time out: if the watchdog is not cleared the SBC will pull the reset pin low for the duration of the reset duration time (parameter: reset-dur).

For debug purposes at 25°C, reset pin can be shorted to 5V.

### 4.8  Software watchdog (selectable window or time out watchdog)

Software watchdog is used in the SBC normal and stand-by modes for the MCU monitoring. The watchdog can be either window or time out. This is selectable by SPI (register TIM, bit WDW). Default is window watchdog. The period for the watchdog is selectable by SPI from 5 to 350ms (register TIM, bits WDT0 and WDT1). When the window watchdog is selected, the closed window is the first half of the selected period, and the open window is the second half of the period. The watchdog can only be cleared within the open window time. An attempt to clear the watchdog in the closed window will generate a reset. Watchdog is cleared through SPI by addressing the TIM register.

Refer to" table for reset pin operations operation in mode 2.

### 4.9  Wake Up capabilities

Several wake-up capabilities are available for the device when it is in sleep or stop mode. When a wake up has occurred, the wake up event is stored into the WUR or CAN registers. The MCU can then access to the wake up source. The wake up options are selectable trough SPI while the device is in normal or standby mode and prior to go to enter low power mode (sleep or stop mode).

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### 4.9.1 Wake up from wake up inputs (L0, L1) without cyclic sense:

The wake up lines are dedicated to sense external switches state and if changes occur to wake up the MCU (In sleep or stop modes). The wake up pins are able to handle 40V DC. The internal threshold is 3V typical and these inputs can be used as input port expander. The wake up inputs state can be read through SPI (register WUR). L0 has a lower threshold than L1 in order to allow connection and wake up from a digital output such as a CAN physical interface for instance.

### 4.9.2 Cyclic sense wake up (Cyclic sense timer and wake up inputs L0, L1)

The SBC can wake up upon state change of one of the wake up input lines (L0, L1) while the external pull up or pull down resistor of the switches associated to the wake up input lines are biased with HS1 Vsup switch. The HS1 switch is activated in sleep or stop mode from an internal timer. Cyclic sense and Forced wake up are exclusive. If Cyclic Sense is enabled the forced wake up can not be enabled.

### 4.9.3 Forced wake up

The SBC can wake up automatically after a pre determined time spent in sleep or stop mode. Forced wake up is enabled by setting bit FWU in LPC register. Cyclic sense and Forced wake up are exclusive. If Forced wake up is enabled the Cyclic Sense can not be enabled.

### 4.9.4 CAN wake up

The device can wake up from a CAN message. CAN wake up cannot be disabled.

### 4.9.5 SPI wake up

The device can wake up by the CSB pin in sleep or stop mode. Wake up is detected by CSB pin transition from  low to high level. In stop mode this correspond to the condition where MCU and SBC are both in Stop mode and when the application wake up events come through the MCU.

### 4.9.6 System power up

At power up the device automatically wakes up.

### 4.10 SPI

The complete device control as well as the status report is done through a 8 bits SPI interface. Refer to SPI paragraph.

### 4.11 CAN

The device incorporates a low speed fault tolerant CAN physical interface. Speed rate is up to 125kBauds. Its electrical parameters for the CANL, CANH, Rtl, Rth Rx and Tx pins are compatible with the MC33388D.
The state of the CAN interface is programmable through SPI.

### 4.12 Device power up, SBC wake up

After device or system power up or a wake up from sleep mode, the SBC enters into "reset mode" then into "normal request mode".

### 4.13 Battery fall early warning:

This function provides an Interrupt when the Vsup voltage is below 6.1V typical. This interrupt is maskable. An hysteresis is included. Operation is only in Normal and Standby modes. Vbat low state reported in IOR register.

### 4.14 Package and thermal consideration

The device is proposed in a standard surface mount SO28 package. In order to improve the thermal performances of the SO28 package, 8 pins are internally connected to the lead frame and are used for heat transfer to the printed circuit board.

### 4.15 Table 1: Reset and Wdogb operation

Figure below shows the reset and watchdog output operation. Reset is active at device power up and wake up. Reset is activated in case of Vdd1 fall or watchdog not triggered. Wdogb output is active low as soon as reset goes low and stays low as long as the watchdog is not properly re-activated by SPI.

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**Figure 5. Reset and Wdogb function diagram**
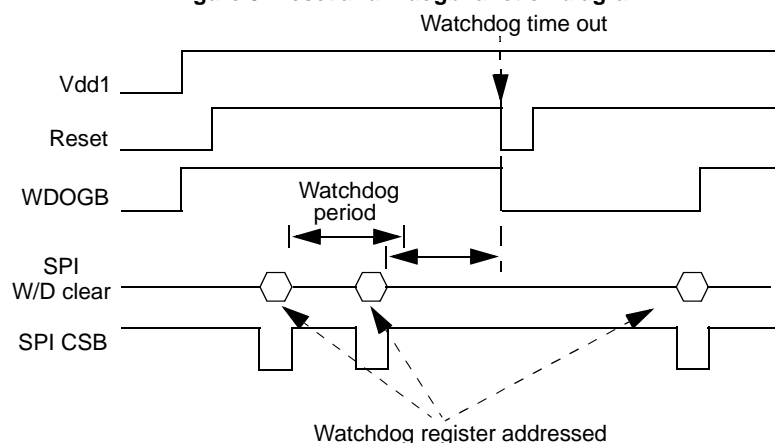


The Wdogb output pin is a push pull structure than can drive external component of the application in order for instance to signal MCU wrong operation. Even if it is internally turned on (low sate) the reset pins can be forced to 5V at 25°C only, thanks to its internal limited current drive capability. Wdogb stays low until the Watchdog register is properly addressed through SPI.

### 4.16    Debug mode Application hardware and software debug with the SBC.

When the SBC is mounted on the same printed circuit board as the micro controller it supplies, both application software and SBC dedicated routine must be debugged. Following features allow the user to debug the software by allowing the possibility to disable the SBC internal software watchdog timer.

### 4.16.1    Device power up, reset pin connected to Vdd1

At SBC power up, the Vdd1 voltage is provided, but if no SPI communication occurs to configure the device, a reset occurs every 350ms. In order to allow software debug and avoid MCU reset the Reset pin can be connected directly to Vdd1 by a jumper.

### 4.16.2    Debug modes with software watchdog disabled though SPI (Normal Debug, Standby Debug and Stop Debug)

The software watchdog can be disabled through SPI. In order to avoid unwanted watchdog disable and to limit the risk of disabling the watchdog during SBC normal operation the watchdog disable has to be done with the following sequence:

Step 1) Power down the SBC

Step 2) Power up the SBC (The BATFAIL bit is set, and the SBC enters normal request mode)

Step 3) Write to TIM1 register to allow SBC to enter Normal mode

Step 4) Write to MCR register with data 0000 (this enables the debug mode). (Complete SPI byte: 000 1 0000)

Step 5) Write to MCR register normal debug (0001 x101), standby debug (0001 x110) or Stop debug (0001 x111)
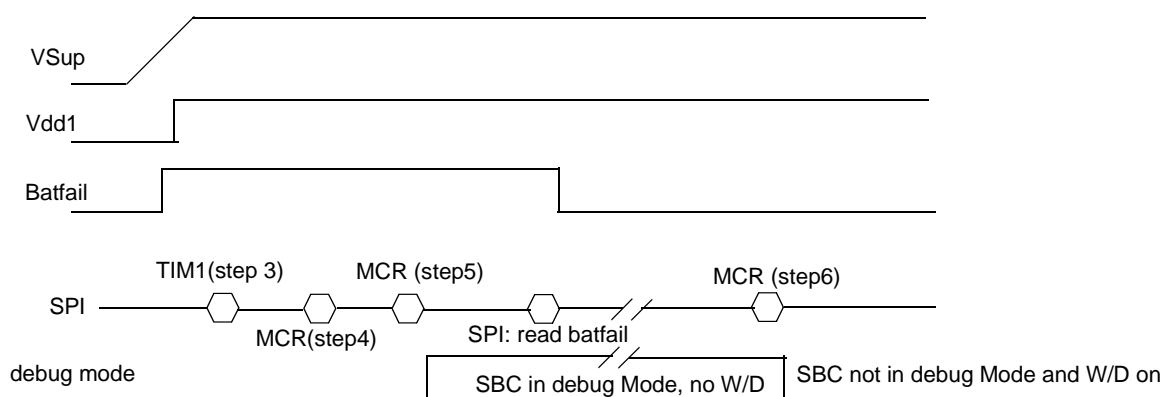
While in debug mode, the SBC can be used without having to clear the W/D on a regular basis to facilitate software and hardware debug.

Step 6) To leave the debug mode, write 0000 to MCR register.

To avoid entering debug mode after a power up, first read BATFAIL bit (MCR read) and write 0000 into MCR.

The graph below illustrates the debug mode entering.

**Figure 6. Debug mode enter**



### 4.16.3    MCU flash programming configuration

In order to allow the possibility to download software into the application memory (MCU EEPROM or Flash) the SBC allows the following capabilities: The Vdd1 can be forced by an external power supply to 5V and the reset and Wdogb outputs by

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external signal sources to zero or 5V and this without damage. This allow for instance to supply the complete application board by external power supply and to apply the correct signal to reset pins.

### 4.17    Gnd Shift Detection

#### 4.17.1    General

When normally working in two-wire operating mode, the CAN transmission can afford some ground shift between different nodes without trouble. Nevertheless, in case of bus failure, the transceiver switches to single-wire operation, therefore working with less noise margin. The affordable ground shift is decreased in this case.

The SBC provides a ground shift detection for diagnosis purpose. Four ground shift levels are selectable and the detection is stored in the IOR register which is accessible via the SPI.

#### 4.17.2    Detection Principle

The gnd shift to detect is selected via the SPI out of 4 different values (-0.5V, -1V, -1.5V, -2V).   At each TX falling edge (end of recessive state) CANH voltage is sensed. If it is detected to be below the selected gnd shift threshold, the bit SHIFT is set at 1 in IOR register. No filter is implemented. Required filtering for reliable detection should be done by software (e.g. several trials).
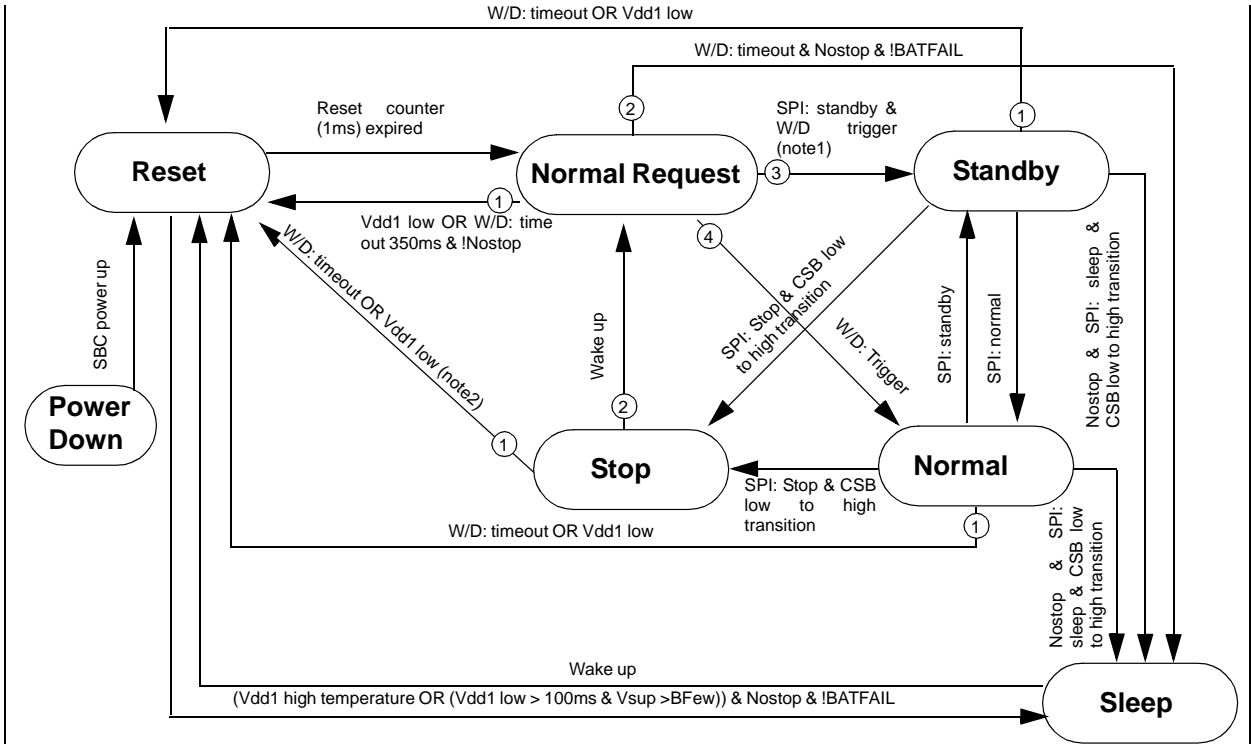
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## 5    TABLE OF OPERATION

The table below describe the SBC operation modes.

| mode | Voltage Regulator HS1 switch | Wake up capabilities (if enabled) | Reset pin | INT | Software Watchdog | CAN cell |
|---|---|---|---|---|---|---|
| Normal Request | Vdd1: ON V2: OFF HS1: OFF | | Low for 1ms, then high | | | term Vbat |
| Normal | Vdd1: ON V2: ON HS1 controllable | | Normally high. Active low if W/D or Vdd1 under voltage occur | If enabled, signal failure (Vdd pre warning temp, CAN, HS1) | Running | Term Vbat Tx/Rx Rec only |
| Standby | Vdd1: ON V2: OFF HS1 controllable | | Normally high. Active low if W/D or Vdd1 under voltage occur | If enabled, signal failure (Vdd temp, HS1) | Running | Term Vbat Tx/Rx Rec only |
| Stop | Vdd1: ON (limited current capability) V2: OFF HS1: OFF or cyclic | CAN (always enable) SPI and L0,L1 Cyclic sense or Forced Wake up | Normally high. Active low if W/D or Vdd1 under voltage occur | Signal SBC wake up (not maskable) | - Running if enabled - Not Running if disabled | Term Vbat. |
| Sleep | Vdd1: OFF V2: OFF HS1 OFF or cyclic | CAN (always enable SPI and L0,L1 Cyclic sense Forced Wake up | Low | Not active | No Running | Term Vbat. |

**Tableau 1 : table of operation**

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## SIMPLIFIED STATE MACHINE

W/D: timeout OR Vdd1 low

W/D: timeout & Nostop & !BATFAIL

Reset counter (1ms) expired

SPI: standby & W/D trigger (note1)

**Reset** → ② **Normal Request** ③ → ① **Standby**

① Vdd1 low OR W/D: time out 350ms & !Nostop

④

SBC power up

W/D: timeout OR Vdd1 low (note2)

Wake up

SPI: Stop & CSB low to high transition

W/D: Trigger

SPI: standby

SPI: normal

Nostop & SPI: sleep & CSB low to high transition

**Power Down**

①

②

**Stop** ← SPI: Stop & CSB low to high transition — **Normal**

W/D: timeout OR Vdd1 low

①

Nostop & SPI: sleep & CSB low to high transition

Wake up

(Vdd1 high temperature OR (Vdd1 low > 100ms & Vsup >BFew)) & Nostop & !BATFAIL

**Sleep**

① ② ③ ④ denotes priority
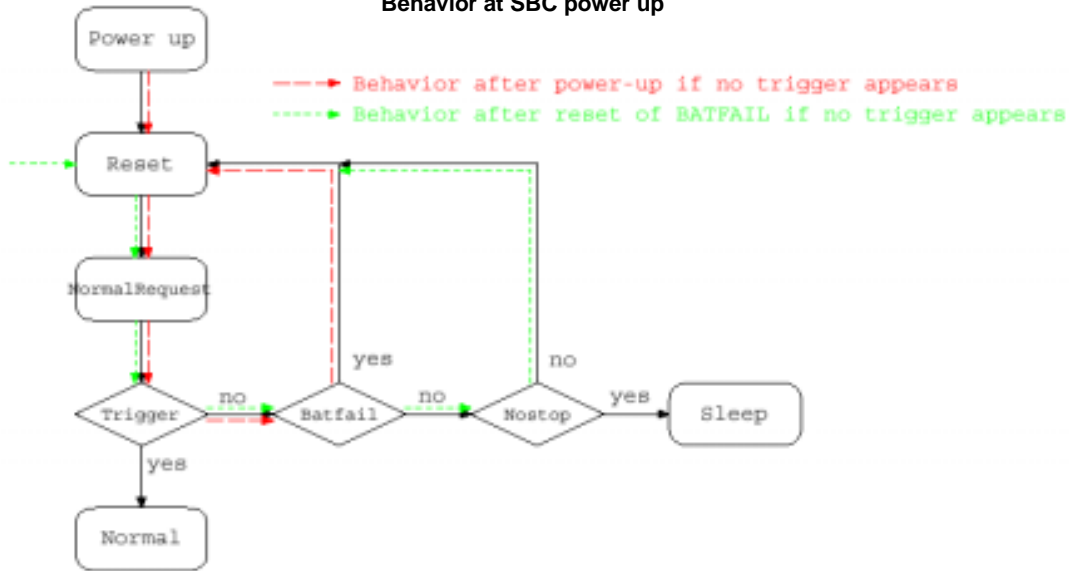
**State machine description:**

"Nostop" means Nostop bit = 1
"! Nostop" means Nostop bit = 0
"BATFAIL" means Batfail bit = 1
"! BATFAIL" means Batfail bit = 0
"Vdd1 over temperature" means Vdd1 thermal shutdown occurs
"Vdd1 low" means Vdd1 below reset threshold
"Vdd1 low > 100ms" means Vdd1 below reset threshold for more than 100ms
"W/D: Trigger" means TIM1 register write operation.
Vsup>BFew means Vsup > Battery Fall Early Warning (6.1V typical)

"W/D: time out" means TIM1 register not written before W/D time out period expired, or W/D written in incorrect time window if window W/D selected (except stop mode). In normal request mode time out is 355ms p2.2 (350ms p3)ms.
"SPI: Sleep" means SPI write command to MCR register, data sleep
"SPI: Stop" means SPI write command to MCR register, data stop
"SPI: Normal" means SPI write command to MCR register, data normal
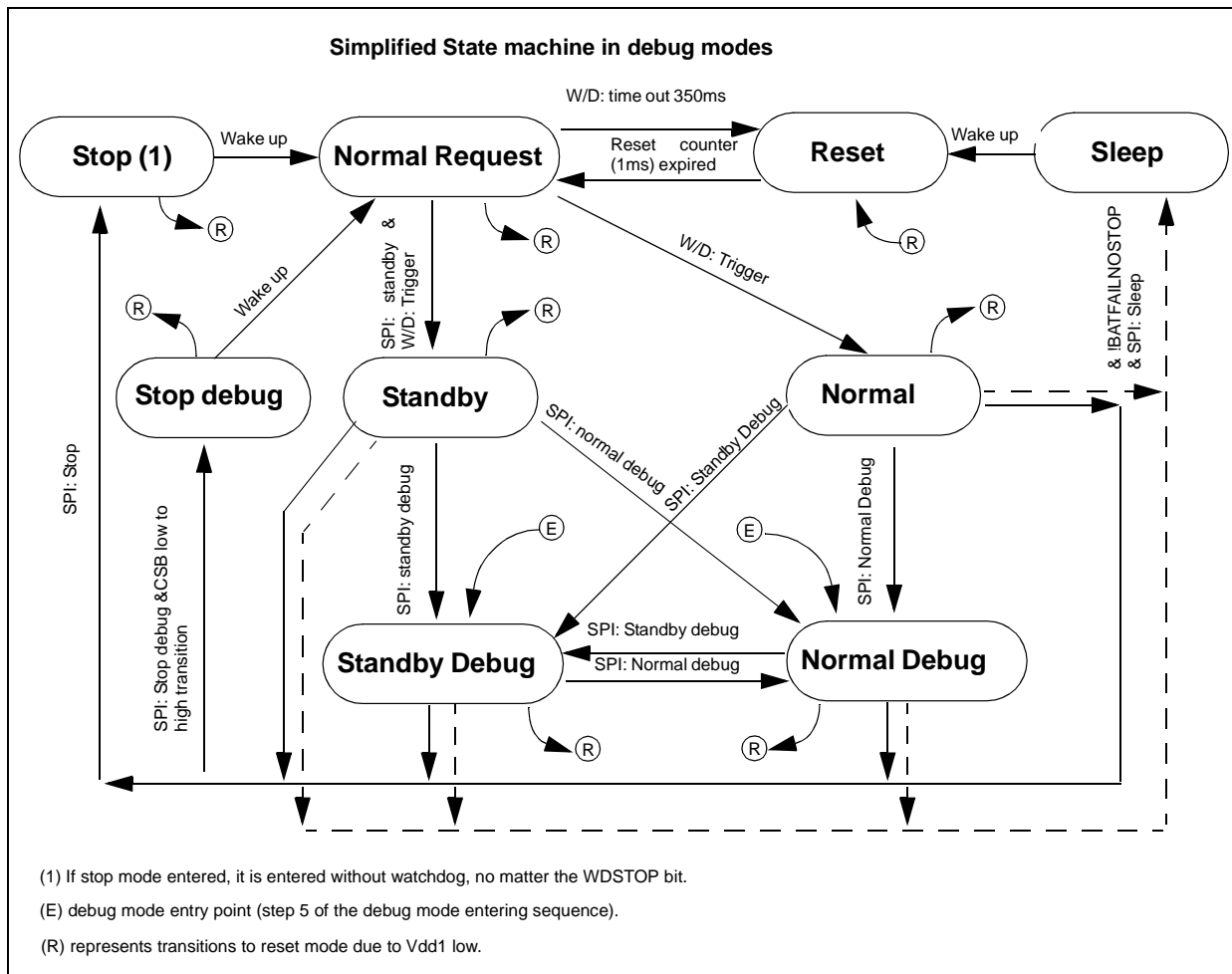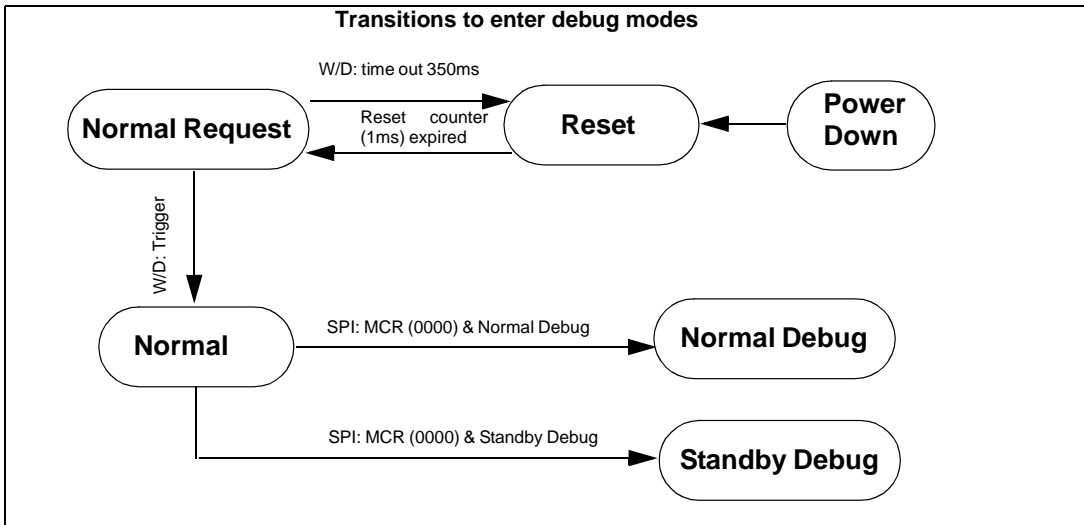"SPI: Standby" means SPI write command to MCR register, data standby

Note 1: these 2 SPI commands must be send in this sequence and consecutively.
Note 2: if W/D activated

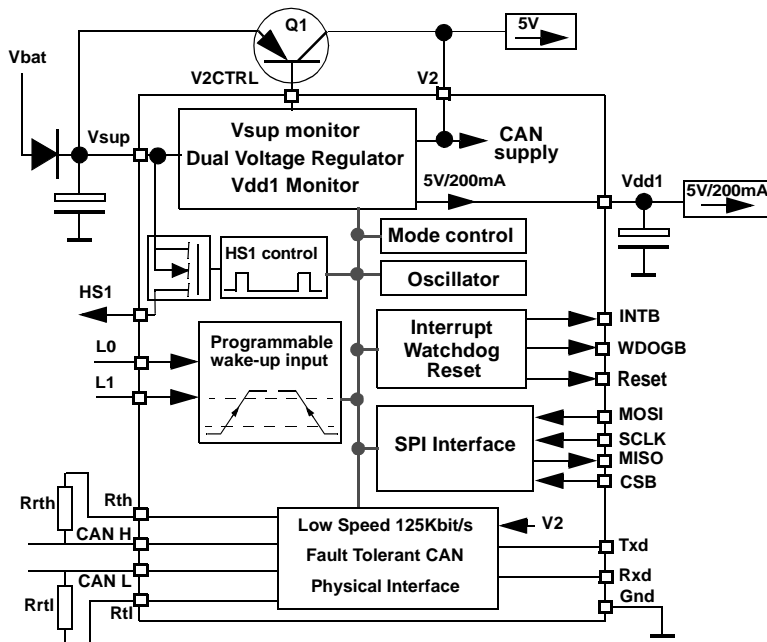### Behavior at SBC power up

Power up

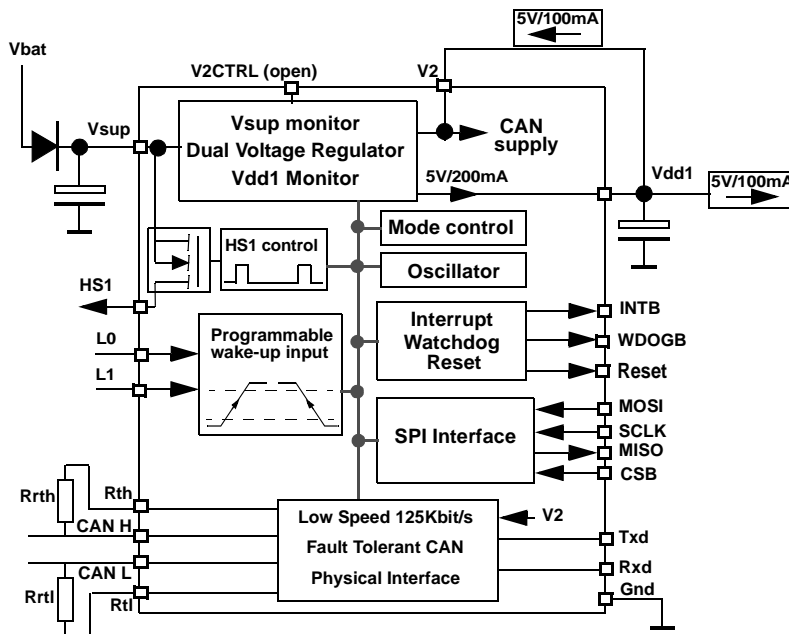- - - → Behavior after power-up if no trigger appears
------→ Behavior after reset of BATFAIL if no trigger appears

Reset

NormalRequest

Trigger — no → Batfail — no → Nostop — yes → Sleep

yes | yes | no

Normal

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## Transitions to enter debug modes

W/D: time out 350ms

**Normal Request** → Reset counter (1ms) expired → **Reset** ← **Power Down**

W/D: Trigger

**Normal** — SPI: MCR (0000) & Normal Debug → **Normal Debug**

SPI: MCR (0000) & Standby Debug → **Standby Debug**

## Simplified State machine in debug modes

W/D: time out 350ms

**Stop (1)** — Wake up → **Normal Request** → Reset counter (1ms) expired → **Reset** ← Wake up — **Sleep**

(R)

W/D: Trigger

(R)

(R)

Wake up

SPI: standby & W/D: Trigger

& IBATFAILNOSTOP & SPI: Sleep

(R)

**Stop debug** **Standby** SPI: normal debug **Normal**

SPI: Standby Debug

(R)

SPI: Stop

(E)

(E)

SPI: standby debug

SPI: Normal Debug

SPI: Stop debug &CSB low to high transition

**Standby Debug** — SPI: Standby debug ← **Normal Debug**

SPI: Normal debug →

(R)

(R)

(1) If stop mode entered, it is entered without watchdog, no matter the WDSTOP bit.

(E) debug mode entry point (step 5 of the debug mode entering sequence).

(R) represents transitions to reset mode due to Vdd1 low.

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## 6 TYPICAL APPLICATIONS
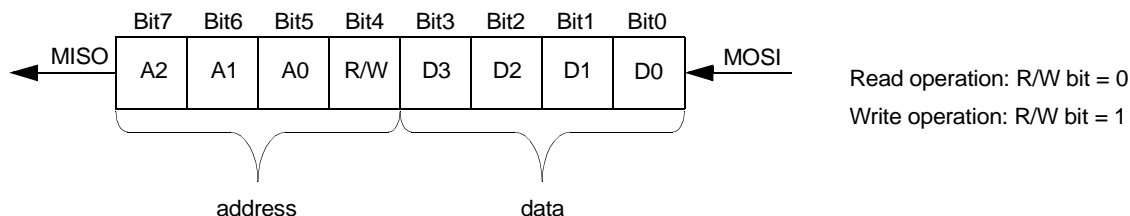
**Fig 1: Simplified typical application with ballast transistor**



**Fig 2: Simplified typical application without ballast transistor**

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## 7    SPI INTERFACE

### 7.1    Data format description

| | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
|---|---|---|---|---|---|---|---|---|---|
| MISO ← | A2 | A1 | A0 | R/W | D3 | D2 | D1 | D0 | ← MOSI |

Read operation: R/W bit = 0

Write operation: R/W bit = 1

address           data

The SPI is a 8 bit SPI. First 3 bits are used to identify the internal SBC register address, bit 4 is a read/write bit. The last 4 bits are data send from MCU to SBC or read back from SBC to MCU.

During write operation state of MISO has no signification.

During read operation only the last 4 bits at MISO have a meaning (content of the accessed register)

Following tables describe the SPI register list, and register bit meaning.

Registers "reset value" is also described, as well as the "reset condition". reset condition is the condition which cause the bit to be set at the "reset value".

Possible reset condition are:

Power On Reset: POR

SBC mode transition:      NR2R - Normal Request to Reset mode

NR2N - Normal Request to Normal mode

N2R - Normal to Reset mode

STB2R - Standby to Reset mode

STO2R - Stop to Reset mode

SBC mode:      RESET - SBC in Reset mode

List of Registers

| Name | Adress | Description | Comment and usage |
|---|---|---|---|
| MCR | $ 0 0 0 | Mode control register | Write: Control of normal, standby, sleep, and stop modes<br>Read: BATFAIL flag and other status bits and flags |
| RCR | $ 0 0 1 | Reset control register | Write: Configuration of reset voltage level, WD in stop mode, low power mode selection<br>        Read: CAN wake up event, Tx permanent dominant |
| CAN | $ 0 1 0 | CAN control register | Write: CAN module control: Tx/Rx, Rec only, term Vbat, Normal and extended modes, filter at L0 input.<br>Read: CAN failure status bits |
| IOR | $ 0 1 1 | I/O control register | Write: HS1 (high side switch) control in normal and standby mode.<br>        Gnd shift register level selection<br>Read: HS1 over temp bit, SHIFT bit (gnd shift above selection), Vsup below 6.1V, V2 below 4V |
| WUR | $ 1 0 0 | Wake up input register | Write: Control of wake up input polarity<br>Read: Wake up input, and real time Lx input state |
| TIM | $ 1 0 1 | Timing register | Write: TIM1, Watchdog timing control, window or Timeout mode.<br>Write: TIM2, Cyclic sense and force wake up timing selection |
| LPC | $ 1 1 0 | Low power mode control register | Write: HS1 periodic activation in sleep and stop modes<br>Force wake up control |
| INTR | $ 1 1 1 | Interrupt register | Write: Interrupt source configuration<br>Read: INT source |

**Table 7-1.**

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## 7.2 Register description

### 7.2.1 MCR Register

| MCR | | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|
| $000b | W | | MCTR2 | MCTR1 | MCTR0 |
| | R | BATFAIL | VDDTEMP | GFAIL | WDRST |
| Reset | | 0 | 0 | 0 | 0 |
| Reset condition | | | POR, RESET | POR, RESET | POR, RESET |

**Table 7-2.**

**Control bits**

| MCTR2 | MCTR1 | MCTR0 | SBC mode | Description |
|---|---|---|---|---|
| 0 | 0 | 0 | Enter/leave debug mode | To enter debug mode, SBC must be in Normal or Standby mode and BATFAIL[1] must be still at 1. To leave debug mode, BATFAIL must be at 0. |
| 0 | 0 | 1 | Normal | |
| 0 | 1 | 0 | Standby | |
| 0 | 1 | 1 | Stop, watchdog off [2] | |
| 0 | 1 | 1 | Stop, watchdog on [2] | |
| 1 | 0 | 0 | Sleep [3] | |
| 1 | 0 | 1 | Normal | |
| 1 | 1 | 0 | Standby | No watchdog running, debug mode |
| 1 | 1 | 1 | Stop | |

(1): Bit BATFAIL cannot be set by SPI. BATFAIL is set when Vsup falls below 3V.
(2): Watchdog ON or OFF depends upon RCR register bit D3.
(3): Before entering sleep mode, bit NOSTOP in RCR register must be previously set to 1.

**Status bits**

| Status bit | Description |
|---|---|
| GFAIL | Logic OR of CAN failure, HS1 failure, V2LOW |
| BATFAIL | Battery fail flag (Vsup<3V) |
| VDDTEMP | Temperature pre-warning on VDD (latched) |
| WDRST | Watchdog reset occurred |

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**7.2.2    RCR register**

| RCR | | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|
| $001b | W | WDSTOP | NOSTOP | | RSTTH |
| | R | | | TXFAILURE | CANWU |
| Reset | | 1 | 0 | | 0 |
| Reset condition | | POR, RESET | POR, NR2N | | POR |

**Table 7-3.**

**Control bits**

| Status bit | Bit value | Description |
|---|---|---|
| WDSTOP | 0 | No watchdog in stop mode |
| | 1 | Watchdog runs in stop mode |
| NOSTOP | 0 | Stop  mode is default low power mode |
| | 1 | Sleep mode is default low power mode |
| RSTTH | 0 | Reset threshold 1 selected (typ 4.6V) |
| | 1 | Reset threshold 2 selected (typ 4.2V) |
| CANWU | 1 | Wake from CAN |
| TXFAILURE | 1 | Tx permanent dominant (CAN) |

**7.2.3    CAN register**
Some description.

| CAN | | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|
| $010b | W | FDIS | CEXT | CCTR1 | CCTR0 |
| | R | CS3 | CS2 | CS1 | CS0 |
| Reset | | 0 | 0 | 0 | 0 |
| Reset condition | | POR, CAN | POR, CAN | POR, CAN | POR, CAN |

**Table 7-4.**

**Fault tolerant CAN transceiver standard modes**
The CAN transceiver standard mode can be programmed by setting CEXT to 0. The transceiver cell will then be behave as known from MC33388.

| CEXT | CCTR1 | CCTR0 | Mode |
|---|---|---|---|
| 0 | 0 | 0 | TermVBAT |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | RxOnly |
| 0 | 1 | 1 | RxTx |

**Table 7-5.**

**Fault tolerant CAN transceiver extended modes**

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By setting CEXT to 1 the transceiver cell supports sub bus communication.

| CEXT | CCTR1 | CCTR0 | Mode |
|------|-------|-------|------|
| 1 | 0 | 0 | TermVBAT |
| 1 | 0 | 1 | TermVDD |
| 1 | 1 | 0 | RxOnly |
| 1 | 1 | 1 | RxTx |

**Table 7-6.**

| FDIS | L0 wake input filter (20us typical) |
|------|-------------------------------------|
| 0 | Enable (LO wake threshold selectable by WUR register) |
| 1 | Disable (L0 wake up threshold is low level only, no matter D0 and D1 bits set in WUR register). |

note: if DFIS bit is set to 1, WUR register must be read before going into sleep or stop mode in order to clear the wake up flag. During read out L0 must be at high level and should stay high when entering sleep or stop.

**Status bits**

| CS3 | CS2 | CS1 | CS0 | Bus failure # | | Description |
|-----|-----|-----|-----|---------------|---|-------------|
| 0 | 0 | 0 | 0 | | no failure | |
| 0 | 0 | 0 | 1 | 1 | CANH open wire | |
| 0 | 1 | 0 | 1 | 5 | CANH short circuit to | ground |
| 0 | 1 | 1 | 0 | 8, 3a | | VDD |
| 0 | 1 | 1 | 1 | 3 | | VBAT |
| 1 | 0 | 0 | 1 | 2 | CANL open wire | |
| 1 | 1 | 0 | 1 | 4, 7 | CANL short circuit to | ground / CANL |
| 1 | 1 | 1 | 0 | 9 | | VDD |
| 1 | 1 | 1 | 1 | 6 | | VBAT |

comments:
CS2 bit at 0 = open failure. CS2 bit at 1 = short failure.
(CS3 bit at 0 and (CS1 = 1 or CS2 =1)) = CANH failure. CS3 bit at 1 = CANL failure.
CS1 and CS0 bits: short type failure coding (gnd, Vdd or Vbat).

In case of multiple failures, the last failure is reported.

### 7.2.4 IOR register
Some description.

| IOR | | D3 | D2 | D1 | D0 |
|-----|---|-----|-----|-----|-----|
| $011b | W | | HS1ON | GSLR1 | GSLR0 |
| | R | SHIFT | HS1OT | V2LOW | VSUPLOW |
| Reset | | | 0 | 0 | 0 |
| Reset condition | | | POR, RESET | POR, RESET | POR, RESET |

**Table 7-7.**

**Control bits**

| HS1ON | HS1 |
|-------|-----|
| 0 | HS1 switch turn OFF |
| 1 | HS1 switch turn ON |

**Table 7-8.**

| GSLR1 | GSLR0 | typical gnd shift comparator level |
|-------|-------|-----------------------------------|
| 0 | 0 | -0.5 V |
| 0 | 1 | -1 V |
| 1 | 0 | -1.5 V |
| 1 | 1 | -2 V |

**Table 7-9. gnd shift selection**

| SHIFT | state |
|-------|-------|
| 0 | Gnd shift value is lower GSLR1 and GSLR2 selection |
| 1 | Gnd shift value is higher GSLR1 and GSLR2 selection |

**Status bits**

| Status bit | Description |
|------------|-------------|
| HS1OT (*) | High side 1 over temperature |
| SHIFT | gnd shift level selected by GSLR1 and GSLR2 bits is reached |
| V2LOW | V2 below 4V typical |
| VSUPLOW | Vsup below 6.1V typical |

(*) Once the HS1 switch has been turned off because of over temperature, it can be turned on again by setting the appropriate control bit to "1".

### 7.2.5    WUR register

The local wake-up inputs L0 and L1 can be used in both normal and standby mode as port expander and for waking up the SBC in sleep or stop mode.

| WUR | | D3 | D2 | D1 | D0 |
|-----|---|-----|-----|-----|-----|
| $100b | W | LCTR3 | LCTR2 | LCTR1 | LCTR0 |
| | R | L1WUb | L1WUa | L0WUb | L0WUa |
| Reset | | 1 | 1 | 1 | 1 |
| Reset condition | | POR, NR2R, N2R, STB2R, STO2R | | | |

**Table 7-10.**

**Control bits:**.

| LCTR3 | LCTR2 | LCTR1 | LCTR0 | L0 configuration | L1 configuration |
|-------|-------|-------|-------|------------------|------------------|
| X | X | 0 | 0 | inputs disabled | |
| X | X | 0 | 1 | high level sensitive | |
| X | X | 1 | 0 | low level sensitive | |
| X | X | 1 | 1 | both level sensitive | |
| 0 | 0 | X | X | | inputs disabled |
| 0 | 1 | X | X | | high level sensitive |
| 1 | 0 | X | X | | low level sensitive |
| 1 | 1 | X | X | | both level sensitive |

**Table 7-11.**

**Status bits:**

| L0WUb | L0WUa | FDIS bit in CAN register | Description |
|-------|-------|--------------------------|-------------|
| 0 | 0 | 0 | No wake up occurred at L0 (sleep or stop mode). Low level state on L0 (standby or normal mode) |
| 1 | 1 | 0 | Wake up occurred at L0 (sleep or stop mode). High level state on L0 (standby or normal mode) |
| 0 | 1 | 1 | Wake up occurred at L0 (sleep or stop mode with L0 filter disable). WUR must be set to xx00 before sleep or stop mode. |

| L1WUb | L1WUa | Description |
|-------|-------|-------------|
| 0 | 0 | No wake up occurred at L1 (sleep or stop mode). Low level state on L1 (standby or normal mode) |
| 1 | 1 | Wake up occurred at L1 (sleep or stop mode). High level state on L1 (standby or normal mode) |

### 7.2.6 TIM registers

Description: This register is splitted into 2 sub registers, TIM1 and TIM2.
TIM1 controls the watchdog timing selection as well as the window or time out option. TIM1 is selected when bit D3 is 0.
TIM2 is used to define the timing for the cyclic sense and forced wake up function. TIM2 is selected when bit D3 is 1.
No read operation is allowed for registers TIM1 and TIM2

### 7.2.7 TIM register

Description.

| TIM1 | | D3 | D2 | D1 | D0 |
|------|---|-----|------|------|------|
| $101b | W | 0 | WDW | WDT1 | WDT0 |
| | R | | | | |

**Table 7-12.**

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| TIM1 | | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|
| Reset | | | 0 | 0 | 0 |
| Reset condition | | | POR, RESET | POR, RESET | POR, RESET |

**Table 7-12.**

Description

| WDW | WDT1 | WDT0 | Watchdog timing [ms] | |
|---|---|---|---|---|
| 0 | 0 | 0 | 10 | no window watchdog |
| 0 | 0 | 1 | 50 | |
| 0 | 1 | 0 | 100 | |
| 0 | 1 | 1 | 350 | |
| 1 | 0 | 0 | 10 | window watchdog enabled (window lenght is half the watchdog timing) |
| 1 | 0 | 1 | 50 | |
| 1 | 1 | 0 | 100 | |
| 1 | 1 | 1 | 350 | |

**Table 7-13.**

**jWatchdog operation (window and time out)**



**Window watchdog**  **Time out watchdog**
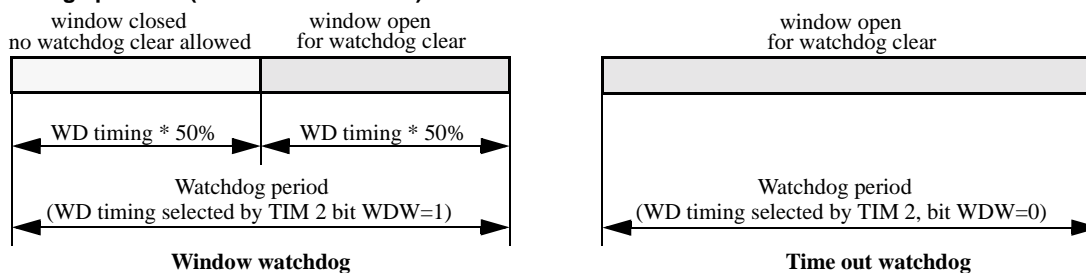
### 7.2.8 TIM2 register

The purpose of TIM2 register is to select an appropriate timing for sensing the wake-up circuitry or cyclically supplying devices by switching on or off HS1

| TIM2 | | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|
| $101b | W | 1 | CSP2 | CSP1 | CSP0 |
| | R | | | | |
| Reset | | | 0 | 0 | 0 |
| Reset condition | | | POR, RESET | POR, RESET | POR, RESET |

**Table 7-14.**

| CSP2 | CSP1 | CSP0 | Cyclic sense timing [ms] |
|---|---|---|---|
| 0 | 0 | 0 | 5 |
| 0 | 0 | 1 | 10 |
| 0 | 1 | 0 | 20 |

**Table 7-15.**

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| CSP2 | CSP1 | CSP0 | Cyclic sense timing [ms] |
|------|------|------|--------------------------|
| 0 | 1 | 1 | 40 |
| 1 | 0 | 0 | 75 |
| 1 | 0 | 1 | 100 |
| 1 | 1 | 0 | 200 |
| 1 | 1 | 1 | 400 |

**Table 7-15.**
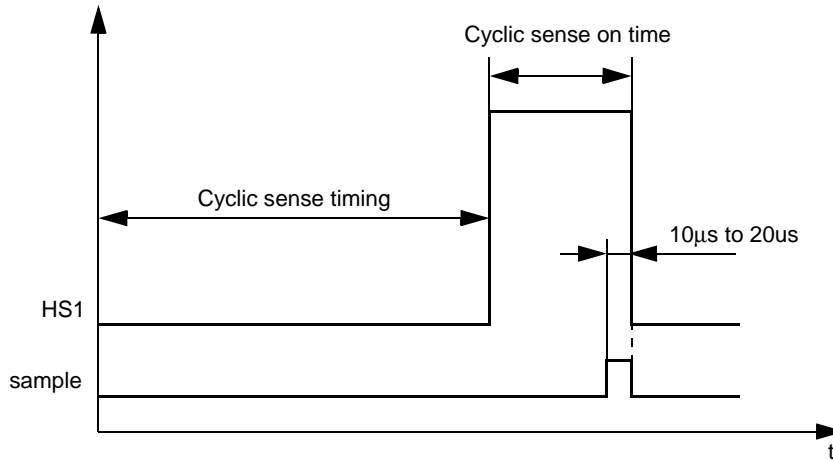


### 7.2.9 LPC register

Description: This register controls:
- The state of HS1 in stop and sleep mode (HS1 permanently off or HS1 cyclic)
- Enable or Disable the forced wake up function (SBC automatic wake up after time spend in sleep or stop mode, time defined by TIM2 register)
- Enable or disable the sense of the wake up inputs (Lx) at sampling point of the cyclic sense period (LX2HS1 bit).

| LPC | | D3 | D2 | D1 | D0 |
|-----|---|----|----|----|----|
| $110b | W | LX2HS1 | FWU | IDDS | HS1AUTO |
| | R | | | | |
| Reset | | 0 | 0 | 0 | 0 |
| Reset condition | | POR, NR2R, N2R, STB2R, STO2R | POR, NR2R, N2R, STB2R, STO2R | POR, NR2R, N2R, STB2R, STO2R | POR, NR2R, N2R, STB2R, STO2R |

**Table 7-16.**

| LX2HS1 | HS1AUTO | Wake-up inputs supplied by HS1 | Autotiming HS1 |
|--------|---------|-------------------------------|----------------|
| X | 0 | | off |
| X | 1 | | on, HS1 cyclic, period defined in TIM2 register |
| 0 | X | no | |
| 1 | X | yes, Lx inputs sensed at sampling point | |

**Table 7-17.**

| Bit | Description |
|---|---|
| FWU | If this bit is set, and the SBC is turned into sleep or stop mode, the SBC wakes up after the time selected in the TIM2 register |
| IDDS | Bit = 0: Idds-wu1 selected (lowest value, typ 3.5mA) <br> Bit = 1: Idds-wu2 selected (highest value, typ 14mA) |

### 7.2.10   INTR register

| INTR | | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|
| $111b | W | VSUPLOW | HS1OT-V2LOW | VDDTEMP | CANF |
| | R | VSUPLOW | HS1OT | VDDTEMP | CANF |
| Reset | | 0 | 0 | 0 | 0 |
| Reset condition | | POR, RESET | POR, RESET | POR, RESET | POR, RESET |

Table 7-18.

**Control bits:**

| Control bit | Description |
|---|---|
| CANF | Mask bit for CAN failures (OR of any CAN failure) |
| VDDTEMP | Mask bit for VDD medium temperature |
| HS1OT-V2LOW | Mask bit for HS1 over temperature OR V2 below 4V |
| VSUPLOW | Mask bit for sup below 6.1V |

**When the mask bit has been set, INTB pin goes low if the appropriate condition occurs.**
**Status bits:**

| Status bit | Description |
|---|---|
| CANF | CAN failure |
| VDDTEMP | VDD medium temperature |
| HS1OT | HS1 over temperature |
| VSUPLOW | Vsup below 6.1V typical |

**Notes:**
If HS1OT-V2LOW interrupt is only selected (only bit D2 set in INTR register), reading INTR register bit D2 leads to two possibilities:
Bit D2 = 1: INT source is HS1OT
Bit D2 = 0: INT source is V2LOW.

Upon a wake up condition from stop mode due to over current detection (Idd1s-wu1 or Idd1s-wu2), an INT pulse is generated, however INTR register contain remains at 0000 (not bit set into the INTR register).

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**CASE OUTLINE**
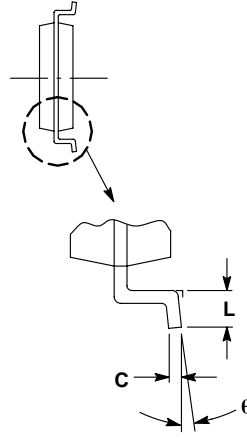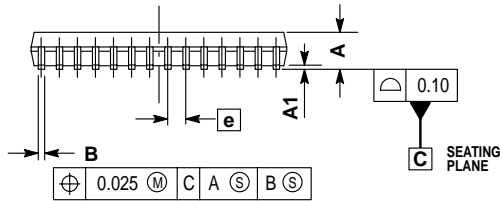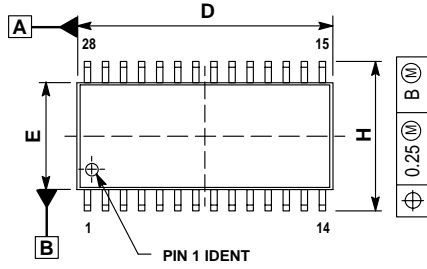
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
4. MAXIMUM MOLD PROTRUSION 0.015 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
|-----|-----|-----|
|     | MIN | MAX |
| A   | 2.35 | 2.65 |
| A1  | 0.13 | 0.29 |
| B   | 0.35 | 0.49 |
| C   | 0.23 | 0.32 |
| D   | 17.80 | 18.05 |
| E   | 7.40 | 7.60 |
| e   | 1.27 BSC | |
| H   | 10.05 | 10.55 |
| L   | 0.41 | 0.90 |
| θ   | 0° | 8° |

**CASE 751F–05**
**ISSUE F**

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