FEATURES

∗0.3 INCH (7.62 mm) DIGIT HEIGHT.
∗FOUR-DIGIT,RIGHT HAND DECIMAL.
∗WIDE SUPPLY VOLTAGE OPERATION.
∗SERIAL DATA INPUT.
∗CONSTANT CURRENT DRIVERS.
∗CONTINUOUS BRIGHTNESS CONTROL.
∗OUTPUT AVAILABLE FOR TWO EXTERNAL LEDS.
∗WIDE VIEWING ANGLE.
∗TTL COMPATIBLE.

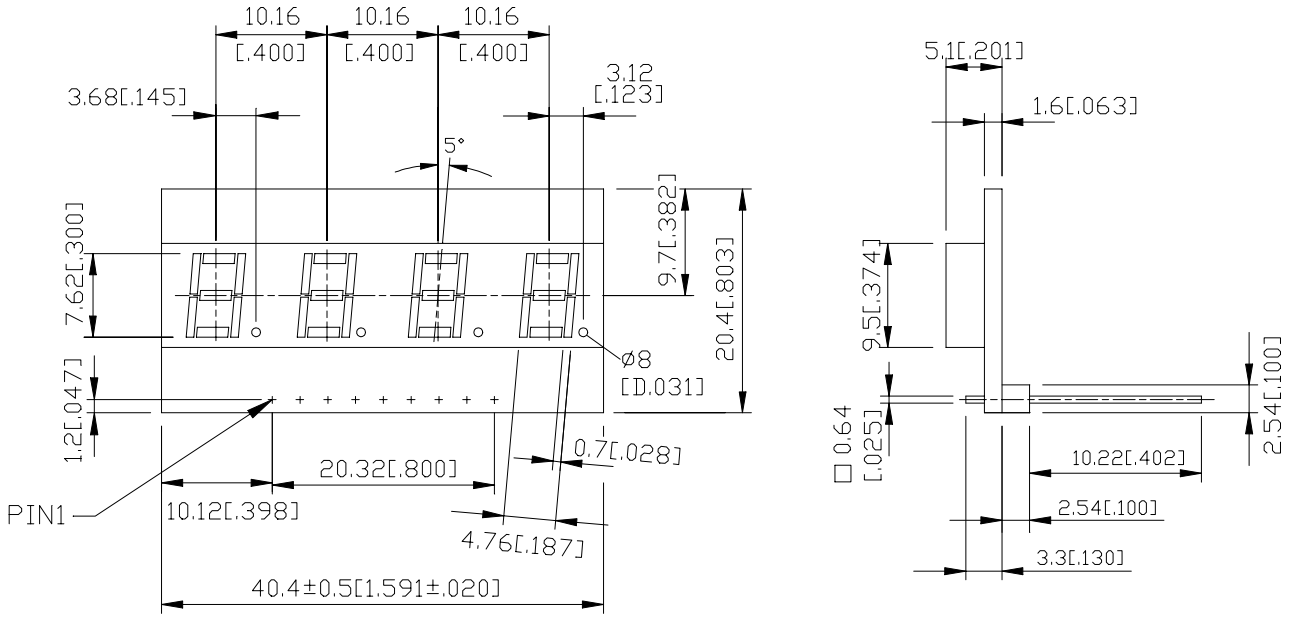
DESCRIPTION

The LTM-8328GKR-04 is a 0.3 inch (7.62mm) digit display. It has a built-in M5450 MOS IC that contains serial data input and 35 bit shift control. The MOS IC produced with N-channel silicon gate technology. This device utilizes bright red LED chips, which are made from GaP on a transparent GaP substrate. Have black face with diffusion tape.

DEVICE

PART NO	DESCRIPTION
GREEN	FOUR DIGIT R.H.D.P,
LTM-8328GKR-04	WITH I.C DRIVER

PACKAGE DIMENSIONS

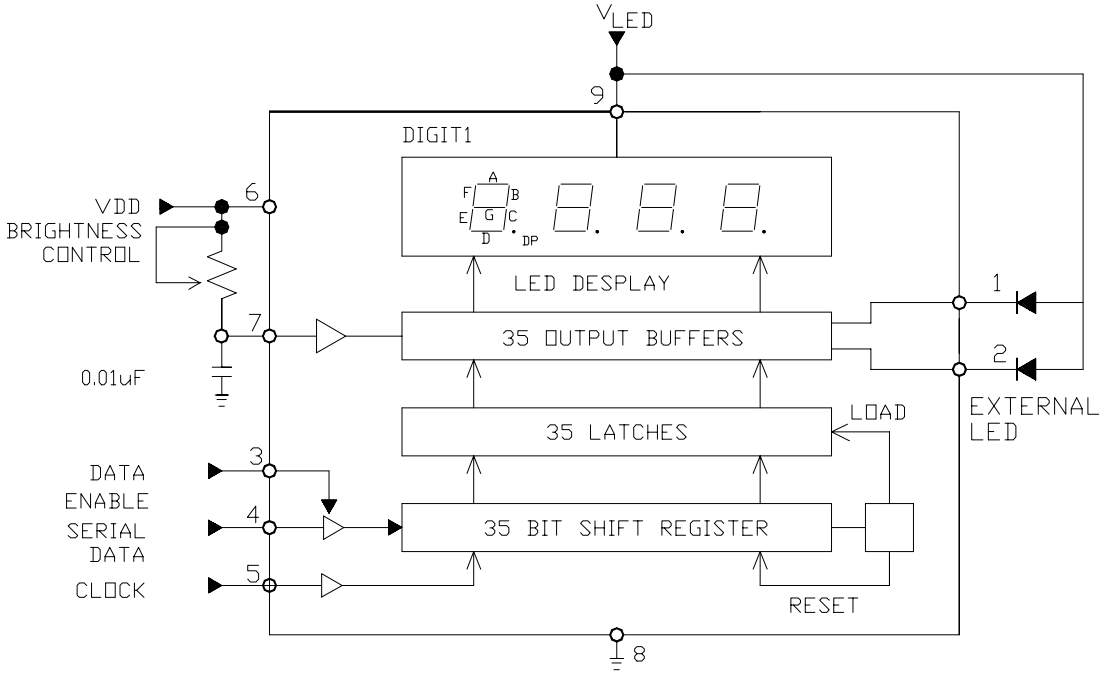


NOTES: All dimensions are in millimeters. Tolerances are ±0.25mm(0.01") unless otherwise noted.

PIN CONNECTION

NO.	CONNECTION	NO.	CONNECTION
1	EXT LED1	6	V_{DD}
2	EXT LED2	7	DIMMER
3	DATA ENABLE	8	GND
4	DATA SERIAL	9	V_{LED}
5	CLOCK		

INTERNAL CIRCUIT DIAGRAM



SERIAL DATA INPUT SEQUENCE

BIT	DIGIT	SEGMENT	BIT	DIGIT	SEGMENT
1	1	A	18	3	B
2	1	B	19	3	C
3	1	C	20	3	D
4	1	D	21	3	E
5	1	E	22	3	F
6	1	F	23	3	G
7	1	G	24	3	DP
8	1	DP	25	4	A
9	2	A	26	4	B
10	2	B	27	4	C
11	2	C	28	4	D
12	2	D	29	4	E
13	2	E	30	4	F
14	2	F	31	4	G
15	2	G	32	4	DP
16	2	DP	33		LED1
17	3	A	34		LED2

ABSOLUTE MAXIMUM RATING AT TA=25°C

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Supply Voltage	V_{DD}	-0.3	12	V
Input Voltage	V_I	-0.3	12	V
Off State Output Voltage	V_O(off)		12	V
LED Supply Voltage	V_{LED}	2.8	3.5	V
Power Dissipation of IC	P_D(IC)		335	mW
Supply Current	I_{DD}		8.5	mA
Operating Temperature Range	T_{OP}	-20	+60	^{0}C
Storage Temperature Range	Tstg	-20	+60	^{0}C
Solder Temperature: 1/16 inch Below Seating Plane for 3 Seconds at 260^{0}C				

NOTE:1.All Voltages are with respect to V_{SS}(GND).

2.Power dissipation of IC is given by P_D =(V_{LED} - V_F) • (I_F) • (NO. of Segments) + (8.5mA) • (V_{DD})

* V_F is LED forward voltage.

RECOMMENDED OPERATING CONDITION AT TA=25°C

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Supply Voltage	V_{DD}	4.75		11	V	
Input Voltage						
Logical "0" Level		-0.3		0.8	V	±10uA Input Bias
Logical "1" Level	V_I	2.2		V_{DD}	V	4.75V< V_{DD}<5.25V
Logical "1" Level		V_{DD}-2		V_{DD}	V	V_{DD} > 5.25V
Brightness Input Current	I_B	0		0.75	mA	
Brightness Input Voltage	V_B	3		4.3	V	Input Current =750uA
Off State Voltage	V_O(off)			11	V	
Ouput Sink Current						
Segment Off				10	uA	IB=0uA
Segment On			3		mA	IB=100uA
			6		mA	IB=200uA
Input Clock Frequency	F_{CLOCK}	0		0.5	MHZ	
Ouput Matching	I_O			±20	%	

ELECTRICAL OPTICAL CHARACTERISTICS AT T_A=25°C

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Average Luminous Intensity	Iv	125	220		ucd	I_B=0.4mA
Peak Emission Wavelength	λp		565		nm	I_B=0.4mA
Spectral Line Half-Width	△λ		30		nm	I_B=0.4mA
Dominant Wavelength	λd		569		nm	I_F=20mA
Luminous Intensity Matching Ratio	Iv-m			2:1		I_B=0.4mA

FUNCTIONAL DESCRIPTION

Serial data transfer from the data source to the display driver is accomplished with 2 signals serial data and clock. Using a format of a leading “1” following by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is completed, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time.

Brightness of display is determined by control the 0utput current of LED display. A 1nF capacitor should be connected to brightness control, Pin 7 to prevent possible oscillations. The output current is typically 25 times greater than the current into Pin 7 which is set by an external variable resistor. There is an internal limiting resistor of 400Ω nominal value.

Figure 1 shows the input data format. A start bit of logical “1” proceed the 35 bits of data. At the 36th clock, a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches. At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configuration. There is no clear for portion of the first register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers won’t clear. When power is first applied to the chip an internal power ON reset signal is generated which reset all registers and all latched. The ATART bit and first clock return the chip on its normal operation. Bit 1 is the first following the start bit and it will appear on the Figure 2 shows the timing relationship between data clock, and DATA ENABLE. A maximum clock frequency of 0.5 MHz is assumed.

FIGURE.1 Input Data Format

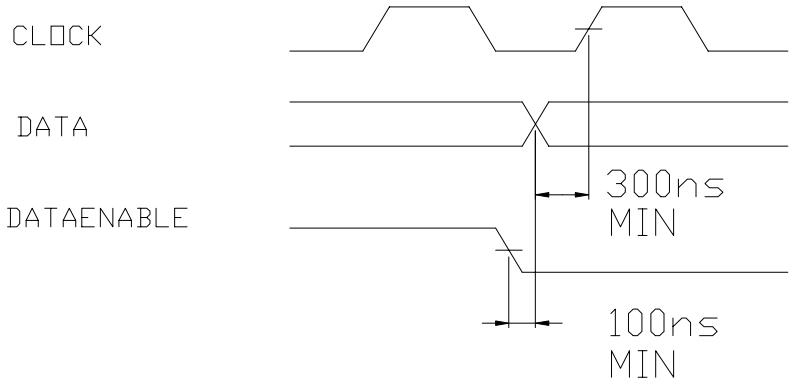
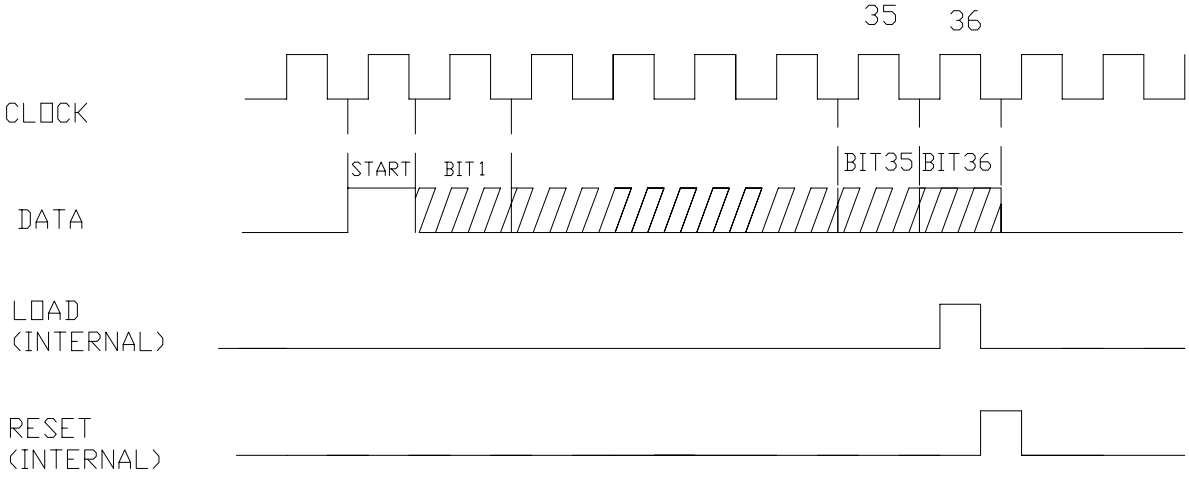



FIGURE.2 Timing Relationship