

## 9-Mbit (256K x 36/512K x 18) Flow-Through SRAM

### Features

- Supports 100, 133 MHz Bus Operations
- Supports 100 MHz Bus Operations (Automotive)
- 256K x 36/512K x 18 Common I/O
- 3.3V -5% and +10% Core Power Supply ( $V_{DD}$ )
- 2.5V or 3.3V I/O Power Supply ( $V_{DDQ}$ )
- Fast Clock-to-Output Times
  - 6.5 ns (133-MHz version)
- Provide High Performance 2-1-1-1 Access Rate
- User-selectable Burst Counter supporting Intel® Pentium® Interleaved or Linear Burst Sequences
- Separate Processor and Controller Address Strokes
- Synchronous Self-timed Write
- Asynchronous Output Enable
- Available in Pb-free 100-Pin TQFP Package, Pb-free and non Pb-free 119-Ball BGA Package, and 165-Ball FBGA Package
- TQFP Available with 3-Chip Enable and 2-Chip Enable
- IEEE 1149.1 JTAG-Compatible Boundary Scan
- "ZZ" Sleep Mode option

### Functional Description

The CY7C1361C/CY7C1363C<sup>[1]</sup> is a 3.3V, 256K x 36/512K x 18 synchronous flow-through SRAMs, respectively designed to interface with high speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 6.5 ns (133 MHz version). A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access. All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining Chip Enable ( $\overline{CE}_1$ ), depth-expansion Chip Enables ( $\overline{CE}_2$  and  $\overline{CE}_3$ <sup>[2]</sup>), Burst Control inputs (ADSC, ADSP, and ADV), Write Enables ( $\overline{BW}_x$  and  $\overline{BWE}$ ), and Global Write ( $\overline{GW}$ ). Asynchronous inputs include the Output Enable ( $\overline{OE}$ ) and the ZZ pin.

The CY7C1361C/CY7C1363C enables either interleaved or linear burst sequences, selected by the MODE input pin. A HIGH selects an interleaved burst sequence, while a LOW selects a linear burst sequence. Burst accesses can be initiated with the Processor Address Strobe (ADSP) or the cache Controller Address Strobe (ADSC) inputs. Address advancement is controlled by the Address Advancement (ADV) input.

Addresses and chip enables are registered at rising edge of clock when either Address Strobe Processor (ADSP) or Address Strobe Controller (ADSC) are active. Subsequent burst addresses can be internally generated as controlled by the Advance pin (ADV).

The CY7C1361C/CY7C1363C operates from a +3.3V core power supply while all outputs may operate with either a +2.5 or +3.3V supply. All inputs and outputs are JEDEC-standard JESD8-5-compatible.

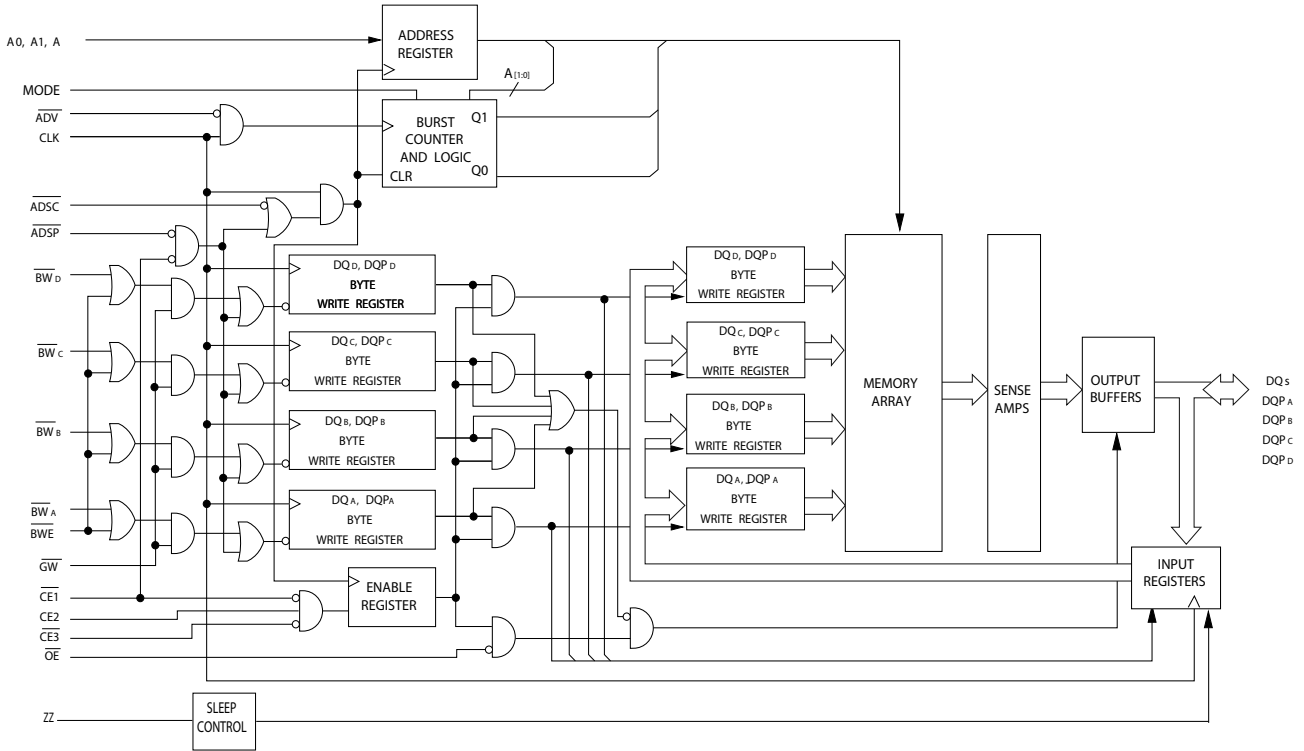
### Selection Guide

Description		133 MHz	100 MHz	Unit
Maximum Access Time		6.5	8.5	ns
Maximum Operating Current		250	180	mA
Maximum CMOS Standby Current	Commercial/ Industrial	40	40	mA
	Automotive		60	mA

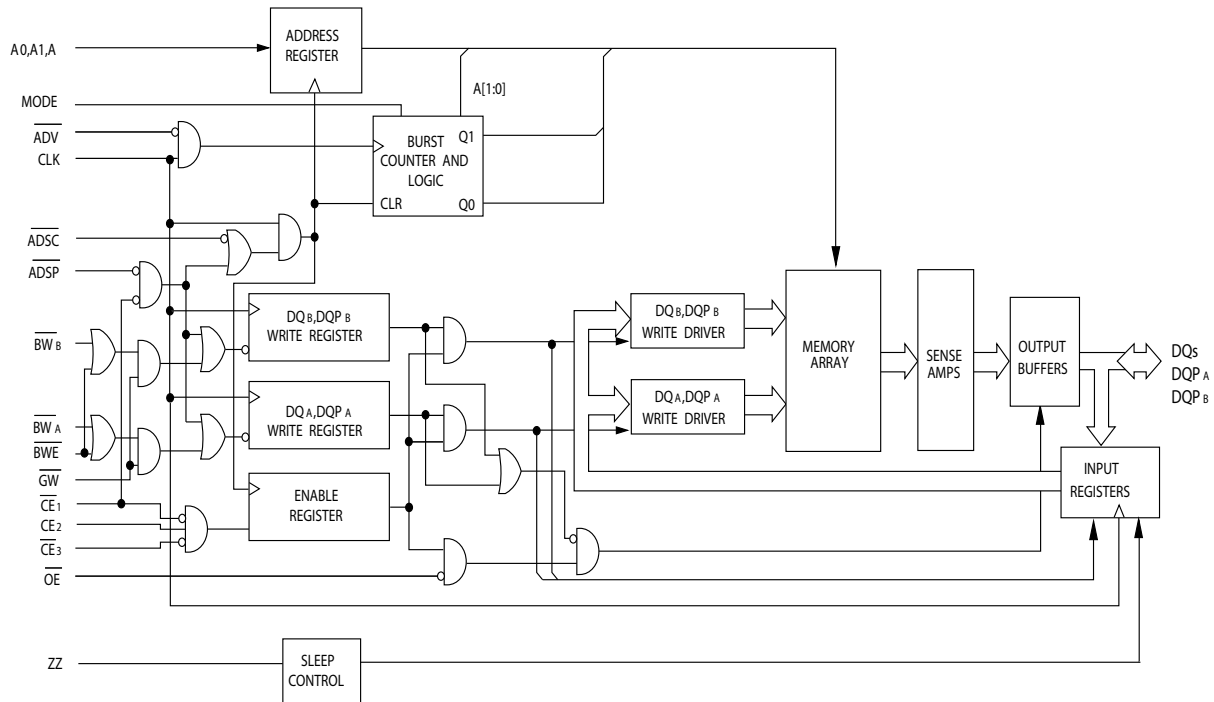
#### Notes

1. For best-practices recommendations, refer to the Cypress application note *System Design Guidelines* on [www.cypress.com](http://www.cypress.com).
2.  $\overline{CE}_3$  is for A version of TQFP (3 Chip Enable Option) and 165 FBGA package only. 119 BGA is offered only in 2 Chip Enable.

Logic Block Diagram – CY7C1361C (256K x 36)



Logic Block Diagram – CY7C1363C (512K x 18)



Pin Configurations

Figure 1. 100-Pin TQFP (3 Chip Enables - A version)

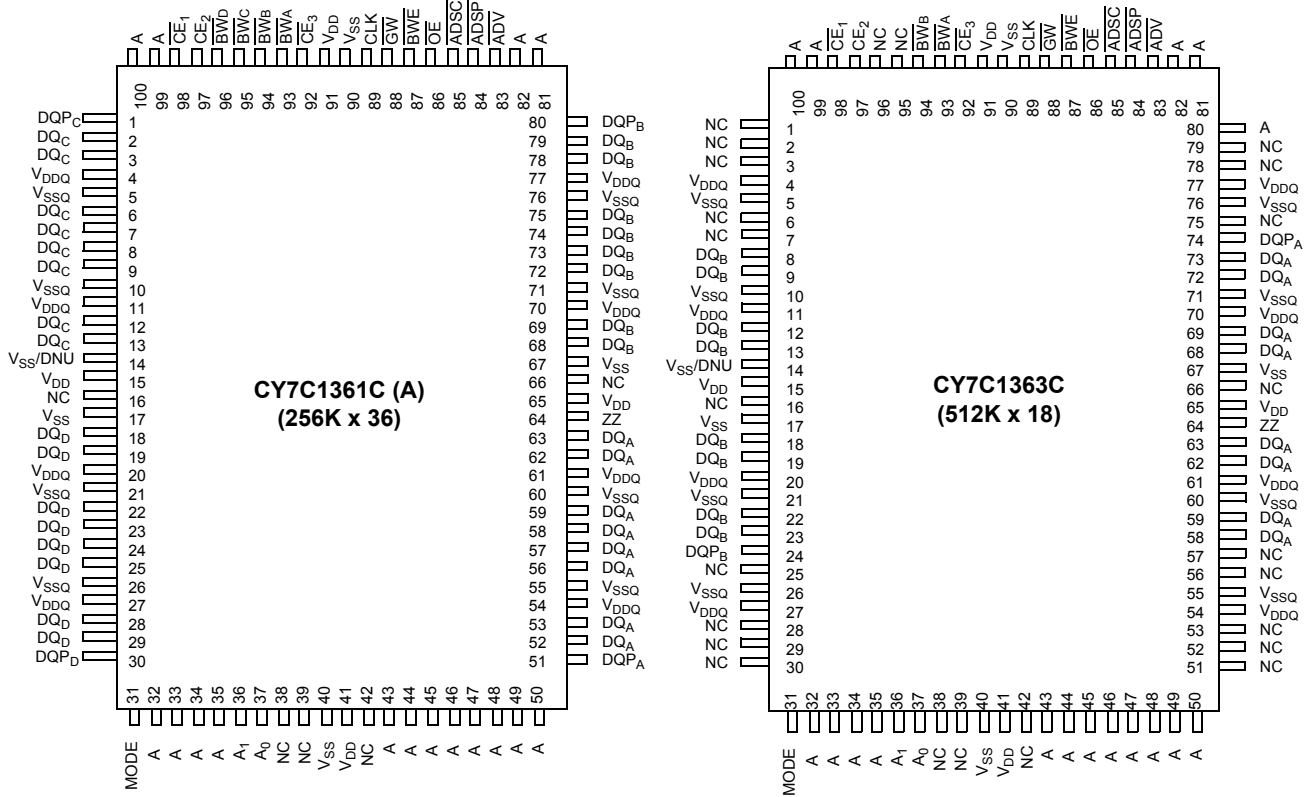
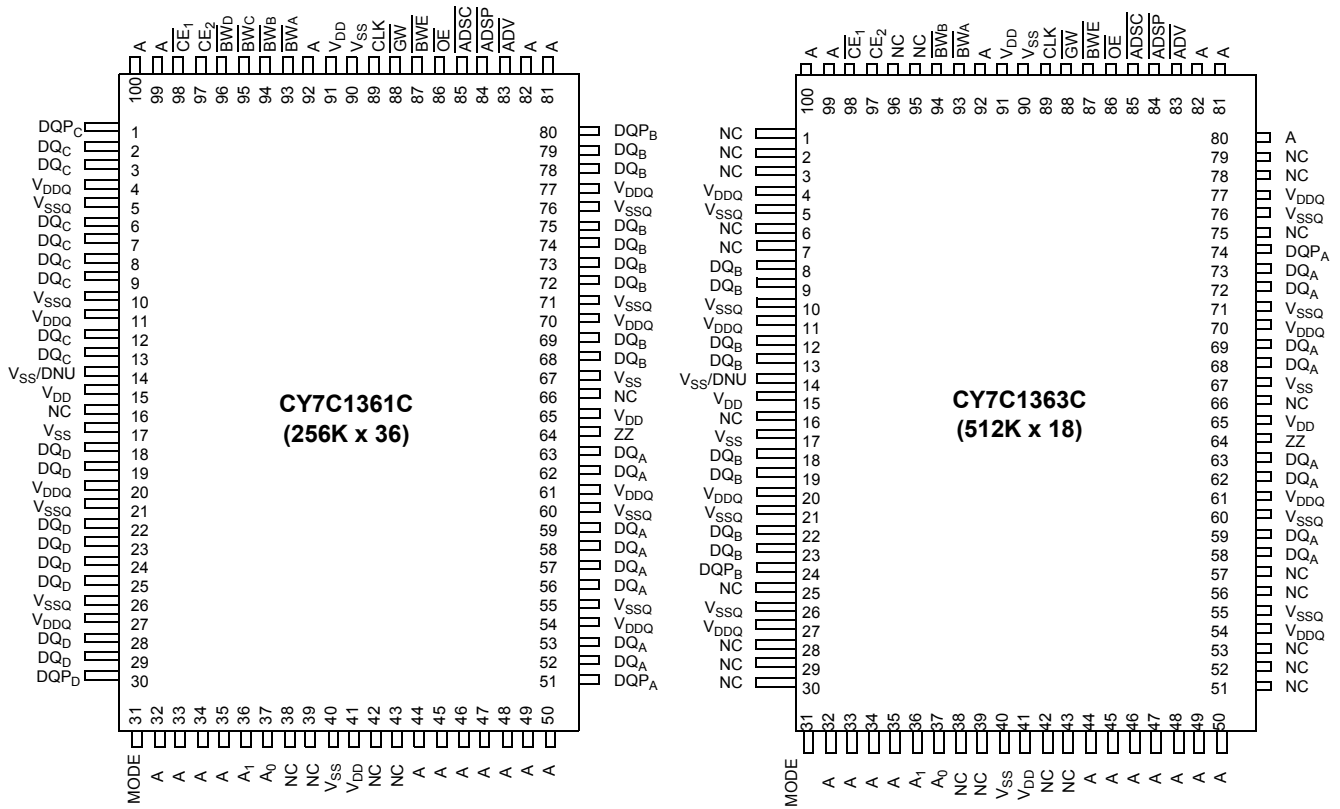


Figure 2. 100-Pin TQFP (2 Chip Enables - AJ Version)



**Figure 3. 100- Ball BGA (2 Chip Enables with JTAG)**
**CY7C1361C (256K x 36)**

	1	2	3	4	5	6	7
<b>A</b>	V <sub>DDQ</sub>	A	A	$\overline{\text{ADSP}}$	A	A	V <sub>DDQ</sub>
<b>B</b>	NC/288M	CE <sub>2</sub>	A	$\overline{\text{ADSC}}$	A	A	NC/512M
<b>C</b>	NC/144M	A	A	V <sub>DD</sub>	A	A	NC/1G
<b>D</b>	DQ <sub>C</sub>	DQP <sub>C</sub>	V <sub>SS</sub>	NC	V <sub>SS</sub>	DQP <sub>B</sub>	DQ <sub>B</sub>
<b>E</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>SS</sub>	$\overline{\text{CE}}_1$	V <sub>SS</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>F</b>	V <sub>DDQ</sub>	DQ <sub>C</sub>	V <sub>SS</sub>	$\overline{\text{OE}}$	V <sub>SS</sub>	DQ <sub>B</sub>	V <sub>DDQ</sub>
<b>G</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	$\overline{\text{BW}}_C$	$\overline{\text{ADV}}$	$\overline{\text{BW}}_B$	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>H</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>SS</sub>	$\overline{\text{GW}}$	V <sub>SS</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>J</b>	V <sub>DDQ</sub>	V <sub>DD</sub>	NC	V <sub>DD</sub>	NC	V <sub>DD</sub>	V <sub>DDQ</sub>
<b>K</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>SS</sub>	CLK	V <sub>SS</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>L</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	$\overline{\text{BW}}_D$	NC	$\overline{\text{BW}}_A$	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>M</b>	V <sub>DDQ</sub>	DQ <sub>D</sub>	V <sub>SS</sub>	$\overline{\text{BWE}}$	V <sub>SS</sub>	DQ <sub>A</sub>	V <sub>DDQ</sub>
<b>N</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>SS</sub>	A1	V <sub>SS</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>P</b>	DQ <sub>D</sub>	DQP <sub>D</sub>	V <sub>SS</sub>	A0	V <sub>SS</sub>	DQP <sub>A</sub>	DQ <sub>A</sub>
<b>R</b>	NC	A	MODE	V <sub>DD</sub>	NC	A	NC
<b>T</b>	NC	NC/72M	A	A	A	NC/36M	ZZ
<b>U</b>	V <sub>DDQ</sub>	TMS	TDI	TCK	TDO	NC	V <sub>DDQ</sub>

**CY7C1363C (512K x 18)**

	1	2	3	4	5	6	7
<b>A</b>	V <sub>DDQ</sub>	A	A	$\overline{\text{ADSP}}$	A	A	V <sub>DDQ</sub>
<b>B</b>	NC/288M	CE <sub>2</sub>	A	$\overline{\text{ADSC}}$	A	A	NC/512M
<b>C</b>	NC/144M	A	A	V <sub>DD</sub>	A	A	NC/1G
<b>D</b>	DQ <sub>B</sub>	NC	V <sub>SS</sub>	NC	V <sub>SS</sub>	DQP <sub>A</sub>	NC
<b>E</b>	NC	DQ <sub>B</sub>	V <sub>SS</sub>	$\overline{\text{CE}}_1$	V <sub>SS</sub>	NC	DQ <sub>A</sub>
<b>F</b>	V <sub>DDQ</sub>	NC	V <sub>SS</sub>	$\overline{\text{OE}}$	V <sub>SS</sub>	DQ <sub>A</sub>	V <sub>DDQ</sub>
<b>G</b>	NC	DQ <sub>B</sub>	$\overline{\text{BW}}_B$	$\overline{\text{ADV}}$	V <sub>SS</sub>	NC	DQ <sub>A</sub>
<b>H</b>	DQ <sub>B</sub>	NC	V <sub>SS</sub>	$\overline{\text{GW}}$	V <sub>SS</sub>	DQ <sub>A</sub>	NC
<b>J</b>	V <sub>DDQ</sub>	V <sub>DD</sub>	NC	V <sub>DD</sub>	NC	V <sub>DD</sub>	V <sub>DDQ</sub>
<b>K</b>	NC	DQ <sub>B</sub>	V <sub>SS</sub>	CLK	V <sub>SS</sub>	NC	DQ <sub>A</sub>
<b>L</b>	DQ <sub>B</sub>	NC	V <sub>SS</sub>	NC	$\overline{\text{BW}}_A$	DQ <sub>A</sub>	NC
<b>M</b>	V <sub>DDQ</sub>	DQ <sub>B</sub>	V <sub>SS</sub>	$\overline{\text{BWE}}$	V <sub>SS</sub>	NC	V <sub>DDQ</sub>
<b>N</b>	DQ <sub>B</sub>	NC	V <sub>SS</sub>	A1	V <sub>SS</sub>	DQ <sub>A</sub>	NC
<b>P</b>	NC	DQP <sub>B</sub>	V <sub>SS</sub>	A0	V <sub>SS</sub>	NC	DQ <sub>A</sub>
<b>R</b>	NC	A	MODE	V <sub>DD</sub>	NC	A	NC
<b>T</b>	NC/72M	A	A	NC/36M	A	A	ZZ
<b>U</b>	V <sub>DDQ</sub>	TMS	TDI	TCK	TDO	NC	V <sub>DDQ</sub>

**Figure 4. 165-Ball FBGA (3 Chip Enable)**
**CY7C1361C (256K x 36)**

	1	2	3	4	5	6	7	8	9	10	11
<b>A</b>	NC/288M	A	$\overline{CE}_1$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{CE}_3$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	NC
<b>B</b>	NC/144M	A	$CE_2$	$\overline{BW}_D$	$\overline{BW}_A$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC/576M
<b>C</b>	DQP <sub>C</sub>	NC	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC/1G	DQP <sub>B</sub>
<b>D</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>E</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>F</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>G</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>H</b>	NC	V <sub>SS</sub>	NC	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	NC	NC	ZZ
<b>J</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>K</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>L</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>M</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>N</b>	DQP <sub>D</sub>	NC	V <sub>DDQ</sub>	V <sub>SS</sub>	NC	NC/18M	NC	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	DQP <sub>A</sub>
<b>P</b>	NC	NC/72M	A	A	TDI	A1	TDO	A	A	A	A
<b>R</b>	MODE	NC/36M	A	A	TMS	A0	TCK	A	A	A	A

**CY7C1363C (512K x 18)**

	1	2	3	4	5	6	7	8	9	10	11
<b>A</b>	NC/288M	A	$\overline{CE}_1$	$\overline{BW}_B$	NC	$\overline{CE}_3$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	A
<b>B</b>	NC/144M	A	$CE_2$	NC	$\overline{BW}_A$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC/576M
<b>C</b>	NC	NC	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC/1G	DQP <sub>A</sub>
<b>D</b>	NC	DQ <sub>B</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	DQ <sub>A</sub>
<b>E</b>	NC	DQ <sub>B</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	DQ <sub>A</sub>
<b>F</b>	NC	DQ <sub>B</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	DQ <sub>A</sub>
<b>G</b>	NC	DQ <sub>B</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	DQ <sub>A</sub>
<b>H</b>	V <sub>SS</sub>	V <sub>SS</sub>	NC	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	NC	NC	ZZ
<b>J</b>	DQ <sub>B</sub>	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	NC
<b>K</b>	DQ <sub>B</sub>	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	NC
<b>L</b>	DQ <sub>B</sub>	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	NC
<b>M</b>	DQ <sub>B</sub>	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	NC
<b>N</b>	DQP <sub>B</sub>	NC	V <sub>DDQ</sub>	V <sub>SS</sub>	NC	NC/18M	NC	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	NC
<b>P</b>	NC	NC/72M	A	A	TDI	A1	TDO	A	A	A	A
<b>R</b>	MODE	NC/36M	A	A	TMS	A0	TCK	A	A	A	A

**Pin Definitions**

Name	I/O	Description
A <sub>0</sub> , A <sub>1</sub> , A	Input-Synchronous	<b>Address Inputs used to select one of the address locations.</b> Sampled at the rising edge of the CLK if ADSP or ADSC is active LOW, and CE <sub>1</sub> , CE <sub>2</sub> , and CE <sub>3</sub> <sup>[2]</sup> are sampled active. A <sub>[1:0]</sub> feed the 2-bit counter.
BW <sub>A</sub> , BW <sub>B</sub> BW <sub>C</sub> , BW <sub>D</sub>	Input-Synchronous	<b>Byte Write Select Inputs, active LOW.</b> Qualified with BWE to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
GW	Input-Synchronous	<b>Global Write Enable Input, active LOW.</b> When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on BW <sub>X</sub> and BWE).
CLK	Input-Clock	<b>Clock Input.</b> Used to capture all synchronous inputs to the device. Also used to increment the burst counter when ADV is asserted LOW, during a burst operation.
CE <sub>1</sub>	Input-Synchronous	<b>Chip Enable 1 Input, active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with CE <sub>2</sub> and CE <sub>3</sub> <sup>[2]</sup> to select/deselect the device. ADSP is ignored if CE <sub>1</sub> is HIGH. CE <sub>1</sub> is sampled only when a new external address is loaded.
CE <sub>2</sub>	Input-Synchronous	<b>Chip Enable 2 Input, active HIGH.</b> Sampled on the rising edge of CLK. Used in conjunction with CE <sub>1</sub> and CE <sub>3</sub> <sup>[2]</sup> to select/deselect the device. CE <sub>2</sub> is sampled only when a new external address is loaded.
CE <sub>3</sub> <sup>[2]</sup>	Input-Synchronous	<b>Chip Enable 3 Input, active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with CE <sub>1</sub> and CE <sub>2</sub> to select/deselect the device. CE <sub>3</sub> is sampled only when a new external address is loaded.
OE	Input-Asynchronous	<b>Output Enable, asynchronous input, active LOW.</b> Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins. OE is masked during the first clock of a read cycle when emerging from a deselected state.
ADV	Input-Synchronous	<b>Advance Input signal, sampled on the rising edge of CLK.</b> When asserted, it automatically increments the address in a burst cycle.
ADSP	Input-Synchronous	<b>Address Strobe from Processor, sampled on the rising edge of CLK, active LOW.</b> When asserted LOW, addresses presented to the device are captured in the address registers. A <sub>[1:0]</sub> are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized. ADSP is ignored when CE <sub>1</sub> is deasserted HIGH.
ADSC	Input-Synchronous	<b>Address Strobe from Controller, sampled on the rising edge of CLK, active LOW.</b> When asserted LOW, addresses presented to the device are captured in the address registers. A <sub>[1:0]</sub> are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized.
BWE	Input-Synchronous	<b>Byte Write Enable Input, active LOW.</b> Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
ZZ	Input-Asynchronous	<b>ZZ “sleep” Input, active HIGH.</b> When asserted HIGH places the device in a non-time-critical “sleep” condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull down.
DQ <sub>s</sub>	I/O-Synchronous	<b>Bidirectional Data I/O lines.</b> As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by OE. When OE is asserted LOW, the pins behave as outputs. When HIGH, DQ <sub>s</sub> and DQP <sub>X</sub> are placed in a tristate condition. The outputs are automatically tristated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of OE.
DQP <sub>X</sub>	I/O-Synchronous	<b>Bidirectional Data Parity I/O Lines.</b> Functionally, these signals are identical to DQ <sub>s</sub> . During write sequences, DQP <sub>X</sub> is controlled by BW <sub>X</sub> correspondingly.
MODE	Input-Static	<b>Selects Burst Order.</b> When tied to GND selects linear burst sequence. When tied to V <sub>DD</sub> or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode Pin has an internal pull up.
V <sub>DD</sub>	Power Supply	<b>Power supply inputs to the core of the device.</b>

**Pin Definitions** (continued)

Name	I/O	Description
V <sub>DDQ</sub>	I/O Power Supply	<b>Power supply for the I/O circuitry.</b>
V <sub>SS</sub>	Ground	<b>Ground for the core of the device.</b>
V <sub>SSQ</sub>	I/O Ground	<b>Ground for the I/O circuitry.</b>
TDO	JTAG serial output Synchronous	<b>Serial data-out to the JTAG circuit.</b> Delivers data on the negative edge of TCK. If the JTAG feature is not being used, this pin should be left unconnected. This pin is not available on TQFP packages.
TDI	JTAG serial input Synchronous	<b>Serial data-In to the JTAG circuit.</b> Sampled on the rising edge of TCK. If the JTAG feature is not being used, this pin can be left floating or connected to V <sub>DD</sub> through a pull up resistor. This pin is not available on TQFP packages.
TMS	JTAG serial input Synchronous	<b>Serial data-In to the JTAG circuit.</b> Sampled on the rising edge of TCK. If the JTAG feature is not being used, this pin can be disconnected or connected to V <sub>DD</sub> . This pin is not available on TQFP packages.
TCK	JTAG- Clock	<b>Clock input to the JTAG circuitry.</b> If the JTAG feature is not being used, this pin must be connected to V <sub>SS</sub> . This pin is not available on TQFP packages.
NC	–	<b>No Connects.</b> Not internally connected to the die. 18M, 36M, 72M, 144M, 288M, 576M, and 1G are address expansion pins and are not internally connected to the die.
V <sub>SS</sub> /DNU	Ground/DNU	This pin can be connected to Ground or should be left floating.



## Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. Maximum access delay from the clock rise ( $t_{CDV}$ ) is 6.5 ns (133 MHz device).

The CY7C1361C/CY7C1363C supports secondary cache in systems using either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486™ processors. The linear burst sequence is suited for processors that use a linear burst sequence. The burst order is user-selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the Processor Address Strobe (ADSP) or the Controller Address Strobe (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the Byte Write Enable (BWE) and Byte Write Select ( $\overline{BW}_X$ ) inputs. A Global Write Enable (GW) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Selects ( $\overline{CE}_1$ ,  $CE_2$ ,  $\overline{CE}_3^{[2]}$ ) and an asynchronous Output Enable ( $\overline{OE}$ ) provide for easy bank selection and output tristate control. ADSP is ignored if  $CE_1$  is HIGH.

### Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1)  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{CE}_3^{[2]}$  are all asserted active and (2) ADSP or ADSC is asserted LOW (if the access is initiated by ADSC, the write inputs must be deasserted during this first cycle). The address presented to the address inputs is latched into the address register and the burst counter/control logic and presented to the memory core. If the  $\overline{OE}$  input is asserted LOW, the requested data will be available at the data outputs a maximum to  $t_{CDV}$  after clock rise. ADSP is ignored if  $CE_1$  is HIGH.

### Single Write Accesses Initiated by ADSP

This access is initiated when the following conditions are satisfied at clock rise: (1)  $\overline{CE}_1$ ,  $CE_2$ ,  $\overline{CE}_3^{[2]}$  are all asserted active and (2) ADSP is asserted LOW. The addresses presented are loaded into the address register and the burst inputs ( $\overline{GW}$ , BWE, and  $\overline{BW}_X$ ) are ignored during this first clock cycle. If the write inputs are asserted active (see [Partial Truth Table for Read/Write](#) on page 11 for appropriate states that indicate a write) on the next clock rise, the appropriate data will be latched and written into the device. Byte writes are allowed. All I/Os are tristated during a byte write. Since this is a common I/O device, the asynchronous OE input signal must be deasserted and the I/Os must be tristated prior to the presentation of data to DQs. As a safety precaution, the data lines are tristated once a write cycle is detected, regardless of the state of OE.

### Single Write Accesses Initiated by $\overline{ADSC}$

This write access is initiated when the following conditions are satisfied at clock rise: (1)  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{CE}_3^{[2]}$  are all asserted active, (2)  $\overline{ADSC}$  is asserted LOW, (3)  $\overline{ADSP}$  is deasserted HIGH, and (4) the write input signals ( $\overline{GW}$ , BWE, and  $\overline{BW}_X$ ) indicate a write access. ADSC is ignored if ADSP is active LOW.

The addresses presented are loaded into the address register and the burst counter/control logic and delivered to the memory core. The information presented to  $DQ_{[A:D]}$  is written into the specified address location. Byte writes are allowed. All I/Os are tristated when a write is detected, even a byte write. Since this is a common I/O device, the asynchronous  $\overline{OE}$  input signal must be deasserted and the I/Os must be tristated prior to the presentation of data to  $DQ_s$ . As a safety precaution, the data lines are tristated once a write cycle is detected, regardless of the state of  $\overline{OE}$ .

## Burst Sequences

The CY7C1361C/CY7C1363C provides an on-chip two-bit wraparound burst counter inside the SRAM. The burst counter is fed by  $A_{[1:0]}$ , and can follow either a linear or interleaved burst order. The burst order is determined by the state of the MODE input. A LOW on MODE will select a linear burst sequence. A HIGH on MODE selects an interleaved burst order. Leaving MODE unconnected causes the device to default to a interleaved burst sequence.

**Table 1. Interleaved Burst Address Table (MODE = Floating or  $V_{DD}$ )**

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

**Table 2. Linear Burst Address Table (MODE = GND)**

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

### Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation 'sleep' mode. Two clock cycles are required to enter into or exit from this 'sleep' mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the 'sleep' mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the 'sleep' mode.  $\overline{CE}_1$ ,  $CE_2$ ,  $\overline{CE}_3^{[2]}$ , ADSP, and ADSC must remain inactive for the duration of  $t_{ZZREC}$  after the ZZ input returns LOW.

### ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions		Min	Max	Unit
I <sub>DDZZ</sub>	Sleep mode standby current	ZZ ≥ V <sub>DD</sub> - 0.2V	Comm/ind'l		50	mA
			Automotive		60	mA
t <sub>ZZS</sub>	Device operation to ZZ	ZZ ≥ V <sub>DD</sub> - 0.2V			2t <sub>CYC</sub>	ns
t <sub>ZZREC</sub>	ZZ recovery time	ZZ ≤ 0.2V		2t <sub>CYC</sub>		ns
t <sub>ZZI</sub>	ZZ active to sleep current	This parameter is sampled			2t <sub>CYC</sub>	ns
t <sub>RZZI</sub>	ZZ Inactive to exit sleep current	This parameter is sampled		0		ns

### Truth Table

The Truth Table for CY7C1361C and CY7C1363C follows. [3, 4, 5, 6, 7]

Cycle Description	Address Used	$\overline{CE}_1$	CE <sub>2</sub>	$\overline{CE}_3$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power Down	None	H	X	X	L	X	L	X	X	X	L-H	Tristate
Deselected Cycle, Power Down	None	L	L	X	L	L	X	X	X	X	L-H	Tristate
Deselected Cycle, Power Down	None	L	X	H	L	L	X	X	X	X	L-H	Tristate
Deselected Cycle, Power Down	None	L	L	X	L	H	L	X	X	X	L-H	Tristate
Deselected Cycle, Power Down	None	X	X	X	L	H	L	X	X	X	L-H	Tristate
Sleep Mode, Power-down	None	X	X	X	H	X	X	X	X	X	X	Tristate
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	L	L-H	Q
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	H	L-H	Tristate
Write Cycle, Begin Burst	External	L	H	L	L	H	L	X	L	X	L-H	D
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	L	L-H	Q
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	H	L-H	Tristate
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	Tristate
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	Tristate
Write Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
Write Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	Tristate
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	Tristate
Write Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

**Notes**

- X="Don't Care." H = Logic HIGH, L = Logic LOW.
- $\overline{WRITE}$  = L when any one or more Byte Write enable signals and  $\overline{BWE}$  = L or  $\overline{GW}$  = L.  $\overline{WRITE}$  = H when all Byte write enable signals,  $\overline{BWE}$ ,  $\overline{GW}$  = H.
- The DQ pins are controlled by the current cycle and the OE signal. OE is asynchronous and is not sampled with the clock.
- The SRAM always initiates a read cycle when ADSP is asserted, regardless of the state of GW, BWE, or BW<sub>x</sub>. Writes may occur only on subsequent clocks after the ADSP or with the assertion of ADSC. As a result, OE must be driven HIGH prior to the start of the write cycle to allow the outputs to tri-state. OE is a don't care for the remainder of the write cycle.
- OE is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tri-state when OE is inactive or when the device is deselected, and all data bits behave as output when OE is active (LOW).

### Partial Truth Table for Read/Write

The Partial Truth Table for Read/Write follows.<sup>[3, 8]</sup>

Function (CY7C1361C)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_D}$	$\overline{BW_C}$	$\overline{BW_B}$	$\overline{BW_A}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte (A, DQP <sub>A</sub> )	H	L	H	H	H	L
Write Byte (B, DQP <sub>B</sub> )	H	L	H	H	L	H
Write Bytes (B, A, DQP <sub>A</sub> , DQP <sub>B</sub> )	H	L	H	H	L	L
Write Byte (C, DQP <sub>C</sub> )	H	L	H	L	H	H
Write Bytes (C, A, DQP <sub>C</sub> , DQP <sub>A</sub> )	H	L	H	L	H	L
Write Bytes (C, B, DQP <sub>C</sub> , DQP <sub>B</sub> )	H	L	H	L	L	H
Write Bytes (C, B, A, DQP <sub>C</sub> , DQP <sub>B</sub> , DQP <sub>A</sub> )	H	L	H	L	L	L
Write Byte (D, DQP <sub>D</sub> )	H	L	L	H	H	H
Write Bytes (D, A, DQP <sub>D</sub> , DQP <sub>A</sub> )	H	L	L	H	H	L
Write Bytes (D, B, DQP <sub>D</sub> , DQP <sub>B</sub> )	H	L	L	H	L	H
Write Bytes (D, B, A, DQP <sub>D</sub> , DQP <sub>B</sub> , DQP <sub>A</sub> )	H	L	L	H	L	L
Write Bytes (D, B, DQP <sub>D</sub> , DQP <sub>B</sub> )	H	L	L	L	H	H
Write Bytes (D, B, A, DQP <sub>D</sub> , DQP <sub>C</sub> , DQP <sub>A</sub> )	H	L	L	L	H	L
Write Bytes (D, C, A, DQP <sub>D</sub> , DQP <sub>B</sub> , DQP <sub>A</sub> )	H	L	L	L	L	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

### Truth Table for Read/Write

The Truth Table for Read/Write follows.<sup>[3, 8]</sup>

Function (CY7C1363C)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_B}$	$\overline{BW_A}$
Read	H	H	X	X
Read	H	L	H	H
Write Byte A – (DQ <sub>A</sub> and DQP <sub>A</sub> )	H	L	H	L
Write Byte B – (DQ <sub>B</sub> and DQP <sub>B</sub> )	H	L	L	H
Write All Bytes	H	L	L	L
Write All Bytes	L	X	X	X

**Note**

8. Table only lists a partial listing of the byte write combinations. Any Combination of  $\overline{BW_X}$  is valid Appropriate write will be done based on which byte write is active.

### IEEE 1149.1 Serial Boundary Scan (JTAG)

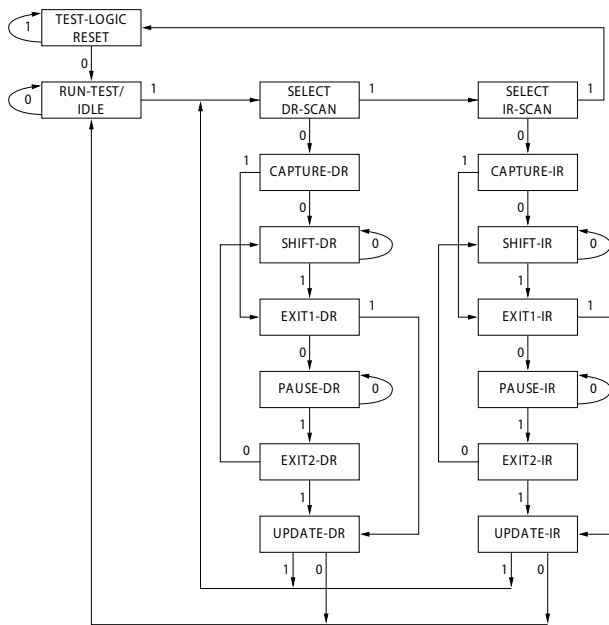
The CY7C1361C/CY7C1363C incorporates a serial boundary scan test access port (TAP) in the BGA package only. The TQFP package does not offer this functionality. This part operates in accordance with IEEE Standard 1149.1-1900, but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC-standard 3.3V or 2.5V I/O logic levels.

The CY7C1361C/CY7C1363C contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

### Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW ( $V_{SS}$ ) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to  $V_{DD}$  through a pull up resistor. TDO should be left unconnected. Upon power up, the device comes up in a reset state which does not interfere with the operation of the device.

### TAP Controller State Diagram



The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

### Test Access Port (TAP)

#### Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

#### Test MODE SELECT (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

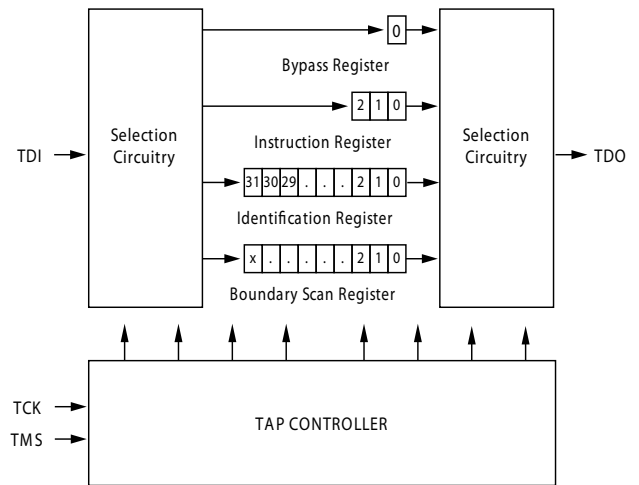
#### Test Data-In (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register. (See [TAP Controller Block Diagram](#).)

#### Test Data-Out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. (See [TAP Controller State Diagram](#).)

### TAP Controller Block Diagram



## Performing a TAP Reset

A RESET is performed by forcing TMS HIGH ( $V_{DD}$ ) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

## TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

### Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the [TAP Controller Block Diagram](#) on page 12. Upon power up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary '01' pattern to enable fault isolation of the board-level serial test data path.

### Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This enables data to be shifted through the SRAM with minimal delay. The bypass register is set LOW ( $V_{SS}$ ) when the BYPASS instruction is executed.

### Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The [119-Ball BGA Boundary Scan Order](#) on page 18 and [165-Ball FBGA Boundary Scan Order](#) on page 19 show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI and the LSB is connected to TDO.

### Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in [Identification Register Definitions](#) on page 16.

## TAP Instruction Set

### Overview

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail in this section.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented.

The TAP controller cannot be used to load address data or control signals into the SRAM and cannot preload the I/O buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather, it performs a capture of the I/O ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

### EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in this SRAM TAP controller, and therefore this device is not compliant to 1149.1. The TAP controller does recognize an all-0 instruction.

When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

### IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and enables the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register upon power up or whenever the TAP controller is given a test logic reset state.

### SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

### SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1-mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output undergoes a transition (metastable state). This does not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times ( $t_{CS}$  and  $t_{CH}$ ). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD enables an initial data pattern to be placed at the latched parallel outputs of the boundary scan register cells prior to the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required - that is, while data captured is shifted out, the preloaded data can be shifted in.

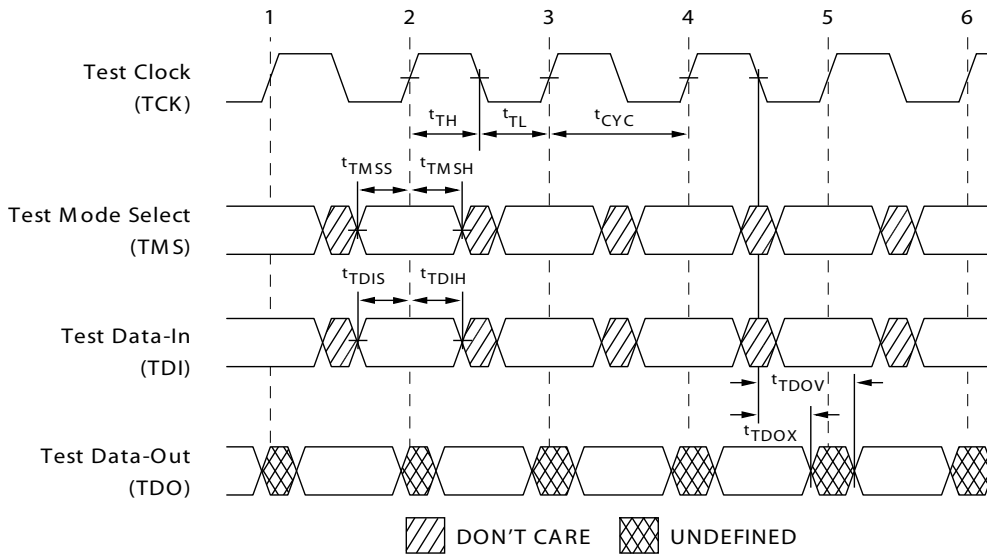
**BYPASS**

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO balls. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

**Reserved**

These instructions are not implemented but are reserved for future use. Do not use these instructions.

**TAP Timing**



**TAP AC Switching Characteristics** Over the Operating Range<sup>[9, 10]</sup>

Parameter	Parameter	Min	Max	Unit
<b>Clock</b>				
t <sub>TCYC</sub>	TCK Clock Cycle Time	50		ns
t <sub>TF</sub>	TCK Clock Frequency		20	MHz
t <sub>TH</sub>	TCK Clock HIGH Time	20		ns
t <sub>TL</sub>	TCK Clock LOW Time	20		ns
<b>Output Times</b>				
t <sub>TDOV</sub>	TCK Clock LOW to TDO Valid		10	ns
t <sub>TDOX</sub>	TCK Clock LOW to TDO Invalid	0		ns
<b>Set-up Times</b>				
t <sub>TMSS</sub>	TMS Setup to TCK Clock Rise	5		ns
t <sub>TDIS</sub>	TDI Setup to TCK Clock Rise	5		ns
t <sub>CS</sub>	Capture Setup to TCK Rise	5		ns
<b>Hold Times</b>				
t <sub>TMSH</sub>	TMS Hold after TCK Clock Rise	5		ns
t <sub>TDIH</sub>	TDI Hold after Clock Rise	5		ns
t <sub>CH</sub>	Capture Hold after Clock Rise	5		ns

**Notes**

9. t<sub>CS</sub> and t<sub>CH</sub> refer to the setup and hold time requirements of latching data from the boundary scan register.  
 10. Test conditions are specified using the load in TAP AC test conditions. t<sub>R</sub>/t<sub>F</sub> = 1 ns.

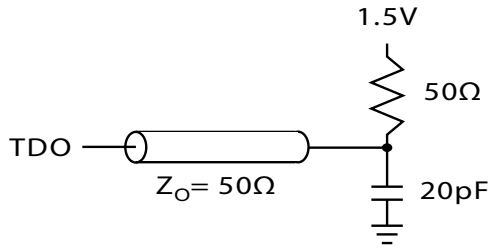
### 3.3V TAP AC Test Conditions

Input pulse levels .....  $V_{SS}$  to 3.3V  
 Input rise and fall times ..... 1 ns  
 Input timing reference levels ..... 1.5V  
 Output reference levels ..... 1.5V  
 Test load termination supply voltage ..... 1.5V

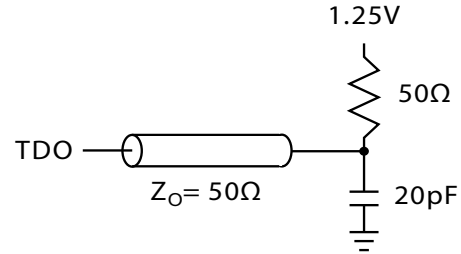
### 2.5V TAP AC Test Conditions

Input pulse levels .....  $V_{SS}$  to 2.5V  
 Input rise and fall time ..... 1 ns  
 Input timing reference levels ..... 1.25V  
 Output reference levels ..... 1.25V  
 Test load termination supply voltage ..... 1.25V

### 3.3V TAP AC Output Load Equivalent



### 2.5V TAP AC Output Load Equivalent



### TAP DC Electrical Characteristics And Operating Conditions

( $0^{\circ}\text{C} < T_A < +70^{\circ}\text{C}$ ;  $V_{DD} = 3.3\text{V} \pm 0.165\text{V}$  unless otherwise noted)<sup>[11]</sup>

Parameter	Description	Description	Conditions	Min	Max	Unit
V <sub>OH1</sub>	Output HIGH Voltage	I <sub>OH</sub> = -4.0 mA	V <sub>DDQ</sub> = 3.3V	2.4		V
		I <sub>OH</sub> = -1.0 mA	V <sub>DDQ</sub> = 2.5V	2.0		V
V <sub>OH2</sub>	Output HIGH Voltage	I <sub>OH</sub> = -100 μA	V <sub>DDQ</sub> = 3.3V	2.9		V
			V <sub>DDQ</sub> = 2.5V	2.1		V
V <sub>OL1</sub>	Output LOW Voltage	I <sub>OL</sub> = 8.0 mA	V <sub>DDQ</sub> = 3.3V		0.4	V
			V <sub>DDQ</sub> = 2.5V		0.4	V
V <sub>OL2</sub>	Output LOW Voltage	I <sub>OL</sub> = 100 μA	V <sub>DDQ</sub> = 3.3V		0.2	V
			V <sub>DDQ</sub> = 2.5V		0.2	V
V <sub>IH</sub>	Input HIGH Voltage		V <sub>DDQ</sub> = 3.3V	2.0	V <sub>DD</sub> + 0.3	V
			V <sub>DDQ</sub> = 2.5V	1.7	V <sub>DD</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage		V <sub>DDQ</sub> = 3.3V	-0.5	0.7	V
			V <sub>DDQ</sub> = 2.5V	-0.3	0.7	V
I <sub>X</sub>	Input Load Current	GND ≤ V <sub>IN</sub> ≤ V <sub>DDQ</sub>		-5	5	μA

### Identification Register Definitions

Instruction Field	CY7C1361C (256K x36)	CY7C1363C (512K x18)	Description
Revision Number (31:29)	000	000	Describes the version number.
Device Depth (28:24) <sup>[12]</sup>	01011	01011	Reserved for Internal Use
Device Width (23:18) 119-BGA	101001	101001	Defines memory type and architecture
Device Width (23:18) 165-FBGA	000001	000001	Defines memory type and architecture
Cypress Device ID (17:12)	100110	010110	Defines width and density
Cypress JEDEC ID Code (11:1)	00000110100	00000110100	Allows unique identification of SRAM vendor.
ID Register Presence Indicator (0)	1	1	Indicates the presence of an ID register.

**Notes**

- 11. All voltages referenced to V<sub>SS</sub> (GND).
- 12. Bit #24 is "1" in the Register Definitions for both 2.5V and 3.3V versions of this device.



### Scan Register Sizes

Register Name	Bit Size (x 36)	Bit Size (x 18)
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan Order (119-ball BGA package)	71	71
Boundary Scan Order (165-ball FBGA package)	71	71

### Identification Codes

Instruction	Code	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to High-Z state.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

119-Ball BGA Boundary Scan Order

CY7C1361C (256K x 36)					
Bit #	ball ID	Signal Name	Bit #	ball ID	Signal Name
1	K4	CLK	37	P4	A0
2	H4	GW	38	N4	A1
3	M4	BWE	39	R6	A
4	F4	OE	40	T5	A
5	B4	ADSC	41	T3	A
6	A4	ADSP	42	R2	A
7	G4	ADV	43	R3	MODE
8	C3	A	44	P2	DQP <sub>D</sub>
9	B3	A	45	P1	DQ <sub>D</sub>
10	D6	DQP <sub>B</sub>	46	L2	DQ <sub>D</sub>
11	H7	DQ <sub>B</sub>	47	K1	DQ <sub>D</sub>
12	G6	DQ <sub>B</sub>	48	N2	DQ <sub>D</sub>
13	E6	DQ <sub>B</sub>	49	N1	DQ <sub>D</sub>
14	D7	DQ <sub>B</sub>	50	M2	DQ <sub>D</sub>
15	E7	DQ <sub>B</sub>	51	L1	DQ <sub>D</sub>
16	F6	DQ <sub>B</sub>	52	K2	DQ <sub>D</sub>
17	G7	DQ <sub>B</sub>	53	Internal	Internal
18	H6	DQ <sub>B</sub>	54	H1	DQ <sub>C</sub>
19	T7	ZZ	55	G2	DQ <sub>C</sub>
20	K7	DQ <sub>A</sub>	56	E2	DQ <sub>C</sub>
21	L6	DQ <sub>A</sub>	57	D1	DQ <sub>C</sub>
22	N6	DQ <sub>A</sub>	58	H2	DQ <sub>C</sub>
23	P7	DQ <sub>A</sub>	59	G1	DQ <sub>C</sub>
24	N7	DQ <sub>A</sub>	60	F2	DQ <sub>C</sub>
25	M6	DQ <sub>A</sub>	61	E1	DQ <sub>C</sub>
26	L7	DQ <sub>A</sub>	62	D2	DQP <sub>C</sub>
27	K6	DQ <sub>A</sub>	63	C2	A
28	P6	DQP <sub>A</sub>	64	A2	A
29	T4	A	65	E4	CE <sub>1</sub>
30	A3	A	66	B2	CE <sub>2</sub>
31	C5	A	67	L3	BWD
32	B5	A	68	G3	BW <sub>C</sub>
33	A5	A	69	G5	BW <sub>B</sub>
34	C6	A	70	L5	BW <sub>A</sub>
35	A6	A	71	Internal	Internal
36	B6	A			

CY7C1363C (512K x 18)					
Bit #	ball ID	Signal Name	Bit #	ball ID	Signal Name
1	K4	CLK	37	P4	A0
2	H4	GW	38	N4	A1
3	M4	BWE	39	R6	A
4	F4	OE	40	T5	A
5	B4	ADSC	41	T3	A
6	A4	ADSP	42	R2	A
7	G4	ADV	43	R3	MODE
8	C3	A	44	Internal	Internal
9	B3	A	45	Internal	Internal
10	T2	A	46	Internal	Internal
11	Internal	Internal	47	Internal	Internal
12	Internal	Internal	48	P2	DQP <sub>B</sub>
13	Internal	Internal	49	N1	DQ <sub>B</sub>
14	D6	DQP <sub>A</sub>	50	M2	DQ <sub>B</sub>
15	E7	DQ <sub>A</sub>	51	L1	DQ <sub>B</sub>
16	F6	DQ <sub>A</sub>	52	K2	DQ <sub>B</sub>
17	G7	DQ <sub>A</sub>	53	Internal	Internal
18	H6	DQ <sub>A</sub>	54	H1	DQ <sub>B</sub>
19	T7	ZZ	55	G2	DQ <sub>B</sub>
20	K7	DQ <sub>A</sub>	56	E2	DQ <sub>B</sub>
21	L6	DQ <sub>A</sub>	57	D1	DQ <sub>B</sub>
22	N6	DQ <sub>A</sub>	58	Internal	Internal
23	P7	DQ <sub>A</sub>	59	Internal	Internal
24	Internal	Internal	60	Internal	Internal
25	Internal	Internal	61	Internal	Internal
26	Internal	Internal	62	Internal	Internal
27	Internal	Internal	63	C2	A
28	Internal	Internal	64	A2	A
29	T6	A	65	E4	CE <sub>1</sub>
30	A3	A	66	B2	CE <sub>2</sub>
31	C5	A	67	Internal	Internal
32	B5	A	68	Internal	Internal
33	A5	A	69	G3	BW <sub>B</sub>
34	C6	A	70	L5	BW <sub>A</sub>
35	A6	A	71	Internal	Internal
36	B6	A			

165-Ball FBGA Boundary Scan Order

CY7C1361C (256K x 36)					
Bit #	ball ID	Signal Name	Bit #	ball ID	Signal Name
1	B6	CLK	37	R6	A0
2	B7	$\overline{GW}$	38	P6	A1
3	A7	$\overline{BWE}$	39	R4	A
4	B8	$\overline{OE}$	40	P4	A
5	A8	$\overline{ADSC}$	41	R3	A
6	B9	$\overline{ADSP}$	42	P3	A
7	A9	$\overline{ADV}$	43	R1	MODE
8	B10	A	44	N1	DQP <sub>D</sub>
9	A10	A	45	L2	DQ <sub>D</sub>
10	C11	DQP <sub>B</sub>	46	K2	DQ <sub>D</sub>
11	E10	DQ <sub>B</sub>	47	J2	DQ <sub>D</sub>
12	F10	DQ <sub>B</sub>	48	M2	DQ <sub>D</sub>
13	G10	DQ <sub>B</sub>	49	M1	DQ <sub>D</sub>
14	D10	DQ <sub>B</sub>	50	L1	DQ <sub>D</sub>
15	D11	DQ <sub>B</sub>	51	K1	DQ <sub>D</sub>
16	E11	DQ <sub>B</sub>	52	J1	DQ <sub>D</sub>
17	F11	DQ <sub>B</sub>	53	Internal	Internal
18	G11	DQ <sub>B</sub>	54	G2	DQ <sub>C</sub>
19	H11	ZZ	55	F2	DQ <sub>C</sub>
20	J10	DQ <sub>A</sub>	56	E2	DQ <sub>C</sub>
21	K10	DQ <sub>A</sub>	57	D2	DQ <sub>C</sub>
22	L10	DQ <sub>A</sub>	58	G1	DQ <sub>C</sub>
23	M10	DQ <sub>A</sub>	59	F1	DQ <sub>C</sub>
24	J11	DQ <sub>A</sub>	60	E1	DQ <sub>C</sub>
25	K11	DQ <sub>A</sub>	61	D1	DQ <sub>C</sub>
26	L11	DQ <sub>A</sub>	62	C1	DQP <sub>C</sub>
27	M11	DQ <sub>A</sub>	63	B2	A
28	N11	DQP <sub>A</sub>	64	A2	A
29	R11	A	65	A3	CE <sub>1</sub>
30	R10	A	66	B3	CE <sub>2</sub>
31	P10	A	67	B4	$\overline{BW}_D$
32	R9	A	68	A4	$\overline{BW}_C$
33	P9	A	69	A5	$\overline{BW}_B$
34	R8	A	70	B5	$\overline{BW}_A$
35	P8	A	71	A6	CE <sub>3</sub>
36	P11	A			

CY7C1363C (512K x 18)					
Bit #	ball ID	Signal Name	Bit #	ball ID	Signal Name
1	B6	CLK	37	R6	A0
2	B7	$\overline{GW}$	38	P6	A1
3	A7	$\overline{BWE}$	39	R4	A
4	B8	$\overline{OE}$	40	P4	A
5	A8	$\overline{ADSC}$	41	R3	A
6	B9	$\overline{ADSP}$	42	P3	A
7	A9	$\overline{ADV}$	43	R1	MODE
8	B10	A	44	Internal	Internal
9	A10	A	45	Internal	Internal
10	A11	A	46	Internal	Internal
11	Internal	Internal	47	Internal	Internal
12	Internal	Internal	48	N1	DQP <sub>B</sub>
13	Internal	Internal	49	M1	DQ <sub>B</sub>
14	C11	DQP <sub>A</sub>	50	L1	DQ <sub>B</sub>
15	D11	DQ <sub>A</sub>	51	K1	DQ <sub>B</sub>
16	E11	DQ <sub>A</sub>	52	J1	DQ <sub>B</sub>
17	F11	DQ <sub>A</sub>	53	Internal	Internal
18	G11	DQ <sub>A</sub>	54	G2	DQ <sub>B</sub>
19	H11	ZZ	55	F2	DQ <sub>B</sub>
20	J10	DQ <sub>A</sub>	56	E2	DQ <sub>B</sub>
21	K10	DQ <sub>A</sub>	57	D2	DQ <sub>B</sub>
22	L10	DQ <sub>A</sub>	58	Internal	Internal
23	M10	DQ <sub>A</sub>	59	Internal	Internal
24	Internal	Internal	60	Internal	Internal
25	Internal	Internal	61	Internal	Internal
26	Internal	Internal	62	Internal	Internal
27	Internal	Internal	63	B2	A
28	Internal	Internal	64	A2	A
29	R11	A	65	A3	$\overline{CE}_1$
30	R10	A	66	B3	CE <sub>2</sub>
31	P10	A	67	Internal	Internal
32	R9	A	68	Internal	Internal
33	P9	A	69	A4	$\overline{BW}_B$
34	R8	A	70	B5	$\overline{BW}_A$
35	P8	A	71	A6	CE <sub>3</sub>
36	P11	A			

### Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

- Storage Temperature ..... -65°C to + 150°C
- Ambient Temperature with Power Applied ..... -55°C to + 125°C
- Supply Voltage on V<sub>DD</sub> Relative to GND ..... -0.5V to + 4.6V
- Supply Voltage on V<sub>DDQ</sub> Relative to GND ..... -0.5V to + V<sub>DD</sub>
- DC Voltage Applied to Outputs in tri-state ..... -0.5V to V<sub>DDQ</sub> + 0.5V
- DC Input Voltage ..... -0.5V to V<sub>DD</sub> + 0.5V
- Current into Outputs (LOW) ..... 20 mA
- Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)
- Latch up Current ..... >200 mA

### Operating Range

Range	Ambient Temperature	V <sub>DD</sub>	V <sub>DDQ</sub>
Commercial	0°C to +70°C	3.3V – 5%/+10%	2.5V – 5% to V <sub>DD</sub>
Industrial	-40°C to +85°C		
Automotive	-40°C to +125°C		

### Neutron Soft Error Immunity

Parameter	Description	Test Conditions	Typ	Max*	Unit
LSBU	Logical Single-Bit Upsets	25°C	361	394	FIT/Mb
LMBU	Logical Multi-Bit Upsets	25°C	0	0.01	FIT/Mb
SEL	Single Event Latch up	85°C	0	0.1	FIT/Dev

\* No LMBU, or SEL events occurred during testing; this column represents a statistical  $\chi^2$ , 95% confidence limit calculation. For more details refer to Application Note AN 54908 "Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates"

### Electrical Characteristics Over the Operating Range [13, 14]

Parameter	Description	Test Conditions	Min	Max	Unit
V <sub>DD</sub>	Power Supply Voltage		3.135	3.6	V
V <sub>DDQ</sub>	I/O Supply Voltage	for 3.3V I/O	3.135	V <sub>DD</sub>	V
		for 2.5V I/O	2.375	2.625	V
V <sub>OH</sub>	Output HIGH Voltage	for 3.3V I/O, I <sub>OH</sub> = -4.0 mA	2.4		V
		for 2.5V I/O, I <sub>OH</sub> = -1.0 mA	2.0		V
V <sub>OL</sub>	Output LOW Voltage	for 3.3V I/O, I <sub>OL</sub> = 8.0 mA		0.4	V
		for 2.5V I/O, I <sub>OL</sub> = 1.0 mA		0.4	V
V <sub>IH</sub>	Input HIGH Voltage <sup>[13]</sup>	for 3.3V I/O	2.0	V <sub>DD</sub> + 0.3V	V
		for 2.5V I/O	1.7	V <sub>DD</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW Voltage <sup>[13]</sup>	for 3.3V I/O	-0.3	0.8	V
		for 2.5V I/O	-0.3	0.7	V
I <sub>X</sub>	Input Leakage Current except ZZ and MODE	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub>	-5	5	μA
	Input Current of MODE	Input = V <sub>SS</sub>	-30		μA
		Input = V <sub>DD</sub>		5	μA
	Input Current of ZZ	Input = V <sub>SS</sub>	-5		μA
Input = V <sub>DD</sub>			30	μA	
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub> , Output Disabled	-5	5	μA

**Notes**

- 13. Overshoot: V<sub>IH</sub>(AC) < V<sub>DD</sub> + 1.5V (Pulse width less than t<sub>CYC/2</sub>), undershoot: V<sub>IL</sub>(AC) > -2V (Pulse width less than t<sub>CYC/2</sub>).
- 14. T<sub>Power-up</sub>: Assumes a linear ramp from 0V to V<sub>DD</sub>(min.) within 200ms. During this time V<sub>IH</sub> < V<sub>DD</sub> and V<sub>DDQ</sub> ≤ V<sub>DD</sub>.

**Electrical Characteristics** Over the Operating Range (continued)<sup>[13, 14]</sup>

Parameter	Description	Test Conditions	Min	Max	Unit
I <sub>DD</sub>	V <sub>DD</sub> Operating Supply Current	V <sub>DD</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>CYC</sub>	7.5 ns cycle, 133 MHz	250	mA
			10 ns cycle, 100 MHz	180	
I <sub>SB1</sub>	Automatic CE Power-down Current—TTL Inputs	Max. V <sub>DD</sub> , Device Deselected, V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub> , inputs switching	All speeds (Comm/Ind'l)	110	mA
			10 ns cycle, 100 MHz (Automotive)	150	
I <sub>SB2</sub>	Automatic CE Power-down Current—CMOS Inputs	Max. V <sub>DD</sub> , Device Deselected, V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0, inputs static	All speeds	40	mA
I <sub>SB3</sub>	Automatic CE Power-down Current—CMOS Inputs	Max. V <sub>DD</sub> , Device Deselected, V <sub>IN</sub> ≥ V <sub>DDQ</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = f <sub>MAX</sub> , inputs switching	All speeds (Comm/Ind'l)	100	mA
			10 ns cycle, 100 MHz (Automotive)	120	
I <sub>SB4</sub>	Automatic CE Power-down Current—TTL Inputs	Max. V <sub>DD</sub> , Device Deselected, V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = 0, inputs static	All speeds (Comm/Ind'l)	40	mA
			10 ns cycle, 100 MHz (Automotive)	60	

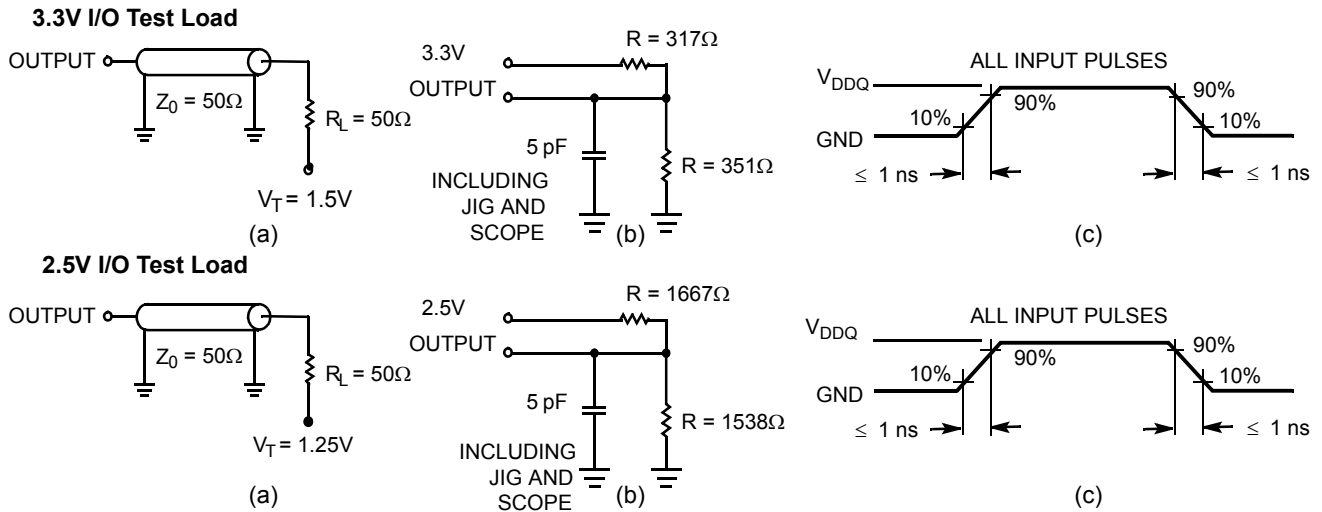
**Capacitance**<sup>[15]</sup>

Parameter	Description	Test Conditions	100 TQFP Max.	119 BGA Max.	165 FBGA Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>DD</sub> = 3.3V, V <sub>DDQ</sub> = 2.5V	5	5	5	pF
C <sub>CLK</sub>	Clock Input Capacitance		5	5	5	pF
C <sub>I/O</sub>	Input/Output Capacitance		5	7	7	pF

**Thermal Resistance**<sup>[15]</sup>

Parameter	Description	Test Conditions	100 TQFP Package	119 BGA Package	165 FBGA Package	Unit
Θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, according to EIA/JESD51	29.41	34.1	16.8	°C/W
Θ <sub>JC</sub>	Thermal Resistance (Junction to Case)		6.31	14.0	3.0	°C/W

**Figure 5. AC Test Loads and Waveforms**



**Note**  
15. Tested initially and after any design or process change that may affect these parameters.

**Switching Characteristics** Over the Operating Range<sup>[20, 21]</sup>

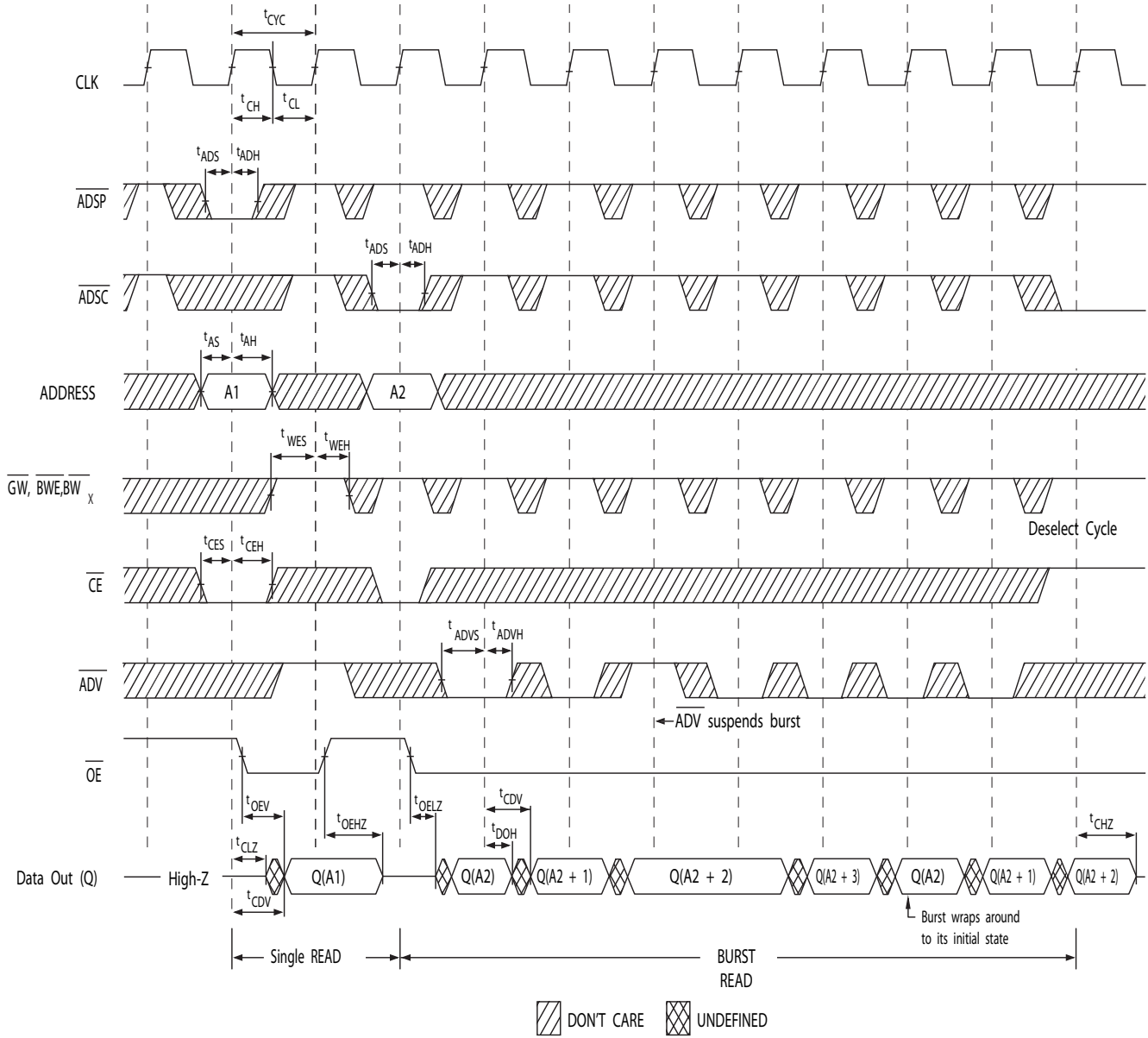
Parameter	Description	-133		-100		Unit
		Min	Max	Min	Max	
t <sub>POWER</sub>	V <sub>DD</sub> (Typical) to the first Access <sup>[16]</sup>	1		1		ms
<b>Clock</b>						
t <sub>CYC</sub>	Clock Cycle Time	7.5		10		ns
t <sub>CH</sub>	Clock HIGH	3.0		4.0		ns
t <sub>CL</sub>	Clock LOW	3.0		4.0		ns
<b>Output Times</b>						
t <sub>CDV</sub>	Data Output Valid After CLK Rise		6.5		8.5	ns
t <sub>DOH</sub>	Data Output Hold After CLK Rise	2.0		2.0		ns
t <sub>CLZ</sub>	Clock to Low-Z <sup>[17, 18, 19]</sup>	0		0		ns
t <sub>CHZ</sub>	Clock to High-Z <sup>[17, 18, 19]</sup>		3.5		3.5	ns
t <sub>OEV</sub>	OE LOW to Output Valid		3.5		3.5	ns
t <sub>OELZ</sub>	OE LOW to Output Low-Z <sup>[17, 18, 19]</sup>	0		0		ns
t <sub>OEHZ</sub>	OE HIGH to Output High-Z <sup>[17, 18, 19]</sup>		3.5		3.5	ns
<b>Set-up Times</b>						
t <sub>AS</sub>	Address Setup Before CLK Rise	1.5		1.5		ns
t <sub>ADS</sub>	ADSP, ADSC Setup Before CLK Rise	1.5		1.5		ns
t <sub>ADVS</sub>	ADV Setup Before CLK Rise	1.5		1.5		ns
t <sub>WES</sub>	GW, BWE, BW <sub>[A:D]</sub> Setup Before CLK Rise	1.5		1.5		ns
t <sub>DS</sub>	Data Input Setup Before CLK Rise	1.5		1.5		ns
t <sub>CES</sub>	Chip Enable Setup	1.5		1.5		ns
<b>Hold Times</b>						
t <sub>AH</sub>	Address Hold After CLK Rise	0.5		0.5		ns
t <sub>ADH</sub>	ADSP, ADSC Hold After CLK Rise	0.5		0.5		ns
t <sub>WEH</sub>	GW, BWE, BW <sub>[A:D]</sub> Hold After CLK Rise	0.5		0.5		ns
t <sub>ADVH</sub>	ADV Hold After CLK Rise	0.5		0.5		ns
t <sub>DH</sub>	Data Input Hold After CLK Rise	0.5		0.5		ns
t <sub>CEH</sub>	Chip Enable Hold After CLK Rise	0.5		0.5		ns

**Notes**

16. This part has a voltage regulator internally; t<sub>POWER</sub> is the time that the power needs to be supplied above V<sub>DD</sub>(minimum) initially, before a read or write operation can be initiated.
17. t<sub>CHZ</sub>, t<sub>CLZ</sub>, t<sub>OELZ</sub>, and t<sub>OEHZ</sub> are specified with AC test conditions shown in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
18. At any given voltage and temperature, t<sub>OEHZ</sub> is less than t<sub>OELZ</sub> and t<sub>CHZ</sub> is less than t<sub>CLZ</sub> to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
19. This parameter is sampled and not 100% tested.
20. Timing reference level is 1.5V when V<sub>DDQ</sub> = 3.3V and is 1.25V when V<sub>DDQ</sub> = 2.5V.
21. Test conditions shown in (a) of AC Test Loads unless otherwise noted.

Timing Diagrams

Figure 6. Read Cycle Timing<sup>[22]</sup>

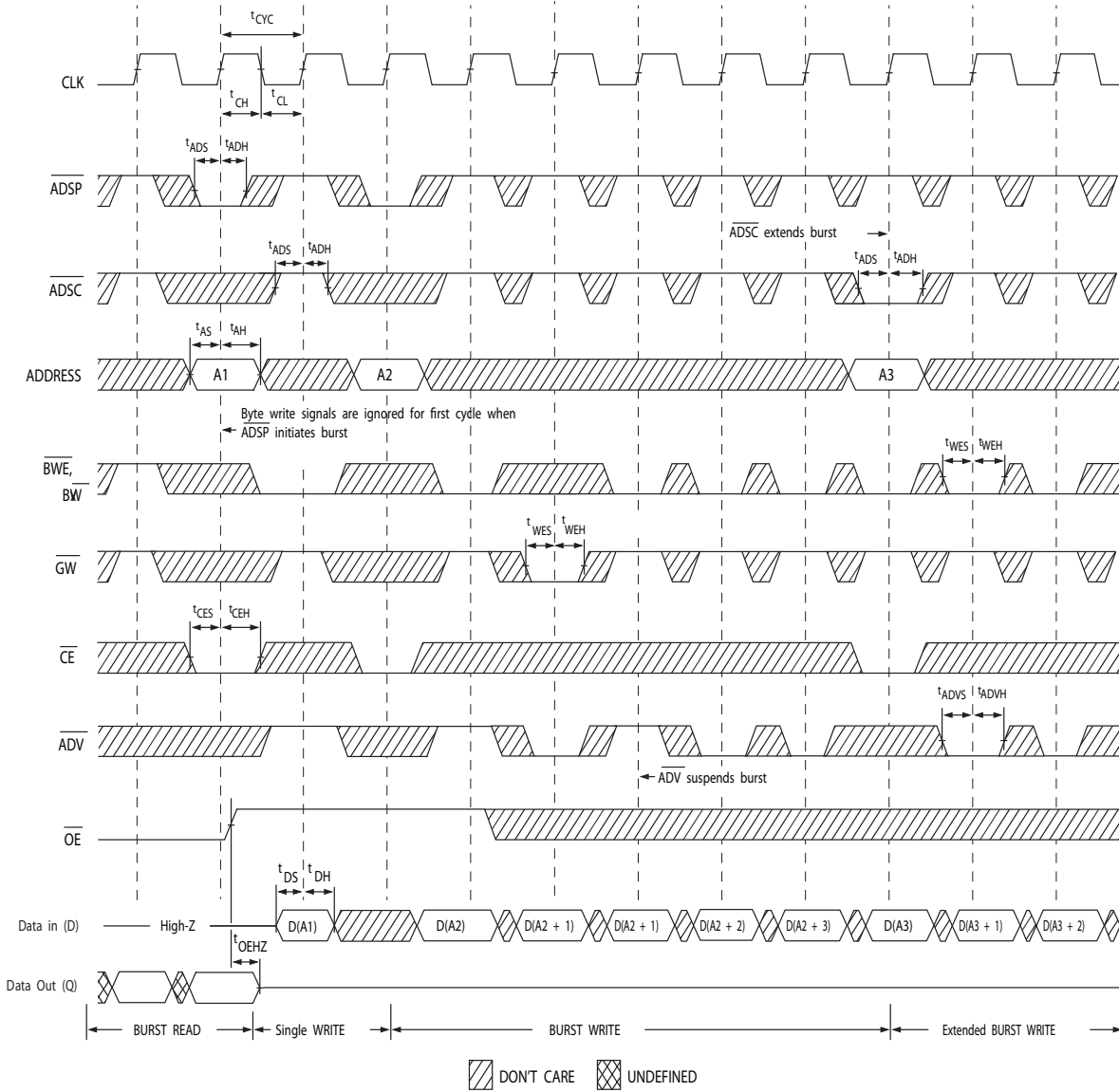


Note

22. On this diagram, when  $\overline{CE}$  is LOW:  $\overline{CE}_1$  is LOW,  $CE_2$  is HIGH and  $\overline{CE}_3$  is LOW. When  $\overline{CE}$  is HIGH:  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW or  $\overline{CE}_3$  is HIGH.

Timing Diagrams (continued)

Figure 7. Write Cycle Timing<sup>[22, 23]</sup>

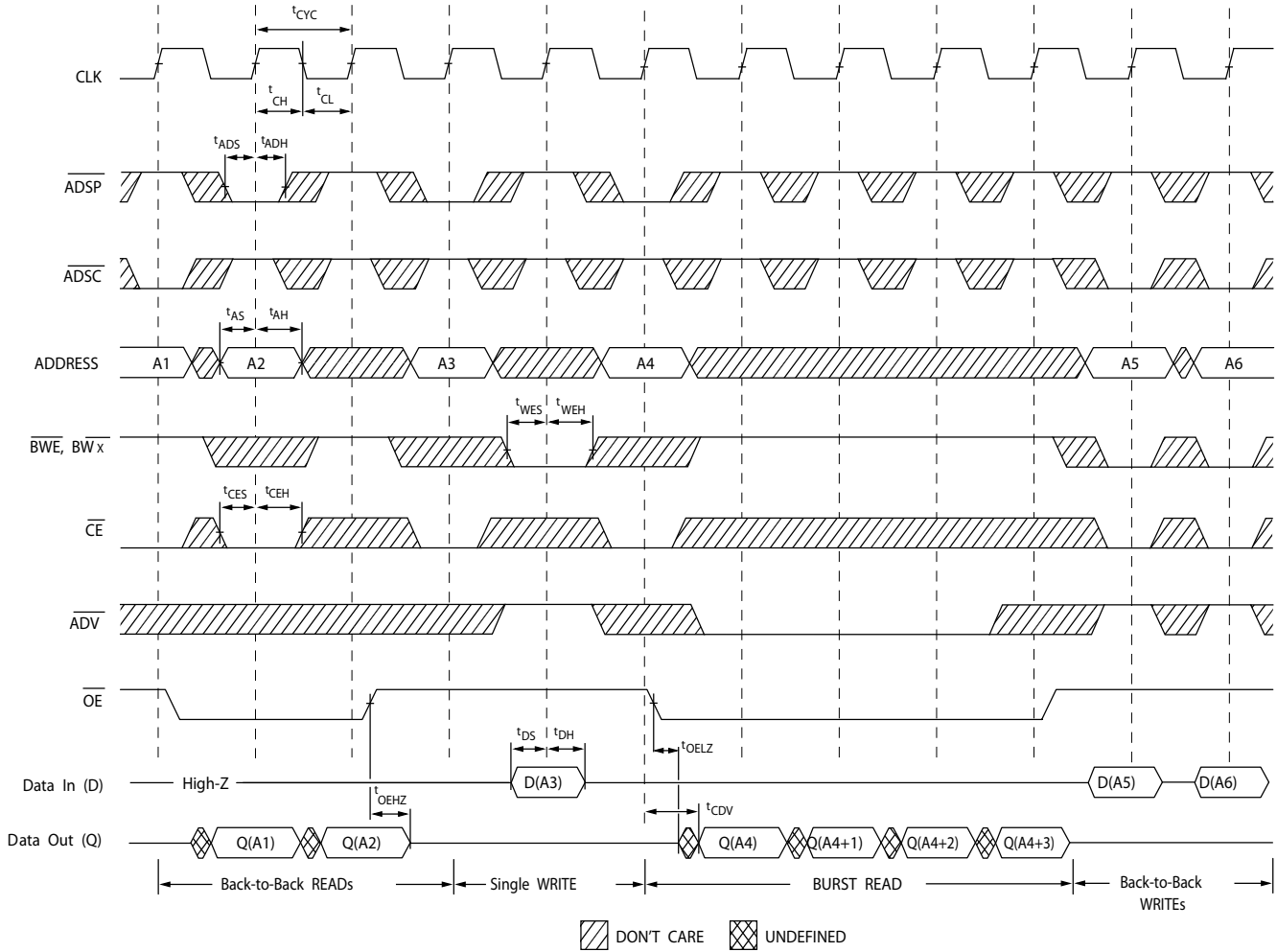


**Note**  
 23. Full width write can be initiated by either  $\overline{GW}$  LOW; or by  $\overline{GW}$  HIGH,  $\overline{BWE}$  LOW and  $\overline{BW}_X$  LOW.



Timing Diagrams (continued)

Figure 8. Read/Write Cycle Timing<sup>[22, 24, 25]</sup>

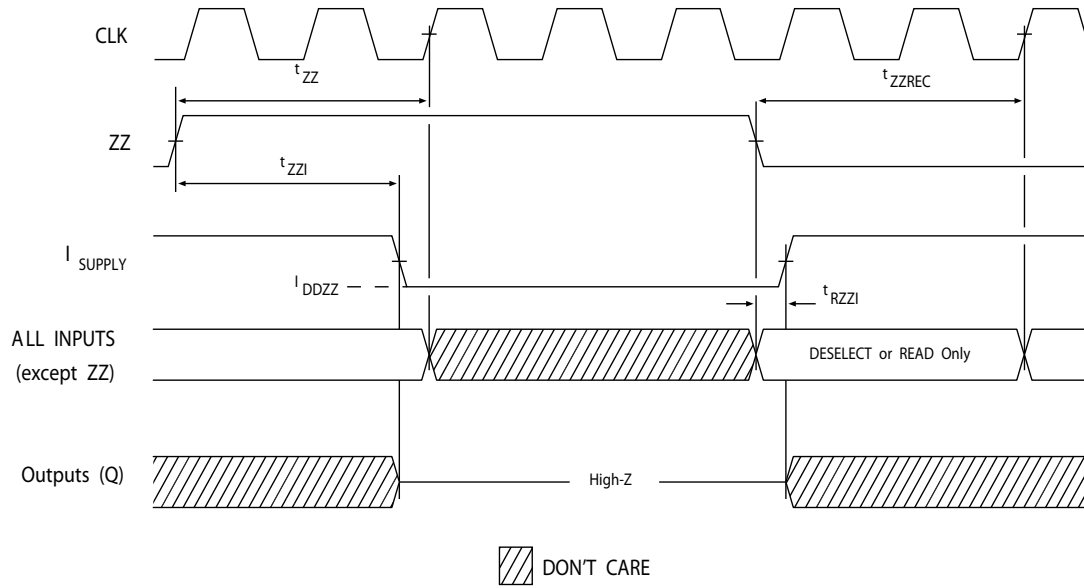


Notes

- 24. The data bus (Q) remains in high-Z following a WRITE cycle, unless a new read access is initiated by  $\overline{ADSP}$  or  $\overline{ADSC}$ .
- 25.  $\overline{GW}$  is HIGH.

**Timing Diagrams** (continued)

**Figure 9. ZZ Mode Timing**<sup>[26, 27]</sup>



**Notes**

- 26. Device must be deselected when entering ZZ mode. See Cycle Descriptions table for all possible signal conditions to deselect the device.
- 27. DQs are in high-Z when exiting ZZ sleep mode.

## Ordering Information

The table below contains only the parts that are currently available. If you don't see what you are looking for, please contact your local sales representative. For more information, visit the Cypress website at [www.cypress.com](http://www.cypress.com) and refer to the product summary page at <http://www.cypress.com/products>

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**Table 3. Ordering Information**

Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
133	CY7C1361C-133AXC	51-85050	100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free (3 Chip Enable)	Commercial
	CY7C1363C-133AXC			
	CY7C1361C-133AJXC	51-85050	100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free (2 Chip Enable)	
	CY7C1363C-133AJXC			
	CY7C1361C-133AXI	51-85050	100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free (3 Chip Enable)	Industrial
	CY7C1363C-133AJXI	51-85050	100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free (2 Chip Enable)	
100	CY7C1361C-100AXC	51-85050	100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free (3 Chip Enable)	Commercial
	CY7C1361C-100BGC	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm)	
100	CY7C1361C-100AXE	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free	Automotive

Package Diagrams (continued)

Figure 10. 100-Pin TQFP (14X20X1.4 mm)

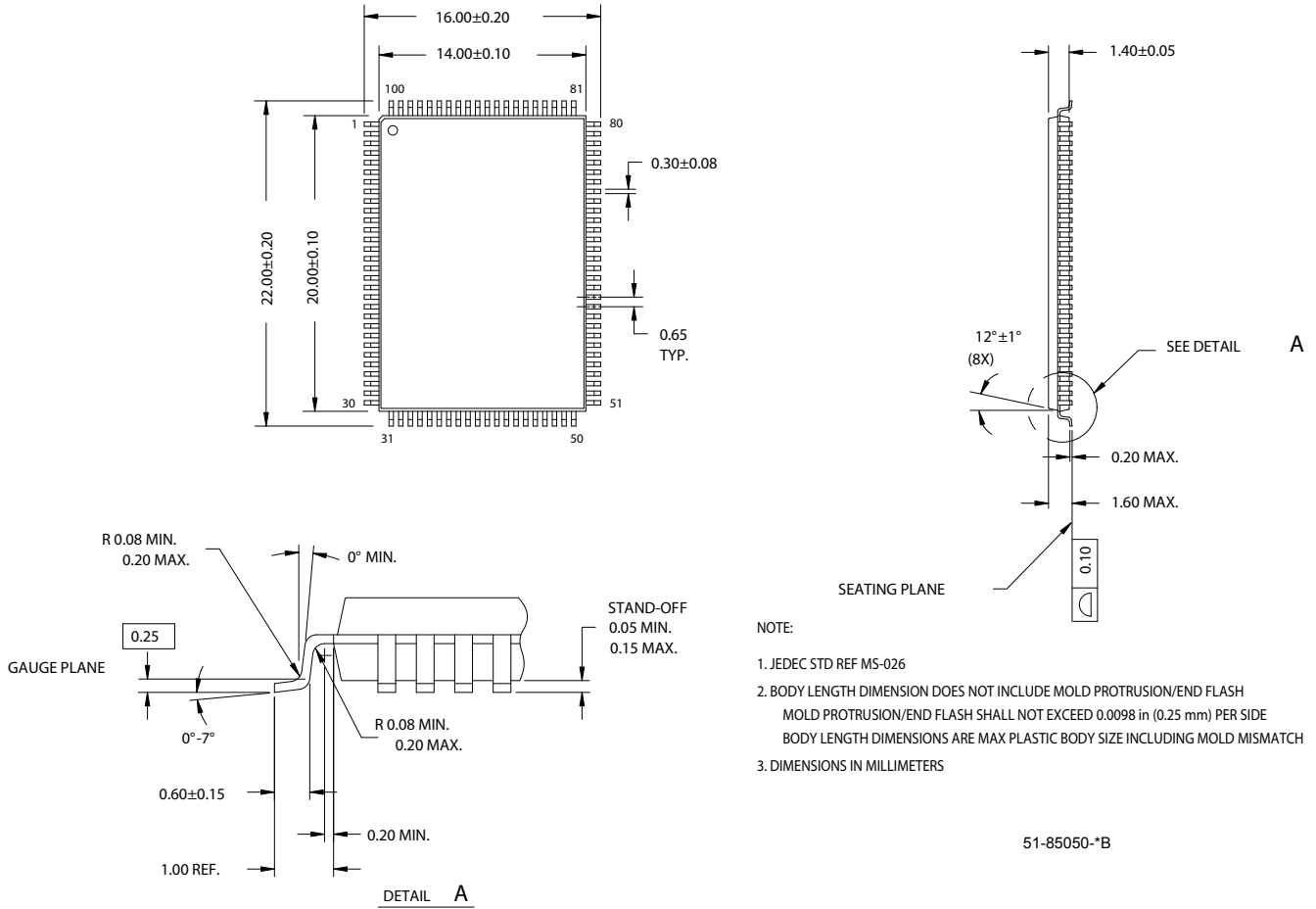


Figure 11. 119-Ball BGA (14X22X2.4 mm)

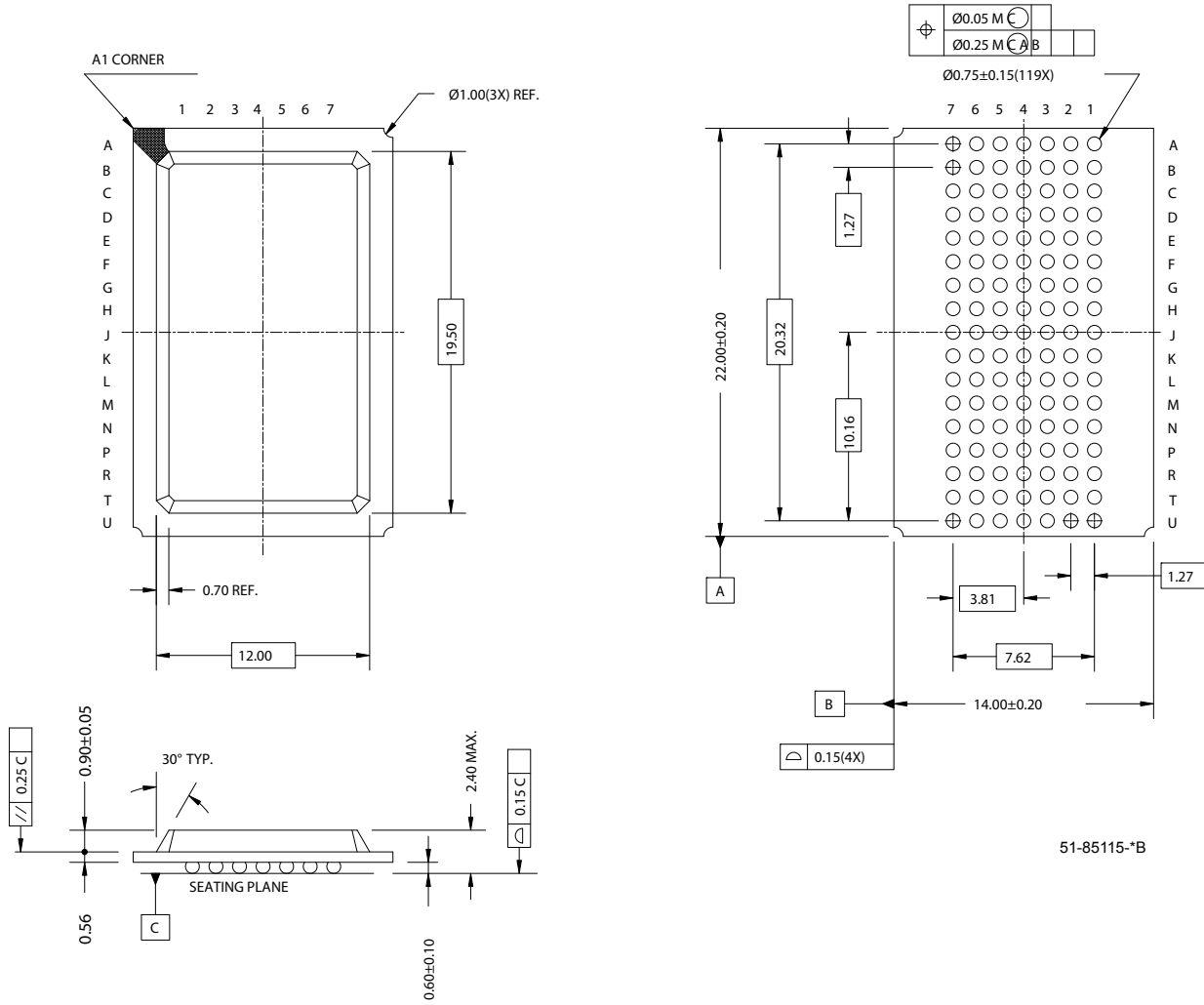
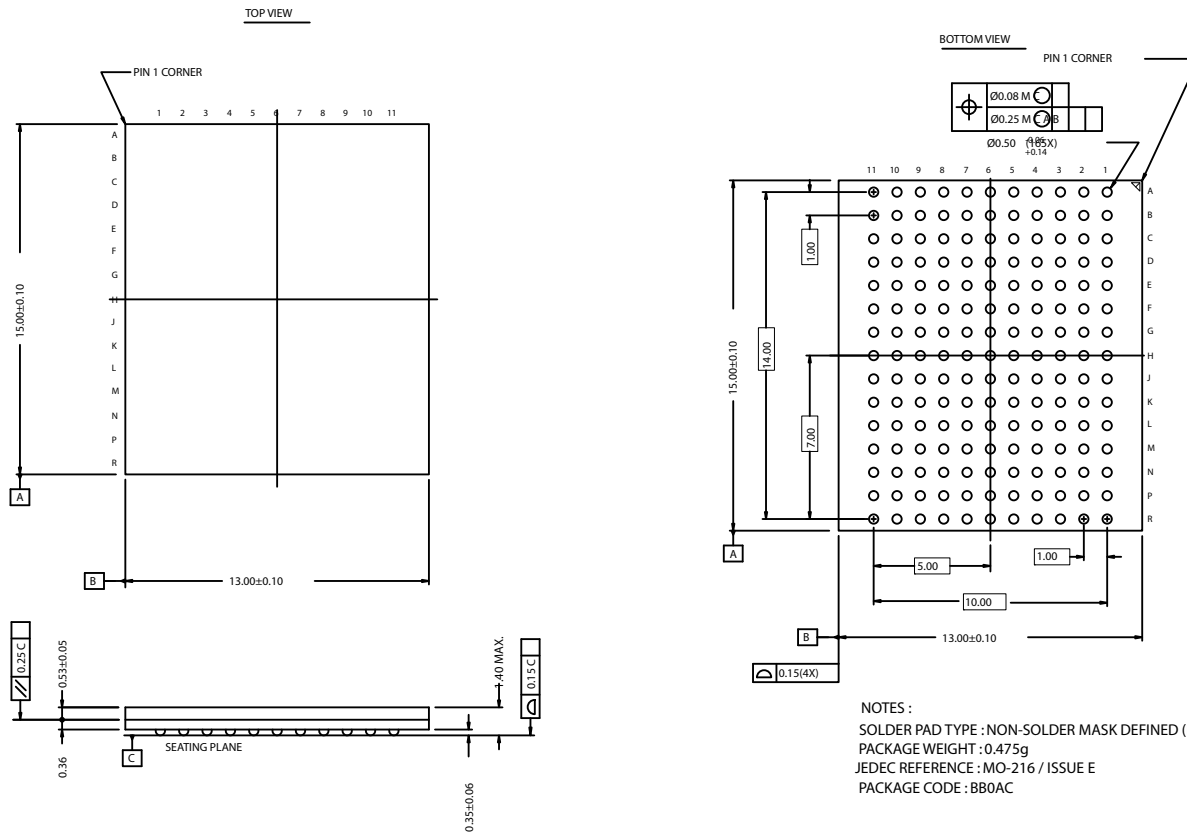


Figure 12. 165-Ball FBGA (13X15X1.4 mm)



51-85180-B

Document History Page

Document Title: CY7C1361C/CY7C1363C 9-Mbit (256K x 36/512K x 18) Flow-Through SRAM Document Number: 38-05541				
REV.	ECN NO.	Submission Date	Orig. of Change	Description of Change
**	241690	See ECN	RKF	New data sheet
*A	278969	See ECN	RKF	Changed Boundary Scan order to match the B rev of these devices.
*B	332059	See ECN	PCI	Removed 117-MHz Speed Bin Address expansion pins/balls in the pinouts for all packages are modified as per JEDEC standard Added Address Expansion pins in the Pin Definitions Table Changed Device Width (23:18) for 119-BGA from 000001 to 101001 Added separate row for 165 -FBGA Device Width (23:18) Changed I <sub>DDZZ</sub> from 35 mA to 50 mA Changed I <sub>SB1</sub> and I <sub>SB3</sub> from 40 mA to 110 and 100 mA, respectively Modified V <sub>OL</sub> , V <sub>OH</sub> test conditions Corrected I <sub>SB4</sub> Test Condition from (V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V) to (V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> ) in the Electrical Characteristics table Changed $\theta_{JA}$ and $\theta_{JC}$ for TQFP Package from 25 and 9 °C/W to 29.41 and 6.13 °C/W respectively Changed $\theta_{JA}$ and $\theta_{JC}$ for BGA Package from 25 and 6 °C/W to 34.1 and 14.0 °C/W respectively Changed $\theta_{JA}$ and $\theta_{JC}$ for FBGA Package from 27 and 6 °C/W to 16.8 and 3.0 °C/W respectively Added lead-free information for 100-pin TQFP, 119 BGA and 165 FBGA packages Updated Ordering Information Table
*C	377095	See ECN	PCI	Changed I <sub>SB2</sub> from 30 to 40 mA Modified test condition in note# 14 from V <sub>IH</sub> ≤ V <sub>DD</sub> to V <sub>IH</sub> < V <sub>DD</sub>
*D	408298	See ECN	RXU	Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Changed tri state to tri-state. Modified "Input Load" to "Input Leakage Current except ZZ and MODE" in the Electrical Characteristics Table. Replaced Package Name column with Package Diagram in the Ordering Information table. Updated the ordering information.
*E	433033	See ECN	NXR	Included Automotive range.
*F	501793	See ECN	VKN	Added the Maximum Rating for Supply Voltage on V <sub>DDQ</sub> Relative to GND Changed t <sub>TH</sub> , t <sub>TL</sub> from 25 ns to 20 ns and t <sub>TDOV</sub> from 5 ns to 10 ns in TAP AC Switching Characteristics table. Updated the Ordering Information table.
*G	2756340	08/26/2009	VKN/AESA	Updated template Included Soft Error Immunity Data Modified Ordering Information table by including parts that are available and modified the disclaimer for the Ordering information.

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