

# 4-Mbit (128 K × 36) Pipelined Sync SRAM

## Features

- Fully registered inputs and outputs for pipelined operation
- 128 K × 36 common I/O architecture
- 3.3 V core power supply ( $V_{DD}$ )
- 2.5- / 3.3-V I/O power supply ( $V_{DDQ}$ )
- Fast clock to output times: 2.6 ns (for 250 MHz device)
- User selectable burst counter supporting Intel Pentium interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self timed writes
- Asynchronous output enable
- Offered in Pb-free 100-Pin TQFP, Pb-free and non Pb-free 119-Ball BGA package, and 165-Ball FBGA package
- “ZZ” sleep mode option and stop clock option
- Available in Industrial and commercial temperature ranges

## Functional Description

The CY7C1347G<sup>[1]</sup> is a 3.3 V, 128 K × 36 synchronous pipelined SRAM designed to support zero-wait-state secondary cache with minimal glue logic. CY7C1347G I/O pins can operate at either the 2.5 V or the 3.3 V level. The I/O pins are 3.3 V tolerant when  $V_{DDQ} = 2.5$  V. All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise is 2.6 ns (250 MHz device). CY7C1347G supports either the interleaved burst sequence used by the Intel Pentium processor or a linear burst sequence used by processors such as the PowerPC. The burst sequence is selected through the MODE pin. Accesses can be initiated by asserting either the address strobe from processor (ADSP) or the address strobe from controller (ADSC) at clock rise. Address advancement through the burst sequence is controlled by the ADV input. A 2-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the four Byte Write Select ( $BW_{[A:D]}$ ) inputs. A global write enable ( $\overline{GW}$ ) overrides all byte write inputs and writes data to all four bytes. All writes are conducted with on-chip synchronous self timed write circuitry.

Three synchronous chip Selects ( $\overline{CE}_1, \overline{CE}_2, \overline{CE}_3$ ) and an asynchronous output enable ( $\overline{OE}$ ) provide for easy bank selection and output tristate control. To provide proper data during depth expansion,  $\overline{OE}$  is masked during the first clock of a read cycle when emerging from a deselected state.

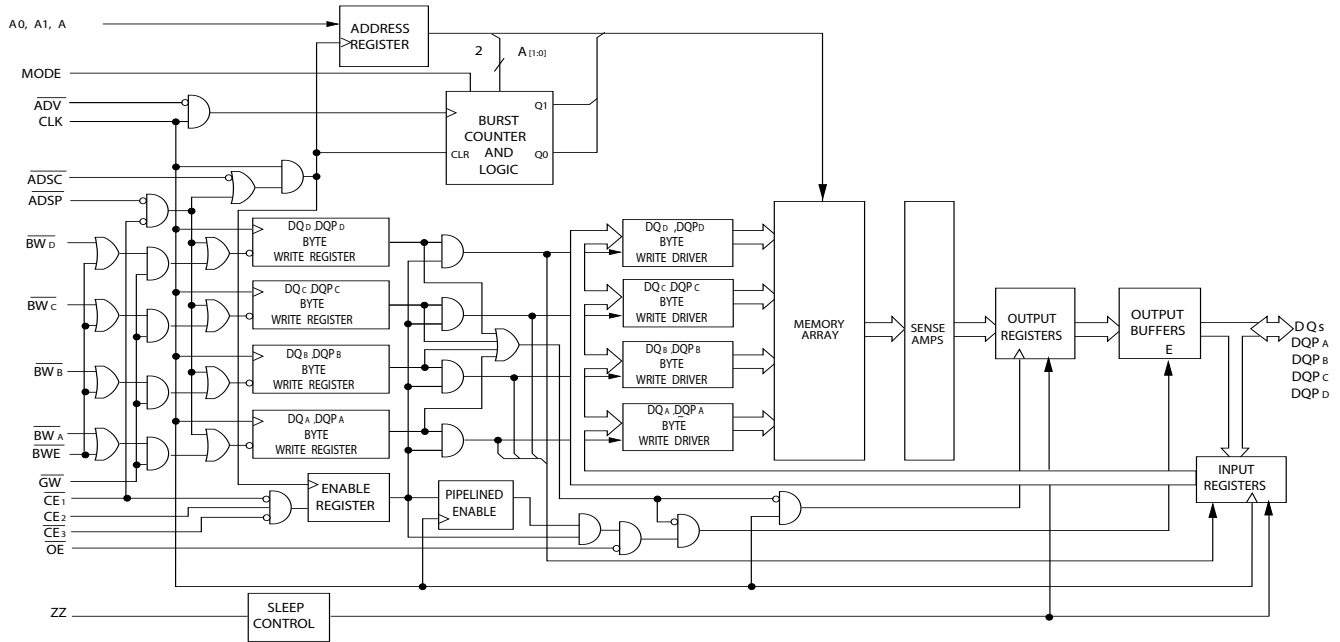
## Selection Guide

Description	250 MHz	200 MHz	166 MHz	133 MHz	Unit
Maximum access time	2.6	2.8	3.5	4.0	ns
Maximum operating current	325	265	240	225	mA
Maximum CMOS standby current	40	40	40	40	mA

### Note

1. For best practice recommendations, refer to the Cypress application note, [SRAM System Guidelines – AN1064](#).

### Logic Block Diagram

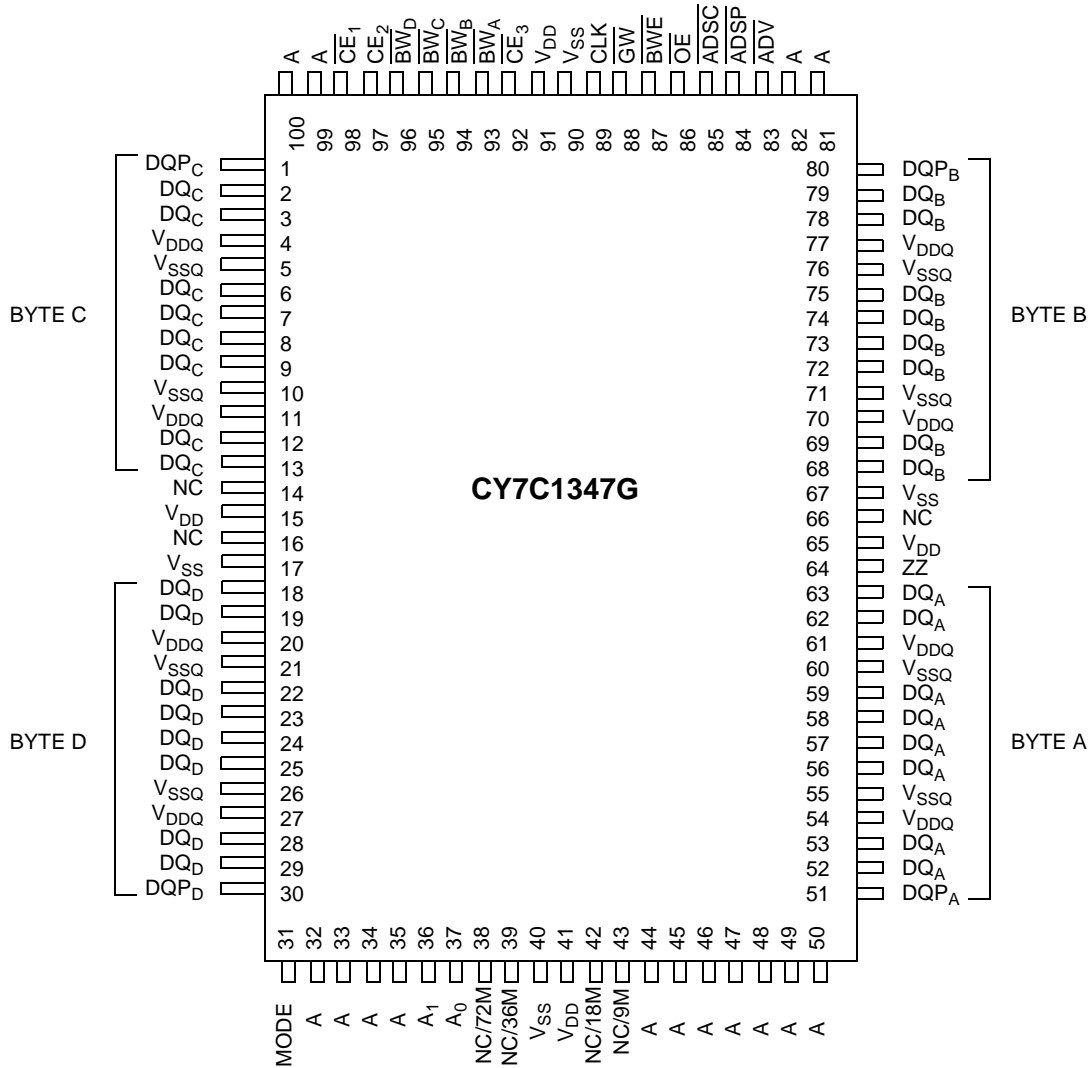


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**Pin Configurations**

**Figure 1. 100-Pin TQFP Pinout**



Pin Configurations

Figure 2. 119-Ball BGA Pinout

	1	2	3	4	5	6	7
A	V <sub>DDQ</sub>	A	A	$\overline{\text{ADSP}}$	A	A	V <sub>DDQ</sub>
B	NC/288 M	CE <sub>2</sub>	A	$\overline{\text{ADSC}}$	A	$\overline{\text{CE}}_3$	NC/576 M
C	NC/144 M	A	A	V <sub>DD</sub>	A	A	NC/1G
D	DQ <sub>C</sub>	DQP <sub>C</sub>	V <sub>SS</sub>	NC	V <sub>SS</sub>	DQP <sub>B</sub>	DQ <sub>B</sub>
E	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>SS</sub>	$\overline{\text{CE}}_1$	V <sub>SS</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
F	V <sub>DDQ</sub>	DQ <sub>C</sub>	V <sub>SS</sub>	$\overline{\text{OE}}$	V <sub>SS</sub>	DQ <sub>B</sub>	V <sub>DDQ</sub>
G	DQ <sub>C</sub>	DQ <sub>C</sub>	$\overline{\text{BW}}_C$	$\overline{\text{ADV}}$	$\overline{\text{BW}}_B$	DQ <sub>B</sub>	DQ <sub>B</sub>
H	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>SS</sub>	$\overline{\text{GW}}$	V <sub>SS</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
J	V <sub>DDQ</sub>	V <sub>DD</sub>	NC	V <sub>DD</sub>	NC	V <sub>DD</sub>	V <sub>DDQ</sub>
K	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>SS</sub>	CLK	V <sub>SS</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
L	DQ <sub>D</sub>	DQ <sub>D</sub>	$\overline{\text{BW}}_D$	NC	$\overline{\text{BW}}_A$	DQ <sub>A</sub>	DQ <sub>A</sub>
M	V <sub>DDQ</sub>	DQ <sub>D</sub>	V <sub>SS</sub>	$\overline{\text{BWE}}$	V <sub>SS</sub>	DQ <sub>A</sub>	V <sub>DDQ</sub>
N	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>SS</sub>	A1	V <sub>SS</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
P	DQ <sub>D</sub>	DQP <sub>D</sub>	V <sub>SS</sub>	A0	V <sub>SS</sub>	DQP <sub>A</sub>	DQ <sub>A</sub>
R	NC	A	MODE	V <sub>DD</sub>	NC	A	NC
T	NC	NC/72M	A	A	A	NC/36M	ZZ
U	V <sub>DDQ</sub>	NC	NC	NC	NC	NC	V <sub>DDQ</sub>

Figure 3. 165-Ball FBGA Pinout

	1	2	3	4	5	6	7	8	9	10	11
A	NC/288 M	A	$\overline{\text{CE}}_1$	$\overline{\text{BW}}_C$	$\overline{\text{BW}}_B$	$\overline{\text{CE}}_3$	$\overline{\text{BWE}}$	$\overline{\text{ADSC}}$	$\overline{\text{ADV}}$	A	NC
B	NC/144 M	A	CE <sub>2</sub>	$\overline{\text{BW}}_D$	$\overline{\text{BW}}_A$	CLK	$\overline{\text{GW}}$	$\overline{\text{OE}}$	$\overline{\text{ADSP}}$	A	NC/576 M
C	DQP <sub>C</sub>	NC	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC/1G	DQP <sub>B</sub>
D	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
E	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
F	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
G	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
H	NC	V <sub>SS</sub>	NC	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	NC	NC	ZZ
J	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
K	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
L	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
M	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
N	DQP <sub>D</sub>	NC	V <sub>DDQ</sub>	V <sub>SS</sub>	NC	NC/18M	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	DQP <sub>A</sub>
P	NC	NC/72 M	A	A	NC	A1	NC	A	A	A	NC/9 M
R	MODE	NC/36 M	A	A	NC	A0	NC	A	A	A	A

**Pin Definitions**

Name	I/O	Description
A <sub>0</sub> , A <sub>1</sub> , A	Input-Synchronous	<b>Address Inputs Used to Select One of the 128 K Address Locations.</b> Sampled at the rising edge of the CLK if ADSP or ADSC is active LOW, and CE <sub>1</sub> , CE <sub>2</sub> , and CE <sub>3</sub> are sampled active. A <sub>[1:0]</sub> feeds the 2-bit counter.
$\overline{BW}_A, \overline{BW}_B, \overline{BW}_C, \overline{BW}_D$	Input-Synchronous	<b>Byte Write Select Inputs, Active LOW.</b> Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	Input-Synchronous	<b>Global Write Enable Input, Active LOW.</b> When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on $\overline{BW}_{[A:D]}$ and $\overline{BWE}$ ).
$\overline{BWE}$	Input-Synchronous	<b>Byte Write Enable Input, Active LOW.</b> Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
CLK	Input-Clock	<b>Clock Input.</b> Used to capture all synchronous inputs to the device. Also used to increment the burst counter when ADV is asserted LOW, during a burst operation.
$\overline{CE}_1$	Input-Synchronous	<b>Chip Enable 1 Input, Active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with CE <sub>2</sub> and CE <sub>3</sub> to select or deselect the device. ADSP is ignored if CE <sub>1</sub> is HIGH. $\overline{CE}_1$ is sampled only when a new external address is loaded.
CE <sub>2</sub>	Input-Synchronous	<b>Chip Enable 2 Input, Active HIGH.</b> Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE <sub>3</sub> to select or deselect the device. CE <sub>2</sub> is sampled only when a new external address is loaded.
$\overline{CE}_3$	Input-Synchronous	<b>Chip Enable 3 Input, Active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE <sub>2</sub> to select or deselect the device. $\overline{CE}_3$ is sampled only when a new external address is loaded.
OE	Input-Asynchronous	<b>Output Enable, Asynchronous Input, Active LOW.</b> Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins. OE is masked during the first clock of a read cycle when emerging from a deselected state.
ADV	Input-Synchronous	<b>Advance Input Signal, Sampled on the Rising Edge of CLK.</b> When asserted, it automatically increments the address in a burst cycle.
ADSP	Input-Synchronous	<b>Address Strobe from Processor, Sampled on the Rising Edge of CLK.</b> When asserted LOW, addresses presented to the device are captured in the address registers. A <sub>[1:0]</sub> are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized. ADSP is ignored when $\overline{CE}_1$ is deasserted HIGH.
ADSC	Input-Synchronous	<b>Address Strobe from Controller, Sampled on the Rising Edge of CLK.</b> When asserted LOW, addresses presented to the device are captured in the address registers. A <sub>[1:0]</sub> are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized.
ZZ	Input-Asynchronous	<b>ZZ "Sleep" Input.</b> This active HIGH input places the device in a non-time-critical "sleep" condition with data integrity preserved. During normal operation, this pin must be LOW or left floating. ZZ pin has an internal pull-down.
DQ <sub>A</sub> , DQ <sub>B</sub> , DQ <sub>C</sub> , DQ <sub>D</sub> , DQP <sub>A</sub> , DQP <sub>B</sub> , DQP <sub>C</sub> , DQP <sub>D</sub>	I/O-Synchronous	<b>Bidirectional Data I/O Lines.</b> As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by OE. When OE is asserted LOW, the pins behave as outputs. When HIGH, DQs and DQPs are placed in a tristate condition.
V <sub>DD</sub>	Power Supply	<b>Power Supply Inputs to the Core of the Device</b>
V <sub>SS</sub>	Ground	<b>Ground for the Core of the Device</b>
V <sub>DDQ</sub>	I/O Power Supply	<b>Power Supply for the I/O circuitry</b>
V <sub>SSQ</sub>	I/O Ground	<b>Ground for the I/O circuitry</b>
MODE	Input-Static	<b>Selects Burst Order.</b> When tied to GND selects linear burst sequence. When tied to V <sub>DDQ</sub> or left floating selects interleaved burst sequence. This is a strap pin and must remain static during device operation. Mode pin has an internal pull-up.
NC, NC/9M, NC/18M, NC/36M, NC/72M, NC/144M, NC/288M, NC/576M, NC/1G	–	<b>No Connects.</b> Not internally connected to the die. NC/9M, NC/18M, NC/36M, NC/72M, NC/144M, NC/288M, NC/576M, and NC/1G are address expansion pins that are not internally connected to the die.

## Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise ( $t_{CO}$ ) is 2.6 ns (250 MHz device).

The CY7C1347G supports secondary cache in systems using either a linear or interleaved burst sequence. The linear burst sequence is suited for processors that use a linear burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the Address Strobe from Processor (ADSP) or the Address Strobe from Controller (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the Byte Write Enable (BWE) and Byte Write Select ( $BW_{[A:D]}$ ) inputs. A Global Write Enable (GW) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self timed write circuitry.

Three synchronous Chip Selects ( $\overline{CE}_1$ ,  $CE_2$ ,  $\overline{CE}_3$ ) and an asynchronous Output Enable (OE) provide for easy bank selection and output tristate control. ADSP is ignored if  $CE_1$  is HIGH.

### Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) ADSP or ADSC is asserted LOW, (2)  $\overline{CE}_1$ ,  $CE_2$ ,  $CE_3$  are all asserted active, and (3) the write signals (GW, BWE) are all deasserted HIGH. ADSP is ignored if  $\overline{CE}_1$  is HIGH. The address presented to the address inputs ( $A_{[16:0]}$ ) is stored into the address advancement logic and the Address Register while being presented to the memory core. The corresponding data is allowed to propagate to the input of the Output Registers. At the rising edge of the next clock the data is allowed to propagate through the Output Register and onto the data bus within 2.6 ns (250 MHz device) if OE is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state, its outputs are always tristated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the OE signal. Consecutive single read cycles are supported. After the SRAM is deselected at clock rise by the chip select and either ADSP or ADSC signals, its output tristates immediately.

### Single Write Accesses Initiated by ADSP

This access is initiated when both of the following conditions are satisfied at clock rise: (1) ADSP is asserted LOW, and (2)  $\overline{CE}_1$ ,  $CE_2$ ,  $CE_3$  are all asserted active. The address presented to  $A_{[16:0]}$  is loaded into the Address Register and the address advancement logic while being delivered to the RAM core. The write signals (GW, BWE, and  $BW_{[A:D]}$ ) and ADV inputs are ignored during this first cycle.

ADSP-triggered write accesses require two clock cycles to complete. If  $\overline{GW}$  is asserted LOW on the second clock rise, the data presented to the DQs and DQPs inputs is written into the corresponding address location in the RAM core. If  $\overline{GW}$  is HIGH, then the write operation is controlled by BWE and  $BW_{[A:D]}$  signals. The CY7C1347G provides byte write capability that is described in Table 2 on page 9. Asserting the Byte Write Enable input (BWE) with the selected Byte Write ( $BW_{[A:D]}$ ) input selectively writes to only the desired bytes.

Bytes not selected during a byte write operation remain unaltered. A synchronous self timed write mechanism is provided to simplify the write operations.

Because the CY7C1347G is a common I/O device, the Output Enable (OE) must be deasserted HIGH before presenting data to the DQs and DQPs inputs. Doing so tristates the output drivers. As a safety precaution, DQs and DQPs are automatically tristated whenever a write cycle is detected, regardless of the state of OE.

### Single Write Accesses Initiated by ADSC

ADSC write accesses are initiated when the following conditions are satisfied: (1) ADSC is asserted LOW, (2) ADSP is deasserted HIGH, (3)  $\overline{CE}_1$ ,  $CE_2$ ,  $CE_3$  are all asserted active, and (4) the appropriate combination of the write inputs (GW, BWE, and  $BW_{[A:D]}$ ) are asserted active to conduct a write to the desired byte(s). ADSC-triggered write accesses require a single clock cycle to complete. The address presented to  $A_{[16:0]}$  is loaded into the address register and the address advancement logic while being delivered to the RAM core. The ADV input is ignored during this cycle. If a global write is conducted, the data presented to the DQs and DQPs is written into the corresponding address location in the RAM core. If a byte write is conducted, only the selected bytes are written. Bytes not selected during a byte write operation remain unaltered. A synchronous self timed write mechanism has been provided to simplify the write operations.

Because the CY7C1347G is a common I/O device, the Output Enable (OE) must be deasserted HIGH before presenting data to the DQs and DQPs inputs. Doing so tristates the output drivers. As a safety precaution, DQs and DQPs are automatically tristated whenever a write cycle is detected, regardless of the state of OE.

### Burst Sequences

The CY7C1347G provides a two-bit wraparound counter, fed by  $A_{[1:0]}$ , that implements either an interleaved or linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The linear burst sequence is designed to support processors that follow a linear burst sequence. The burst sequence is user-selectable through the MODE input.

Asserting  $\overline{ADV}$  LOW at clock rise automatically increments the burst counter to the next address in the burst sequence. Both read and write burst operations are supported.

### Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation "sleep" mode. Two clock cycles are required to enter into or exit from this "sleep" mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the "sleep" mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected before entering the "sleep" mode.  $CE_1$ ,  $CE_2$ ,  $CE_3$ , ADSP, and ADSC must remain inactive for the duration of  $t_{ZZREC}$  after the ZZ input returns LOW.

### Interleaved Burst Sequence

First Address	Second Address	Third Address	Fourth Address
$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

### Linear Burst Sequence

First Address	Second Address	Third Address	Fourth Address
$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

### ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
$I_{DDZZ}$	Snooze mode standby current	$ZZ \geq V_{DD} - 0.2V$		40	mA
$t_{ZZS}$	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2V$		$2t_{CYC}$	ns
$t_{ZZREC}$	ZZ recovery time	$ZZ \leq 0.2V$	$2t_{CYC}$		ns
$t_{ZZI}$	ZZ Active to snooze current	This parameter is sampled		$2t_{CYC}$	ns
$t_{RZZI}$	ZZ Inactive to exit snooze current	This parameter is sampled	0		ns

Table 1. Truth Table

The truth table for part number CY7C1347G follow. [2, 3, 4, 5, 6]

Next Cycle	Add. Used	$\overline{CE}_1$	$CE_2$	$\overline{CE}_3$	ZZ	ADSP	ADSC	ADV	WRITE	$\overline{OE}$	CLK	DQ
Deselect cycle, power-down	None	H	X	X	L	X	L	X	X	X	L-H	Tristate
Deselect cycle, power-down	None	L	L	X	L	L	X	X	X	X	L-H	Tristate
Deselect cycle, power-down	None	L	X	H	L	L	X	X	X	X	L-H	Tristate
Deselect cycle, power-down	None	L	L	X	L	H	L	X	X	X	L-H	Tristate
Deselect cycle, power-down	None	L	X	H	L	H	L	X	X	X	L-H	Tristate
Snooze mode, power-down	None	X	X	X	H	X	X	X	X	X	X	Tristate

Note

- X = "Do not Care." H = Logic HIGH, L = Logic LOW.
- WRITE = L when any one or more Byte Write Enable signals ( $\overline{BW}_A$ ,  $\overline{BW}_B$ ,  $\overline{BW}_C$ ,  $\overline{BW}_D$ ) and  $\overline{BWE} = L$  or  $\overline{GW} = L$ . WRITE = H when all Byte Write Enable signals ( $\overline{BW}_A$ ,  $\overline{BW}_B$ ,  $\overline{BW}_C$ ,  $\overline{BW}_D$ ), BWE,  $\overline{GW} = H$ .
- The DQ pins are controlled by the current cycle and the  $\overline{OE}$  signal.  $\overline{OE}$  is asynchronous and is not sampled with the clock.
- The SRAM always initiates a read cycle when ADSP is asserted, regardless of the state of  $\overline{GW}$ , BWE, or  $\overline{BW}_{[A:D]}$ . Writes may occur only on subsequent clocks after the ADSP or with the assertion of ADSC. As a result,  $\overline{OE}$  must be driven HIGH before the start of the write cycle to allow the outputs to tristate.  $\overline{OE}$  is a do not care for the remainder of the write cycle.
- $\overline{OE}$  is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tristate when  $\overline{OE}$  is inactive or when the device is deselected, and all data bits behave as output when OE is active (LOW).



**Table 1. Truth Table**

The truth table for part number CY7C1347G follow. [2, 3, 4, 5, 6] (continued)

Next Cycle	Add. Used	$\overline{CE}_1$	$CE_2$	$\overline{CE}_3$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	L	L-H	Q
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	H	L-H	Tristate
Write Cycle, Begin Burst	External	L	H	L	L	H	L	X	L	X	L-H	D
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	L	L-H	Q
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	H	L-H	Tristate
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	Tristate
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	Tristate
Write cycle, continue burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
Write cycle, continue burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read cycle, suspend burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read cycle, suspend burst	Current	X	X	X	L	H	H	H	H	H	L-H	Tristate
Read cycle, suspend burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read cycle, suspend burst	Current	H	X	X	L	X	H	H	H	H	L-H	Tristate
Write cycle, suspend burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write cycle, suspend burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

**Table 2. Partial Truth Table for Read/Write**

The partial truth table for read/write for part number CY7C1347G follow. [2, 7]

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_D$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{BW}_A$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write byte A – $DQ_A$	H	L	H	H	H	L
Write byte B – $DQ_B$	H	L	H	H	L	H
Write bytes B, A	H	L	H	H	L	L
Write byte C – $DQ_C$	H	L	H	L	H	H
Write bytes C, A	H	L	H	L	H	L
Write bytes C, B	H	L	H	L	L	H
Write bytes C, B, A	H	L	H	L	L	L
Write byte D – $DQ_D$	H	L	L	H	H	H
Write bytes D, A	H	L	L	H	H	L
Write bytes D, B	H	L	L	H	L	H
Write bytes D, B, A	H	L	L	H	L	L
Write bytes D, C	H	L	L	L	H	H
Write bytes D, C, A	H	L	L	L	H	L
Write bytes D, C, B	H	L	L	L	L	H
Write all bytes	H	L	L	L	L	L
Write all bytes	L	X	X	X	X	X

### Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

- Storage temperature ..... -65 °C to +150 °C
- Ambient temperature with power applied..... -55 °C to +125 °C
- Supply voltage on V<sub>DD</sub> relative to GND ..... -0.5 V to +4.6 V
- Supply voltage on V<sub>DDQ</sub> relative to GND..... -0.5 V to +V<sub>DD</sub>
- DC voltage applied to outputs in high Z State ..... -0.5 V to V<sub>DD</sub> + 0.5 V
- DC input voltage ..... -0.5 V to V<sub>DD</sub> + 0.5 V
- Current into outputs (LOW) ..... 20 mA
- Static discharge voltage..... > 2001 V (MIL-STD-883, Method 3015)
- Latch-up Current..... > 200 mA

### Operating Range

Range	Ambient Temperature	V <sub>DD</sub>	V <sub>DDQ</sub>
Commercial	0 °C to +70 °C	3.3 V	2.5 V -5%
Industrial	-40 °C to +85 °C	-5%/+10%	to V <sub>DD</sub>

### Electrical Characteristics

Over the Operating Range<sup>[8, 9]</sup>

Parameter	Description	Test Conditions	Min	Max	Unit
V <sub>DD</sub>	Power supply voltage		3.135	3.6	V
V <sub>DDQ</sub>	I/O supply voltage		2.375	V <sub>DD</sub>	V
V <sub>OH</sub>	Output HIGH voltage	For 3.3 V I/O, I <sub>OH</sub> = -4.0 mA	2.4		V
		For 2.5 V I/O, I <sub>OH</sub> = -1.0 mA	2.0		V
V <sub>OL</sub>	Output LOW voltage	For 3.3 V I/O, I <sub>OL</sub> = 8.0 mA		0.4	V
		For 2.5 V I/O, I <sub>OL</sub> = 1.0 mA		0.4	V
V <sub>IH</sub>	Input HIGH voltage <sup>[8]</sup>	For 3.3 V I/O	2.0	V <sub>DD</sub> + 0.3 V	V
		For 2.5 V I/O	1.7	V <sub>DD</sub> + 0.3 V	V
V <sub>IL</sub>	Input LOW voltage <sup>[8]</sup>	For 3.3 V I/O	-0.3	0.8	V
		For 2.5 V I/O	-0.3	0.7	V
I <sub>X</sub>	Input leakage current except ZZ and MODE	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub>	-5	5	μA
	Input current of MODE	Input = V <sub>SS</sub>	-30		μA
		Input = V <sub>DD</sub>		5	μA
	Input current of ZZ	Input = V <sub>SS</sub>	-5		μA
Input = V <sub>DD</sub>			30	μA	
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub> , output disabled	-5	5	μA

**Note**

7. This table is only a partial listing of the byte write combinations. Any combination of BW<sub>x</sub> is valid. Appropriate write is based on which byte write is active.

### Neutron Soft Error Immunity

Parameter	Description	Test Conditions	Typ	Max*	Unit
LSBU	Logical single-bit upsets	25 °C	361	394	FIT/Mb
LMBU	Logical multi-bit upsets	25 °C	0	0.01	FIT/Mb
SEL	Single event latch-up	85 °C	0	0.1	FIT/Dev

\* No LMBU or SEL events occurred during testing; this column represents a statistical  $\chi^2$ , 95% confidence limit calculation. For more details refer to Application Note, Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates – AN54908.

**Electrical Characteristics** (continued)

 Over the Operating Range<sup>[8, 9]</sup>

Parameter	Description	Test Conditions	Min	Max	Unit
I <sub>DD</sub>	V <sub>DD</sub> operating supply current	V <sub>DD</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>CYC</sub>	4 ns cycle, 250 MHz	325	mA
			5 ns cycle, 200 MHz	265	mA
			6 ns cycle, 166 MHz	240	mA
			7.5 ns cycle, 133 MHz	225	mA
I <sub>SB1</sub>	Automatic CE power-down current—TTL inputs	Max. V <sub>DD</sub> , device deselected, V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub> = 1/t <sub>CYC</sub>	4 ns cycle, 250 MHz	120	mA
			5 ns cycle, 200 MHz	110	mA
			6 ns cycle, 166 MHz	100	mA
			7.5 ns cycle, 133 MHz	90	mA
I <sub>SB2</sub>	Automatic CE power-down current—CMOS inputs	Max. V <sub>DD</sub> , device deselected, V <sub>IN</sub> ≤ 0.3 V or V <sub>IN</sub> ≥ V <sub>DDQ</sub> - 0.3 V, f = 0	All speeds	40	mA
I <sub>SB3</sub>	Automatic CE power-down current—CMOS inputs	Max. V <sub>DD</sub> , device deselected, or V <sub>IN</sub> ≤ 0.3 V or V <sub>IN</sub> ≥ V <sub>DDQ</sub> - 0.3 V, f = f <sub>MAX</sub> = 1/t <sub>CYC</sub>	4 ns cycle, 250 MHz	105	mA
			5 ns cycle, 200 MHz	95	mA
			6 ns cycle, 166 MHz	85	mA
			7.5 ns cycle, 133 MHz	75	mA
I <sub>SB4</sub>	Automatic CE power-down current—TTL inputs	Max. V <sub>DD</sub> , device deselected, V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = 0		45	mA

**Notes**

8. Overshoot: V<sub>IH</sub>(AC) < V<sub>DD</sub> + 1.5 V (pulse width less than t<sub>CYC</sub>/2). Undershoot: V<sub>IL</sub>(AC) > -2 V (pulse width less than t<sub>CYC</sub>/2).  
 9. t<sub>power-up</sub>: assumes a linear ramp from 0V to V<sub>DD</sub>(min) within 200 ms. During this time V<sub>IH</sub> < V<sub>DD</sub> and V<sub>DDQ</sub> ≤ V<sub>DD</sub>.

## Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	100 TQFP Max	119 BGA Max	165 FBGA Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25\text{ }^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{DD} = 3.3\text{ V}$ , $V_{DDQ} = 3.3\text{ V}$	5	5	5	pF
$C_{CLK}$	Clock input capacitance		5	5	5	pF
$C_{IO}$	I/O capacitance		5	7	7	pF

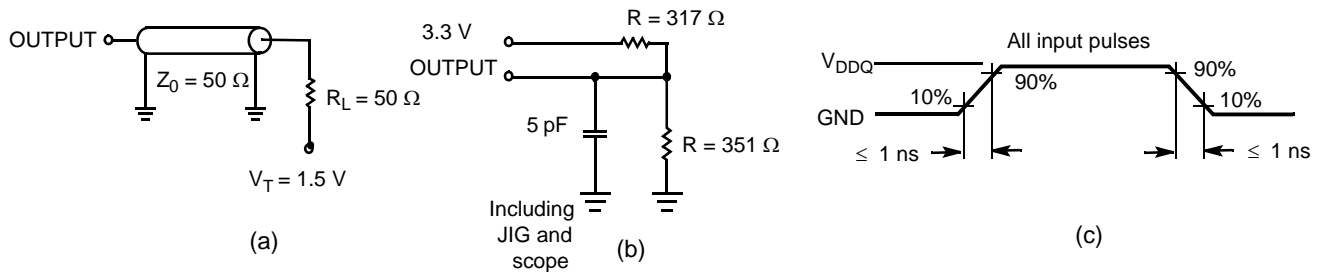
## Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

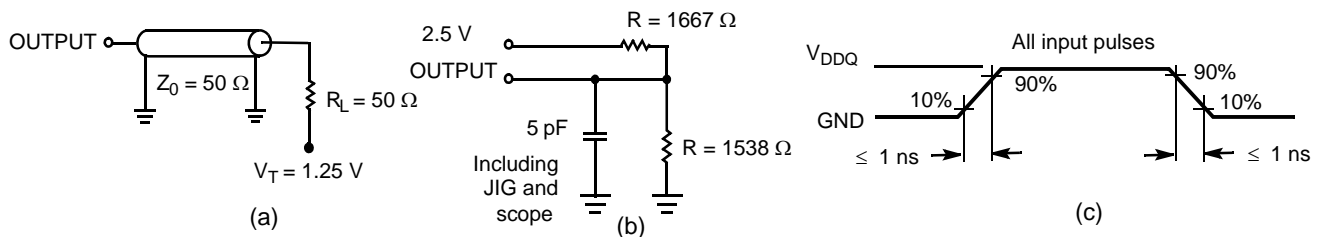
Parameter	Description	Test Conditions	100 TQFP Package	119 BGA Package	165 FBGA Package	Unit
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	30.32	34.1	20.3	$^\circ\text{C/W}$
$\Theta_{JC}$	Thermal resistance (junction to case)		6.85	14.0	4.6	$^\circ\text{C/W}$

Figure 4. AC Test Loads and Waveforms

### 3.3-V I/O Test Load



### 2.5-V I/O Test Load



## Switching Characteristics

Over the Operating Range<sup>[14, 15]</sup>

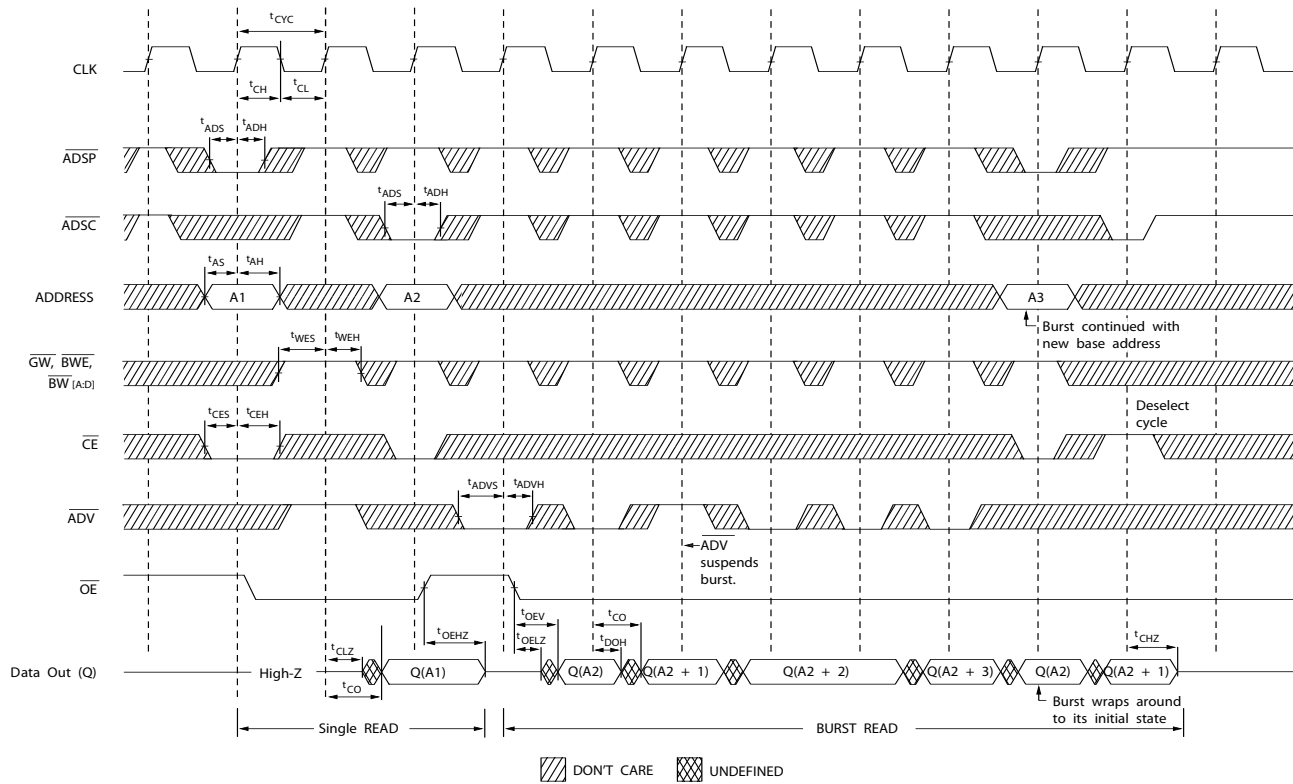
Parameter	Description	-250		-200		-166		-133		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>POWER</sub>	V <sub>DD</sub> (Typical) to the first Access <sup>[10]</sup>	1		1		1		1		ms
<b>Clock</b>										
t <sub>CYC</sub>	Clock cycle time	4.0		5.0		6.0		7.5		ns
t <sub>CH</sub>	Clock HIGH	1.7		2.0		2.5		3.0		ns
t <sub>CL</sub>	Clock LOW	1.7		2.0		2.5		3.0		ns
<b>Output Times</b>										
t <sub>CO</sub>	Data output valid after CLK rise		2.6		2.8		3.5		4.0	ns
t <sub>DOH</sub>	Data output hold after CLK rise	1.0		1.0		1.5		1.5		ns
t <sub>CLZ</sub>	Clock to low Z <sup>[11, 12, 13]</sup>	0		0		0		0		ns
t <sub>CHZ</sub>	Clock to high Z <sup>[11, 12, 13]</sup>		2.6		2.8		3.5		4.0	ns
t <sub>OEV</sub>	$\overline{OE}$ LOW to output valid		2.6		2.8		3.5		4.5	ns
t <sub>OEZ</sub>	$\overline{OE}$ LOW to output low Z <sup>[11, 12, 13]</sup>	0		0		0		0		ns
t <sub>OEZ</sub>	$\overline{OE}$ HIGH to output high Z <sup>[11, 12, 13]</sup>		2.6		2.8		3.5		4.0	ns
<b>Setup Times</b>										
t <sub>AS</sub>	Address setup before CLK rise	1.2		1.2		1.5		1.5		ns
t <sub>ADS</sub>	$\overline{ADSC}$ , $\overline{ADSP}$ setup before CLK rise	1.2		1.2		1.5		1.5		ns
t <sub>ADVS</sub>	$\overline{ADV}$ setup before CLK rise	1.2		1.2		1.5		1.5		ns
t <sub>WES</sub>	$\overline{GW}$ , $\overline{BWE}$ , $\overline{BW}_X$ setup before CLK rise	1.2		1.2		1.5		1.5		ns
t <sub>DS</sub>	Data input setup before CLK rise	1.2		1.2		1.5		1.5		ns
t <sub>CES</sub>	Chip enable setup before CLK rise	1.2		1.2		1.5		1.5		ns
<b>Hold Times</b>										
t <sub>AH</sub>	Address hold after CLK rise	0.3		0.5		0.5		0.5		ns
t <sub>ADH</sub>	$\overline{ADSP}$ , $\overline{ADSC}$ hold after CLK rise	0.3		0.5		0.5		0.5		ns
t <sub>ADVH</sub>	$\overline{ADV}$ hold after CLK Rise	0.3		0.5		0.5		0.5		ns
t <sub>WEH</sub>	$\overline{GW}$ , $\overline{BWE}$ , $\overline{BW}_X$ hold after CLK rise	0.3		0.5		0.5		0.5		ns
t <sub>DH</sub>	Data input hold after CLK rise	0.3		0.5		0.5		0.5		ns
t <sub>CEH</sub>	Chip enable hold after CLK rise	0.3		0.5		0.5		0.5		ns

### Notes

- This part has an internal voltage regulator; t<sub>POWER</sub> is the time that the power must be supplied above V<sub>DD</sub>(min) initially before a read or write operation can be initiated.
- t<sub>CHZ</sub>, t<sub>CLZ</sub>, t<sub>OEZ</sub>, and t<sub>OEZ</sub> are specified with AC test conditions shown in part (b) of [AC Test Loads and Waveforms on page 12](#). Transition is measured ±200 mV from steady-state voltage.
- At any voltage and temperature, t<sub>OEZ</sub> is less than t<sub>OEZ</sub> and t<sub>CHZ</sub> is less than t<sub>CLZ</sub> to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High Z before Low Z under the same system conditions.
- This parameter is sampled and not 100% tested.
- Timing references level is 1.5 V when V<sub>DDQ</sub> = 3.3 V and is 1.25 V when V<sub>DDQ</sub> = 2.5 V on all datasheets.
- Test conditions shown in (a) of [AC Test Loads and Waveforms on page 12](#) unless otherwise noted.

## Switching Waveforms

Figure 5. Read Cycle Timing<sup>[16]</sup>

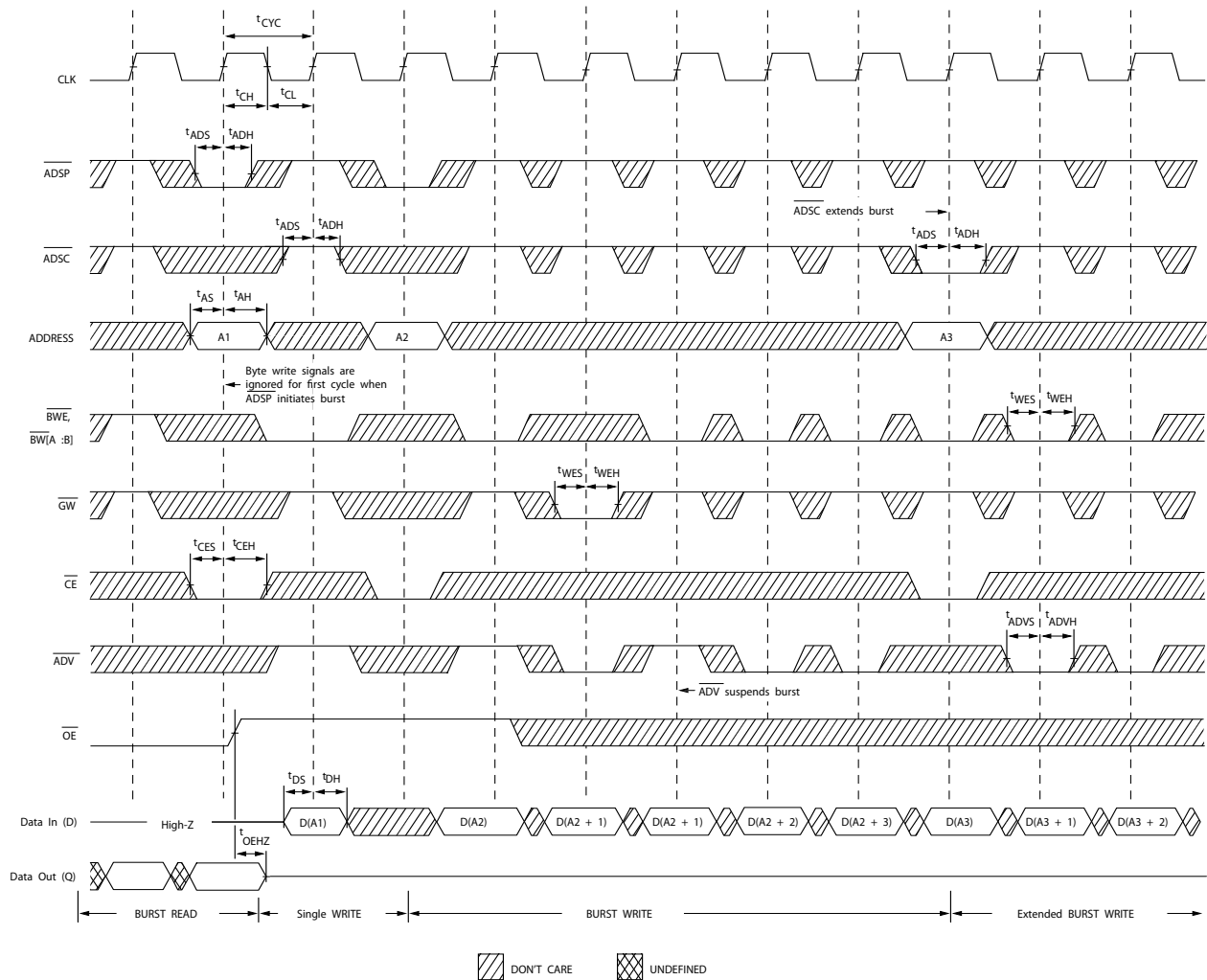


**Note**

16. In this diagram, when  $\overline{CE}$  is LOW,  $\overline{CE}_1$  is LOW,  $CE_2$  is HIGH, and  $\overline{CE}_3$  is LOW. When  $\overline{CE}$  is HIGH,  $\overline{CE}_1$  is HIGH,  $CE_2$  is LOW, or  $\overline{CE}_3$  is HIGH.

Switching Waveforms (continued)

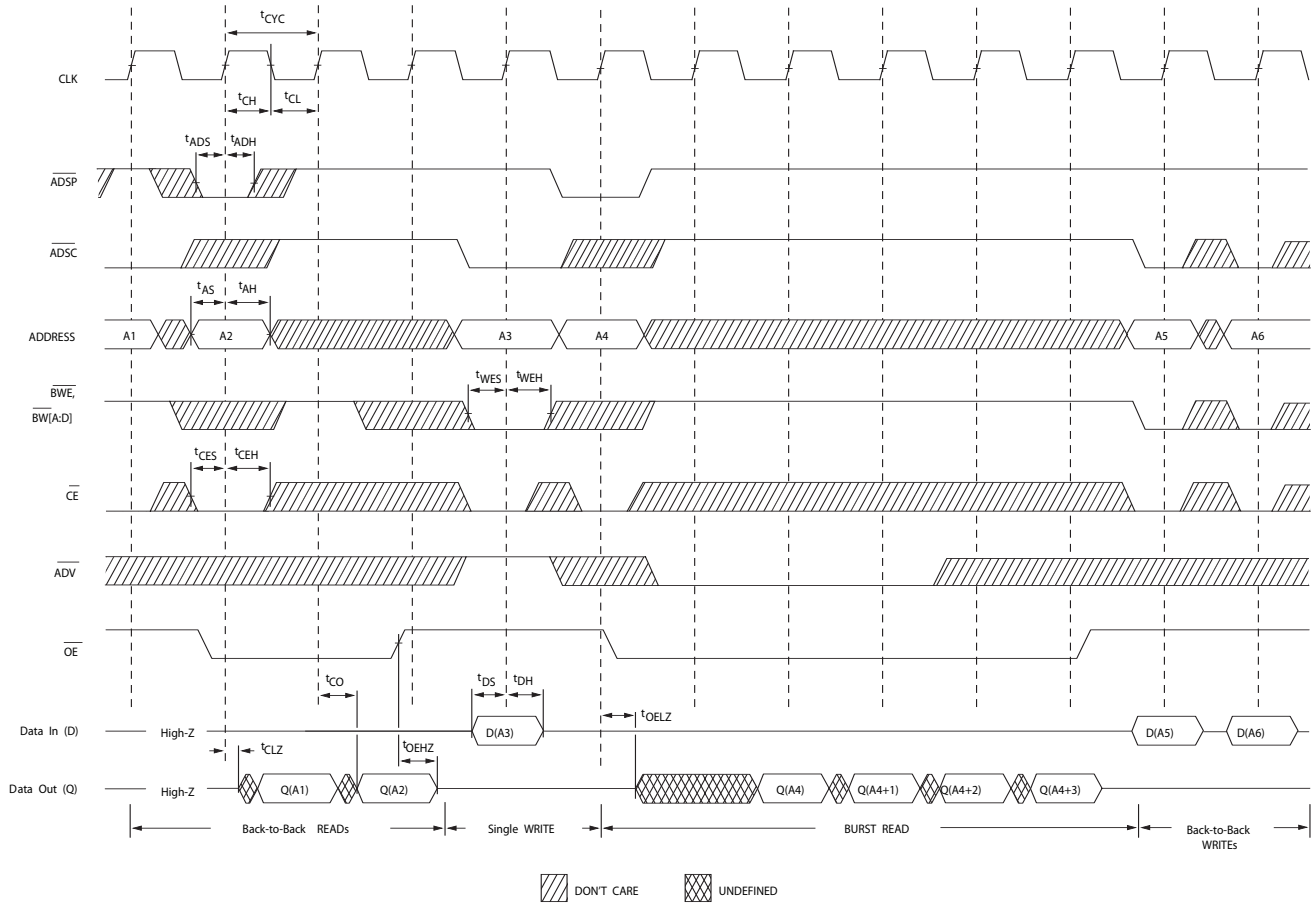
Figure 6. Write Cycle Timing<sup>[16, 17]</sup>



**Note**  
 17. Full width write can be initiated by either  $\overline{GW}$  LOW, or by  $\overline{GW}$  HIGH,  $\overline{BWE}$  LOW, and  $BW_x$  LOW.

Switching Waveforms (continued)

Figure 7. Read/Write Cycle Timing [16, 18, 19]



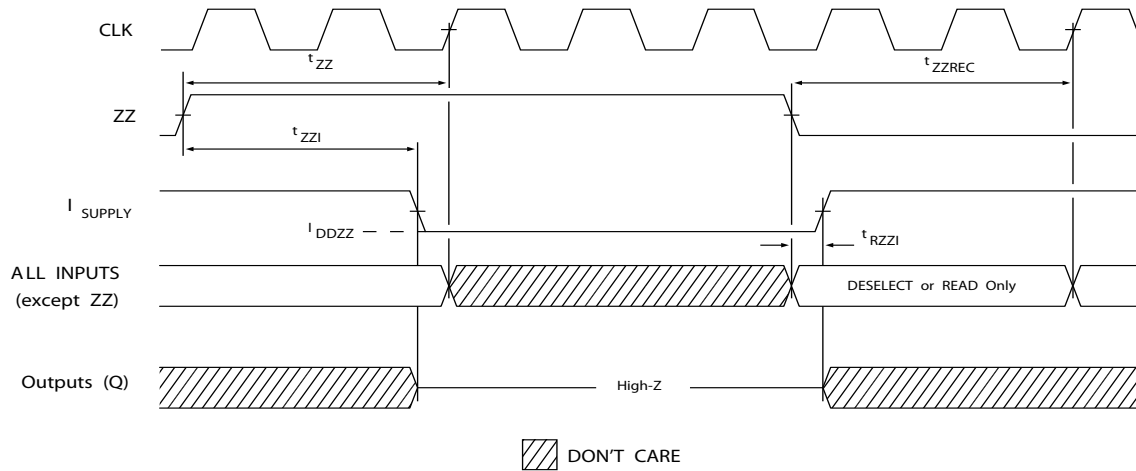
Notes

- 18. The data bus (Q) remains in High Z following a write cycle, unless a new read access is initiated by  $\overline{ADSP}$  or  $\overline{ADSC}$ .
- 19.  $\overline{GW}$  is HIGH.



Switching Waveforms (continued)

Figure 8. ZZ Mode Timing<sup>[20, 21]</sup>



Notes

- 20. Device must be deselected when entering ZZ mode. See Table 1 on page 8 for all possible signal conditions to deselect the device.
- 21. DQs are in High Z when exiting ZZ sleep mode.

**Ordering Information**

The table below contains only the parts that are currently available. If you don't see what you are looking for, please contact your local sales representative. For more information, visit the Cypress website at [www.cypress.com](http://www.cypress.com) and refer to the product summary page at <http://www.cypress.com/products>

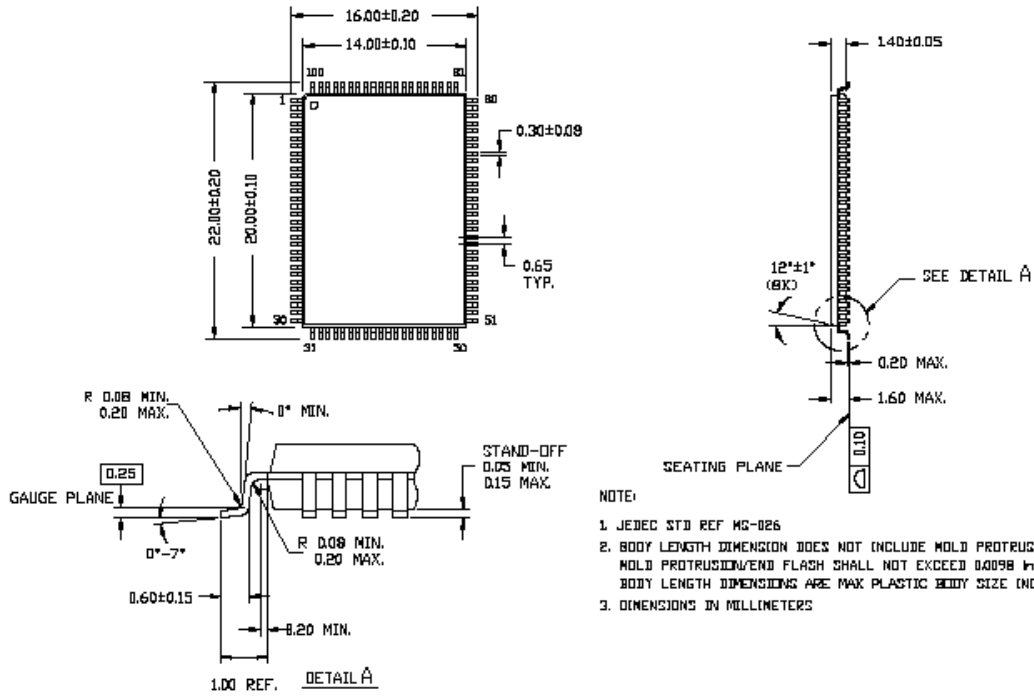
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**Table 3. Ordering Information**

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
133	CY7C1347G-133AXC	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Commercial
	CY7C1347G-133BGXC	51-85115	119-Ball Ball Grid Array (14 x 22 x 2.4 mm) Pb-Free	
166	CY7C1347G-166AXC	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Commercial
	CY7C1347G-166AXI	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Industrial
200	CY7C1347G-200AXC	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Commercial
250	CY7C1347G-250AXC	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Commercial

Package Diagrams

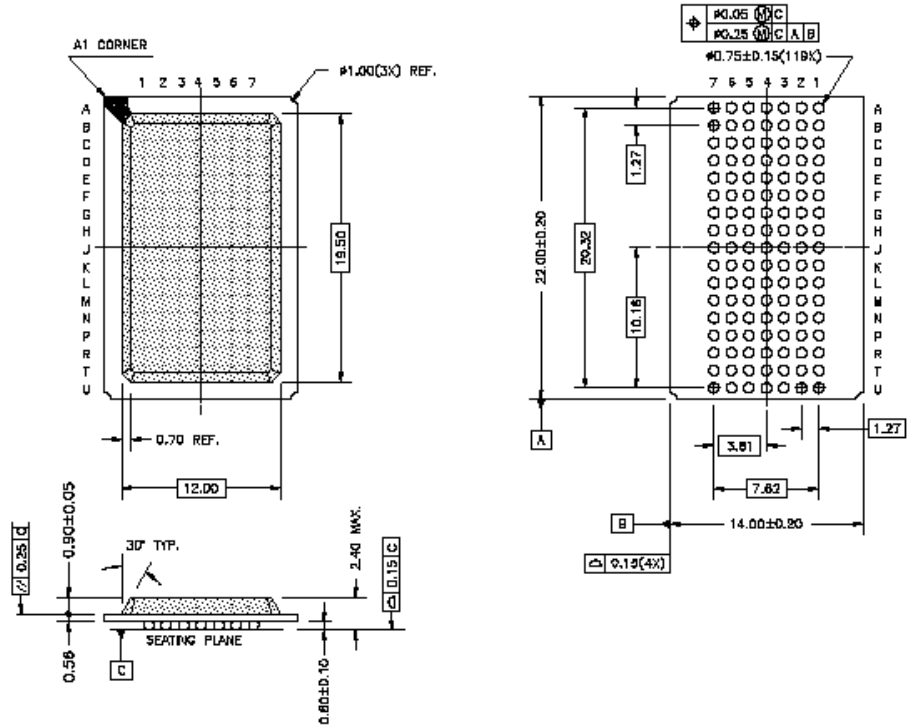
Figure 9. 100-Pin Thin Plastic Quad Flatpack (14 × 20 × 1.4 mm)



51-85050 \*C

Package Diagrams (continued)

Figure 10. 119-Ball BGA (14 × 22 × 2.4 mm)



51-85115 °C



**Document History Page**

Document Title: CY7C1347G 4-Mbit (128 K x 36) Pipelined Sync SRAM Document Number: 38-05516				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	224364	RKF	See ECN	New datasheet
*A	276690	VBL	See ECN	Changed TQFP package in Ordering Information section to Pb-Free TQFP Added comment of BG and BZ Pb-Free package availability
*B	333625	SYT	See ECN	Removed 225 MHz and 100 MHz speed grades Modified Address Expansion balls in the pinouts for 100 TQFP Package as per JEDEC standards and updated the Pin Definitions accordingly Modified $V_{OL}$ , $V_{OH}$ test conditions Replaced TBDs for $\theta_{JA}$ and $\theta_{JC}$ to their respective values on the Thermal Resistance table Changed the package name for 100 TQFP from A100RA to A101 Removed comment on the availability of BG Pb-Free package Updated the Ordering Information by shading and unshading MPNs as per availability
*C	419256	R XU	See ECN	Converted from Preliminary to Final. Changed address of Cypress Semiconductor Corporation on Page #1 from "3901 North First Street" to "198 Champion Court" Swapped typo $CE_2$ and $CE_3$ in the Truth Table column heading on Page #6 Modified test condition from $V_{IH} \leq V_{DD}$ to $V_{IH} < V_{DD}$ . Modified test condition from $V_{DDQ} < V_{DD}$ to $V_{DDQ} \leq V_{DD}$ Modified "Input Load" to "Input Leakage Current except ZZ and MODE" in the Electrical Characteristics Table. Replaced Package Name column with Package Diagram in the Ordering Information table. Replaced Package Diagram of 51-85050 from *A to *B Replaced Package Diagram of 51-85180 from ** to *A Updated the Ordering Information.
*D	480124	VKN	See ECN	Added the Maximum Rating for Supply Voltage on $V_{DDQ}$ Relative to GND. Updated the Ordering Information table.
*E	1078184	VKN	See ECN	Corrected write timing diagram on page 12
*F	2633279	NXR/AESA	01/15/09	Updated Ordering Information and data sheet template.
*G	2756998	VKN	08/28/09	Included Soft Error Immunity Data Modified Ordering Information table by including parts that are available and modified the disclaimer for the Ordering information. Updated Package Diagram for spec 51-85180.
*H	2998771	NJY	08/02/10	Template update. Updated package diagrams to latest revision. 51-85050 – *B to *C 51-85115 – *B to *C 51-85180 – *B to *C

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