

### FEATURES

**Full-scale frequency (up to 2 MHz) set by external system clock**

**Extremely low linearity error (0.005% max at 1 MHz FS, 0.02% max at 2 MHz FS)**

**No critical external components required**

**Accurate 5 V reference voltage**

**Low drift (25 ppm/°C max)**

**Dual- or single-supply operation**

**Voltage or current input**

**MIL-STD-883 compliant versions available**

### PRODUCT DESCRIPTION

The AD652 synchronous voltage-to-frequency converter (SVFC) is a powerful building block for precision analog-to-digital conversion, offering typical nonlinearity of 0.002% (0.005% maximum) at a 100 kHz output frequency. The inherent monotonicity of the transfer function and wide range of clock frequencies allow the conversion time and resolution to be optimized for specific applications.

The AD652 uses a variation of the charge-balancing technique to perform the conversion function. The AD652 uses an external clock to define the full-scale output frequency, rather than relying on the stability of an external capacitor. The result is a more stable, more linear transfer function, with significant application benefits in both single- and multichannel systems.

Gain drift is minimized using a precision low drift reference and low TC, on-chip, thin-film scaling resistors. Furthermore, initial gain error is reduced to less than 0.5% by the use of laser-wafer-trimming.

The analog and digital sections of the AD652 have been designed to allow operation from a single-ended power source, simplifying its use with isolated power supplies.

The AD652 is available in five performance grades. The 20-lead PLCC-packaged JP and KP grades are specified for operation over the 0°C to +70°C commercial temperature range. The 16-lead CERDIP-packaged AQ and BQ grades are specified for operation over the -40°C to +85°C industrial temperature range. The AD652SQ is available for operation over the full -55°C to +125°C extended temperature range.

### PRODUCT HIGHLIGHTS

1. The use of an external clock to set the full-scale frequency allows the AD652 to achieve linearity and stability far superior to other monolithic VFCs. By using the same clock to drive the AD652 and set the counting period (through a suitable divider), conversion accuracy is maintained independent of variations in clock frequency.
2. The AD652 synchronous VFC requires only one external component (a noncritical integrator capacitor) for operation.
3. The AD652 includes a buffered, accurate 5 V reference.
4. The AD652's clock input is TTL and CMOS compatible and can also be driven by sources referred to the negative power supply. The flexible open-collector output stage provides sufficient current sinking capability for TTL and CMOS logic, as well as for optical couplers and pulse transformers. A capacitor-programmable one-shot is provided for selection of optimum output pulse width for power reduction.
5. The AD652 can also be configured for use as a synchronous F/V converter for isolated analog signal transmission.
6. The AD652 is available in versions compliant with MILSTD-883. Refer to the Analog Devices Military Products Databook or current AD652/883B data sheet for detailed specifications.

### FUNCTIONAL BLOCK DIAGRAM



Figure 1.

### Rev. C

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# AD652

## ORDERING GUIDE

Model	Gain Drift, 100 kHz	1 MHz Linearity (%)	Specified Temperature Range	Package Options <sup>1</sup>
AD652JP	50 ppm/°C max	0.02 max	0°C to +70°C	PLCC (P-20A)
AD652JP-REEL	50 ppm/°C max	0.02 max	0°C to +70°C	PLCC (P-20A)
AD652JP-REEL7	50 ppm/°C max	0.02 max	0°C to +70°C	PLCC (P-20A)
AD652KP	25 ppm/°C max	0.005 max	0°C to +70°C	PLCC (P-20A)
AD652KP-REEL	25 ppm/°C max	0.005 max	0°C to +70°C	PLCC (P-20A)
AD652AQ <sup>2</sup>	50 ppm/°C max	0.02 max	−40°C to +85°C	CERDIP (Q-16)
AD652BQ <sup>2</sup>	25 ppm/°C max	0.005 max	−40°C to +85°C	CERDIP (Q-16)
AD652SE/883B <sup>2</sup>	50 ppm/°C max	0.02 max	−55°C to +125°C	LCC (E-20A)
AD652SQ <sup>2</sup>	50 ppm/°C max	0.02 max	−55°C to +125°C	CERDIP (Q-16)
AD652SQ/883B <sup>2</sup>	50 ppm/°C max	0.02 max	−55°C to +125°C	CERDIP (Q-16)

<sup>1</sup> P = Plastic Leaded Chip Carrier; Q = CERDIP, E = Leadless Chip Carrier.

<sup>2</sup> For details on grade and package offerings screened in accordance with MILSTD-883, refer to the Analog Devices Military Products Databook or current AD652/883 data sheet.