Ultrafast 7 ns Single Supply Comparator

AD8561

ANALOG DEVICES

FEATURES
7 ns Propagation Delay at 5 V
Single Supply Operation: 3 V to 10 V
Low Power
Latch Function
TSSOP Packages

APPLICATIONS
High Speed Timing
Clock Recovery and Clock Distribution
Line Receivers
Digital Communications
Phase Detectors
High Speed Sampling
Read Channel Detection
PCMCIA Cards
Upgrade for LT1016 Designs

PIN CONFIGURATIONS

8-Lead Narrow Body SO (SO-8)

8-Lead Plastic DIP (N-8)

8-Lead TSSOP (RU-8)

GENERAL DESCRIPTION

The AD8561 is a single 7 ns comparator with separate input and output sections. Separate supplies enable the input stage to be operated from ±5 V dual supplies and +5 V single supplies.
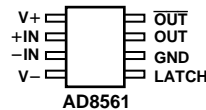
Fast 7 ns propagation delay makes the AD8561 a good choice for timing circuits and line receivers. Propagation delays for rising and falling signals are closely matched and track over temperature. This matched delay makes the AD8561 a good choice for clock recovery, since the duty cycle of the output will match the duty cycle of the input.

The AD8561 has the same pinout as the LT1016, with lower supply current and a wider common-mode input range, which includes the negative supply rail.
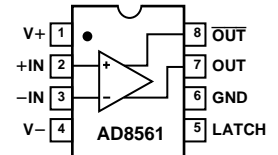
The AD8561 is specified over the industrial (–40°C to +85°C) temperature range. The AD8561 is available in both the 8-lead plastic DIP, 8-lead TSSOP or narrow SO-8 surface mount packages.
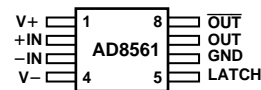
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AD8561–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (@ V+ = +5.0 V, V− = V$_{GND}$ = 0 V, T$_A$ = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V$_{OS}$			2.3	7	mV
		−40°C ≤ T$_A$ ≤ +85°C			8	mV
Offset Voltage Drift	ΔV$_{OS}$/ΔT			4		μV/°C
Input Bias Current	I$_B$	V$_{CM}$ = 0 V	−6	−3		μA
	I$_B$	−40°C ≤ T$_A$ ≤ +85°C	−7	−3.5		μA
Input Offset Current	I$_{OS}$	V$_{CM}$ = 0 V			±4	μA
Input Common-Mode Voltage Range	V$_{CM}$		0.0		+3.0	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V$_{CM}$ ≤ +3.0 V	65	85		dB
Large Signal Voltage Gain	A$_{VO}$	R$_L$ = 10 kΩ		3000		V/V
Input Capacitance	C$_{IN}$			3.0		pF
LATCH ENABLE INPUT						
Logic "1" Voltage Threshold	V$_{IH}$		2.0	1.65		V
Logic "0" Voltage Threshold	V$_{IL}$			1.60	0.8	V
Logic "1" Current	I$_{IH}$	V$_{LH}$ = 3.0 V	−1.0	−0.3		μA
Logic "0" Current	I$_{IL}$	V$_{LL}$ = 0.3 V	−4	−2		μA
Latch Enable						
Pulsewidth	t$_{PW(E)}$			6		ns
Setup Time	t$_S$			1		ns
Hold Time	t$_H$			1.2		ns
DIGITAL OUTPUTS						
Logic "1" Voltage	V$_{OH}$	I$_{OH}$ = −50 μA, ΔV$_{IN}$ > 250 mV	3.5			V
Logic "1" Voltage	V$_{OH}$	I$_{OH}$ = −3.2 mA, ΔV$_{IN}$ > 250 mV	2.4	3.5		V
Logic "0" Voltage	V$_{OL}$	I$_{OL}$ = 3.2 mA, ΔV$_{IN}$ > 250 mV		0.25	0.4	V
DYNAMIC PERFORMANCE						
Propagation Delay	t$_P$	200 mV Step with 100 mV Overdrive		6.75	9.8	ns
		−40°C ≤ T$_A$ ≤ +85°C		8	13	ns
Propagation Delay	t$_P$	100 mV Step with 5 mV Overdrive		8		ns
Differential Propagation Delay						
(Rising Propagation Delay vs.						
Falling Propagation Delay)	Δt$_P$	100 mV Step with 100 mV Overdrive[1]		0.5	2.0	ns
Rise Time		20% to 80%		3.8		ns
Fall Time		80% to 20%		1.5		ns
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	+4.5 V ≤ V+ ≤ +5.5 V	50	65		dB
Positive Supply Current	I+			4.5	6.0	mA
		−40°C ≤ T$_A$ ≤ +85°C			7.5	mA
Ground Supply Current	I$_{GND}$	V$_O$ = 0 V, R$_L$ = ∞		2.2	3.3	mA
		−40°C ≤ T$_A$ ≤ +85°C			3.8	mA
Analog Supply Current	I−			2.3	4.5	mA
		−40°C ≤ T$_A$ ≤ +85°C			5.5	mA

NOTES
[1] Guaranteed by design.

Specifications subject to change without notice.

ELECTRICAL SPECIFICATIONS (@ V+ = +5.0 V, V– = V$_{GND}$ = 0 V, V– = –5 V, T$_A$ = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V$_{OS}$			1	7	mV
		–40°C ≤ T$_A$ ≤ +85°C			8	mV
Offset Voltage Drift	ΔV$_{OS}$/ΔT			4		μV/°C
Input Bias Current	I$_B$	V$_{CM}$ = 0 V	–6	–3		μA
	I$_B$	–40°C ≤ T$_A$ ≤ +85°C	–7	–2.5		μA
Input Offset Current	I$_{OS}$	V$_{CM}$ = 0 V			±4	μA
Input Common-Mode Voltage Range	V$_{CM}$		–5.0		+3.0	V
Common-Mode Rejection Ratio	CMRR	–5.0 V ≤ V$_{CM}$ ≤ +3.0 V	65	85		dB
Large Signal Voltage Gain	A$_{VO}$	R$_L$ = 10 kΩ		3000		V/V
Input Capacitance	C$_{IN}$			3.0		pF
LATCH ENABLE INPUT						
Logic "1" Voltage Threshold	V$_{IH}$		2.0	1.65		V
Logic "0" Voltage Threshold	V$_{IL}$			1.60	0.8	V
Logic "1" Current	I$_{IH}$	V$_{LH}$ = 3.0 V	–1	–0.5	20	μA
Logic "0" Current	I$_{IL}$	V$_{LL}$ = 0.3 V	–4	–2	20	μA
Latch Enable						
Pulsewidth	t$_{PW(E)}$			6		ns
Setup Time	t$_S$			1.0		ns
Hold Time	t$_H$			1.2		ns
DIGITAL OUTPUTS						
Logic "1" Voltage	V$_{OH}$	I$_{OH}$ = –3.2 mA	2.6	3.5		V
Logic "0" Voltage	V$_{OL}$	I$_{OL}$ = 3.2 mA		0.2	0.3	V
DYNAMIC PERFORMANCE						
Propagation Delay	t$_P$	200 mV Step with 100 mV Overdrive		6.5	9.8	ns
		–40°C ≤ T$_A$ ≤ +85°C		8	13	ns
Propagation Delay	t$_P$	100 mV Step with 5 mV Overdrive		7		ns
Differential Propagation Delay						
(Rising Propagation Delay vs.						
Falling Propagation Delay)	Δt$_P$	100 mV Step with 100 mV Overdrive[1]		0.5	2	ns
Rise Time		20% to 80%		3.8		ns
Fall Time		80% to 20%		1.5		ns
Dispersion				1		ns
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	±4.5 V ≤ V$_{CC}$ and V$_{EE}$ ≤ ±5.5 V	55	70		dB
Supply Current		V$_O$ = 0 V, R$_L$ = ∞				
Positive Supply Current	I+			4.7	6.5	mA
		–40°C ≤ T$_A$ ≤ +85°C			7.5	mA
Ground Supply Current	I$_{GND}$	V$_O$ = 0 V, R$_L$ = ∞		2.2	3.3	mA
		–40°C ≤ T$_A$ ≤ +85°C			3.8	mA
Negative Supply Current	I–			2.4	4.5	mA
		–40°C ≤ T$_A$ ≤ +85°C			5.5	mA

NOTES
[1] Guaranteed by design.

Specifications subject to change without notice.

AD8561–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (@ V+ = +3.0 V, V− = V$_{GND}$ = 0 V, T$_A$ = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V$_{OS}$				7	mV
Input Bias Current	I$_B$	V$_{CM}$ = 0 V	−6	−3.0		μA
Input Bias Current	I$_B$	−40°C ≤ T$_A$ ≤ +85°C	−7	−4		μA
Input Common-Mode Voltage Range	V$_{CM}$		0		+1.5	V
Common-Mode Rejection Ratio	CMRR	0.1 V ≤ V$_{CM}$ ≤ 1.5 V	60			dB
OUTPUT CHARACTERISTICS						
Output High Voltage	V$_{OH}$	I$_{OH}$ = −3.2 mA, V$_{IN}$ > 250 mV	1.2[1]			V
Output Low Voltage	V$_{OL}$	I$_{OL}$ = +3.2 mA, V$_{IN}$ > 250 mV			0.3	V
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	+2.7 V ≤ V$_{CC}$, V$_{EE}$ ≤ +6 V		40		dB
Supply Currents		V$_O$ = 0 V, R$_L$ = ∞				
V+ Supply Current	I+			4.0	4.5	mA
		−40°C ≤ T$_A$ ≤ +85°C			5.5	mA
Ground Supply Current	I$_{GND}$			1.6	2.5	mA
		−40°C ≤ T$_A$ ≤ +85°C			3.0	mA
V− Supply Current	I−			2.4	3.3	mA
		−40°C ≤ T$_A$ ≤ +85°C			3.8	mA
DYNAMIC PERFORMANCE						
Propagation Delay	t$_P$	100 mV Step with 20 mV Overdrive[2]		8.5	9.8	ns

NOTES
[1]Output high voltage without pull-up resistor. It may be useful to have a pull-up resistor to V+ for 3 V operation.
[2]Guaranteed by design.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS
Total Analog Supply Voltage . . . . +14 V
Digital Supply Voltage . . . . +14 V
Analog Positive Supply–Digital Positive Supply . . . . . −600 mV
Input Voltage[1] . . . . ±7 V
Differential Input Voltage . . . . ±8 V
Output Short-Circuit Duration to GND . . . . Indefinite
Storage Temperature Range
  N, R, RU Package . . . . −65°C to +150°C
Operating Temperature Range . . . . −40°C to +85°C
Junction Temperature Range
  N, R, RU Package . . . . −65°C to +150°C
Lead Temperature Range (Soldering, 10 sec) . . . .+300°C

Package Type	θ$_{JA}$[2]	θ$_{JC}$	Units
8-Lead Plastic DIP (N)	103	43	°C/W
8-Lead SO (R)	158	43	°C/W
8-Lead TSSOP	240	43	°C/W

NOTES
[1]The analog input voltage is equal to ±7 V or the analog supply voltage, whichever is less.
[2]θ$_{JA}$ is specified for the worst case conditions, i.e., θ$_{JA}$ is specified for device in socket for P-DIP and θ$_{JA}$ is specified for device soldered in circuit board for SOIC and TSSOP packages.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
AD8561AN	−40°C to +85°C	8-Lead Plastic DIP	N-8
AD8561ARU	−40°C to +85°C	8-Lead Thin Shrink Small Outline	RU-8
AD8561AR	−40°C to +85°C	8-Lead Small Outline IC	SO-8

CAUTION
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8561 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

WARNING!
ESD SENSITIVE DEVICE

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OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

8-Lead Plastic DIP
(N-8)

0.430 (10.92)
0.348 (8.84)

8   5

0.280 (7.11)
0.240 (6.10)

1   4

PIN 1

0.325 (8.25)
0.300 (7.62)

0.060 (1.52)
0.015 (0.38)

0.210 (5.33)
MAX

0.195 (4.95)
0.115 (2.93)

0.130
(3.30)
MIN

0.160 (4.06)
0.115 (2.93)

0.022 (0.558)   **0.100**   **0.070 (1.77)**
0.014 (0.356)   **(2.54)**   **0.045 (1.15)**
BSC

SEATING
PLANE
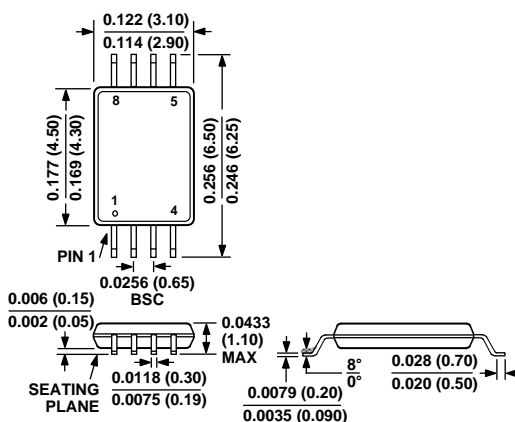
0.015 (0.381)
0.008 (0.204)

8-Lead Thin Shrink Small Outline
(RU-8)

0.122 (3.10)
0.114 (2.90)

8   5

0.177 (4.50)
0.169 (4.30)

0.256 (6.50)
0.246 (6.25)

1   4

PIN 1

0.0256 (0.65)
BSC

0.006 (0.15)
0.002 (0.05)

0.0433
(1.10)
MAX

SEATING
PLANE

0.0118 (0.30)
0.0075 (0.19)

0.0079 (0.20)
0.0035 (0.090)

8°
0°

0.028 (0.70)
0.020 (0.50)

8-Lead Small Outline IC
(SO-8)

0.1968 (5.00)
0.1890 (4.80)

8   5

0.1574 (4.00)
0.1497 (3.80)

0.2440 (6.20)
0.2284 (5.80)

1   4

PIN 1

0.0688 (1.75)
0.0532 (1.35)

0.0098 (0.25)
0.0040 (0.10)

0.0196 (0.50)
0.0099 (0.25) x 45°

SEATING
PLANE

0.0500   **0.0192 (0.49)**
(1.27)   **0.0138 (0.35)**
BSC

0.0098 (0.25)
0.0075 (0.19)

8°
0°

0.0500 (1.27)
0.0160 (0.41)

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