12-Bit, 125 MSPS High Performance TxDAC® D/A Converter

AD9752*

FEATURES

High Performance Member of Pin-Compatible TxDAC Product Family
125 MSPS Update Rate
12-Bit Resolution
Excellent Spurious Free Dynamic Range Performance
SFDR to Nyquist @ 5 MHz Output: 79 dBc
Differential Current Outputs: 2 mA to 20 mA
Power Dissipation: 185 mW @ 5 V
Power-Down Mode: 20 mW @ 5 V
On-Chip 1.20 V Reference
CMOS-Compatible +2.7 V to +5.5 V Digital Interface
Package: 28-Lead SOIC and TSSOP
Edge-Triggered Latches

APPLICATIONS

Wideband Communication Transmit Channel:
Direct IF
Basestations
Wireless Local Loop
Digital Radio Link
Direct Digital Synthesis (DDS)
Instrumentation

PRODUCT DESCRIPTION

The AD9752 is a 12-bit resolution, wideband, second generation member of the TxDAC series of high performance, low power CMOS digital-to-analog-converters (DACs). The TxDAC family, which consists of pin compatible 8-, 10-, 12-, and 14-bit DACs, is specifically optimized for the transmit signal path of communication systems. All of the devices share the same interface options, small outline package and pinout, thus providing an upward or downward component selection path based on performance, resolution and cost. The AD9752 offers exceptional ac and dc performance while supporting update rates up to 125 MSPS.

The AD9752's flexible single-supply operating range of 4.5 V to 5.5 V and low power dissipation are well suited for portable and low power applications. Its power dissipation can be further reduced to a mere 65 mW, without a significant degradation in performance, by lowering the full-scale current output. Also, a power-down mode reduces the standby power dissipation to approximately 20 mW.

The AD9752 is manufactured on an advanced CMOS process. A segmented current source architecture is combined with a proprietary switching technique to reduce spurious components and enhance dynamic performance. Edge-triggered input latches and a 1.2 V temperature compensated bandgap reference have been integrated to provide a complete monolithic DAC solution. The digital inputs support +2.7 V to +5 V CMOS logic families.

TxDAC is a registered trademark of Analog Devices, Inc.
*Protected by U.S. Patents Numbers 5450084, 5568145, 5689257, 5612697 and 5703519. Other patents pending.

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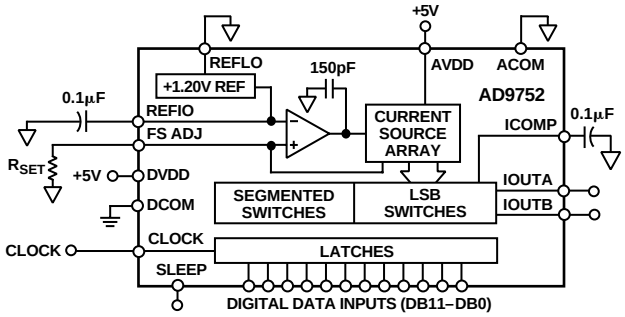
FUNCTIONAL BLOCK DIAGRAM



The AD9752 is a current-output DAC with a nominal full-scale output current of 20 mA and > 100 kΩ output impedance.

Differential current outputs are provided to support single-ended or differential applications. Matching between the two current outputs ensures enhanced dynamic performance in a differential output configuration. The current outputs may be tied directly to an output resistor to provide two complementary, single-ended voltage outputs or fed directly into a transformer. The output voltage compliance range is 1.25 V.

The on-chip reference and control amplifier are configured for maximum accuracy and flexibility. The AD9752 can be driven by the on-chip reference or by a variety of external reference voltages. The internal control amplifier, which provides a wide (>10:1) adjustment span, allows the AD9752 full-scale current to be adjusted over a 2 mA to 20 mA range while maintaining excellent dynamic performance. Thus, the AD9752 may operate at reduced power levels or be adjusted over a 20 dB range to provide additional gain ranging capabilities.

The AD9752 is available in 28-lead SOIC and TSSOP packages. It is specified for operation over the industrial temperature range.

PRODUCT HIGHLIGHTS

1. The AD9752 is a member of the wideband TxDAC product family that provides an upward or downward component selection path based on resolution (8 to 14 bits), performance and cost. The entire family of TxDACs is available in industry standard pinouts.
2. Manufactured on a CMOS process, the AD9752 uses a proprietary switching technique that enhances dynamic performance beyond that previously attainable by higher power/cost bipolar or BiCMOS devices.
3. On-chip, edge-triggered input CMOS latches interface readily to +2.7 V to +5 V CMOS logic families. The AD9752 can support update rates up to 125 MSPS.
4. A flexible single-supply operating range of 4.5 V to 5.5 V and a wide full-scale current adjustment span of 2 mA to 20 mA allow the AD9752 to operate at reduced power levels.
5. The current output(s) of the AD9752 can be easily configured for various single-ended or differential circuit topologies.

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AD9752–SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = +5 V, DVDD = +5 V, I_{OUTFS} = 20 mA, unless otherwise noted)

Parameter	Min	Typ	Max	Units
RESOLUTION	12			Bits
DC ACCURACY[1]				
Integral Linearity Error (INL)				
T_A = +25°C	–1.5	±0.5	+1.5	LSB
T_{MIN} to T_{MAX}	–2.0		+2.0	LSB
Differential Nonlinearity (DNL)				
T_A = +25°C	–0.75	±0.25	+0.75	LSB
T_{MIN} to T_{MAX}	–1.0		+1.0	LSB
ANALOG OUTPUT				
Offset Error	–0.02		+0.02	% of FSR
Gain Error (Without Internal Reference)	–2	±0.5	+2	% of FSR
Gain Error (With Internal Reference)	–5	±1.5	+5	% of FSR
Full-Scale Output Current[2]	2.0		20.0	mA
Output Compliance Range	–1.0		1.25	V
Output Resistance		100		kΩ
Output Capacitance		5		pF
REFERENCE OUTPUT				
Reference Voltage	1.14	1.20	1.26	V
Reference Output Current[3]		100		nA
REFERENCE INPUT				
Input Compliance Range	0.1		1.25	V
Reference Input Resistance		1		MΩ
Small Signal Bandwidth		0.5		MHz
TEMPERATURE COEFFICIENTS				
Offset Drift		0		ppm of FSR/°C
Gain Drift (Without Internal Reference)		±50		ppm of FSR/°C
Gain Drift (With Internal Reference)		±100		ppm of FSR/°C
Reference Voltage Drift		±50		ppm/°C
POWER SUPPLY				
Supply Voltages				
AVDD	4.5	5.0	5.5	V
DVDD	2.7	5.0	5.5	V
Analog Supply Current (I_{AVDD})[4]		34	39	mA
Digital Supply Current (I_{DVDD})[5]		3	5	mA
Supply Current Sleep Mode (I_{AVDD})[6]		4	8	mA
Power Dissipation[5] (5 V, I_{OUTFS} = 20 mA)		185	220	mW
Power Supply Rejection Ratio[7]—AVDD	–0.4		+0.4	% of FSR/V
Power Supply Rejection Ratio[7]—DVDD	–0.025		+0.025	% of FSR/V
OPERATING RANGE	–40		+85	°C

NOTES
[1]Measured at IOUTA, driving a virtual ground.
[2]Nominal full-scale current, I_{OUTFS}, is 32 × the I_{REF} current.
[3]Use an external buffer amplifier to drive any external load.
[4]Requires +5 V supply.
[5]Measured at f_{CLOCK} = 25 MSPS and I_{OUT} = static full scale (20 mA).
[6]Logic level for SLEEP pin must be referenced to AVDD. Min V_{IH} = 3.5 V.
[7]±5% Power supply variation.

Specifications subject to change without notice.

DYNAMIC SPECIFICATIONS

(T_{MIN} to T_{MAX}, AVDD = +5 V, DVDD = +5 V, I_{OUTFS} = 20 mA, Differential Transformer Coupled Output, 50 Ω Doubly Terminated, unless otherwise noted)

Parameter	Min	Typ	Max	Units
DYNAMIC PERFORMANCE				
Maximum Output Update Rate (f_{CLOCK})	125			MSPS
Output Settling Time (t_{ST}) (to 0.1%)[1]		35		ns
Output Propagation Delay (t_{PD})		1		ns
Glitch Impulse		5		pV-s
Output Rise Time (10% to 90%)[1]		2.5		ns
Output Fall Time (10% to 90%)[1]		2.5		ns
Output Noise (I_{OUTFS} = 20 mA)		50		pA/√Hz
Output Noise (I_{OUTFS} = 2 mA)		30		pA/√Hz
AC LINEARITY				
Spurious-Free Dynamic Range to Nyquist				
f_{CLOCK} = 25 MSPS; f_{OUT} = 1.00 MHz				
0 dBFS Output				
T_A = +25°C	75	84		dBc
–6 dBFS Output		76		dBc
–12 dBFS Output		81		dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 1.00 MHz		81		dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 2.51 MHz		81		dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 5.02 MHz		76		dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 14.02 MHz		62		dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 20.2 MHz		60		dBc
f_{CLOCK} = 100 MSPS; f_{OUT} = 2.5 MHz		78		dBc
f_{CLOCK} = 100 MSPS; f_{OUT} = 5 MHz		76		dBc
f_{CLOCK} = 100 MSPS; f_{OUT} = 20 MHz		63		dBc
f_{CLOCK} = 100 MSPS; f_{OUT} = 40 MHz		55		dBc
Spurious-Free Dynamic Range within a Window				
f_{CLOCK} = 25 MSPS; f_{OUT} = 1.00 MHz	84	93		dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 5.02 MHz; 2 MHz Span		86		dBc
f_{CLOCK} = 100 MSPS; f_{OUT} = 5.04 MHz; 4 MHz Span		86		dBc
Total Harmonic Distortion				
f_{CLOCK} = 25 MSPS; f_{OUT} = 1.00 MHz				
T_A = +25°C		–82	–74	dBc
f_{CLOCK} = 50 MHz; f_{OUT} = 2.00 MHz		–76		dBc
f_{CLOCK} = 100 MHz; f_{OUT} = 2.00 MHz		–76		dBc
Multitone Power Ratio (8 Tones at 110 kHz Spacing)				
f_{CLOCK} = 20 MSPS; f_{OUT} = 2.00 MHz to 2.99 MHz				
0 dBFS Output		81		dBc
–6 dBFS Output		81		dBc
–12 dBFS Output		85		dBc
–18 dBFS Output		86		dBc

NOTES

[1]Measured single ended into 50 Ω load.

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = +5 V, DVDD = +5 V, I_{OUTFS} = 20 mA, unless otherwise noted)

Parameter	Min	Typ	Max	Units
DIGITAL INPUTS				
Logic "1" Voltage @ DVDD = +5 V[1]	3.5	5		V
Logic "1" Voltage @ DVDD = +3 V	2.1	3		V
Logic "0" Voltage @ DVDD = +5 V[1]		0	1.3	V
Logic "0" Voltage @ DVDD = +3 V		0	0.9	V
Logic "1" Current	–10		+10	µA
Logic "0" Current	–10		+10	µA
Input Capacitance		5		pF
Input Setup Time (t_S)	2.0			ns
Input Hold Time (t_H)	1.5			ns
Latch Pulsewidth (t_{LPW})	3.5			ns

NOTES
[1]When DVDD = +5 V and Logic 1 voltage ≈3.5 V and Logic 0 voltage ≈1.3 V. IVDD can increase by up to 10 mA, depending on f_{CLOCK}.
Specifications subject to change without notice.

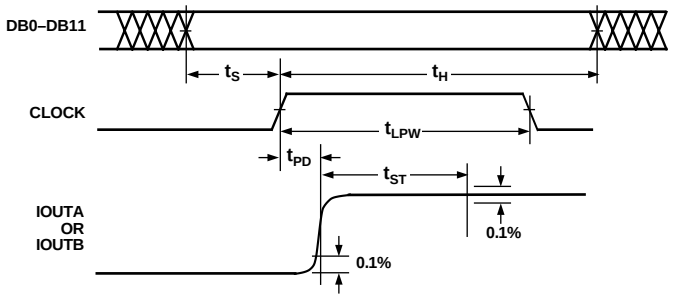

Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
AVDD	ACOM	–0.3	+6.5	V
DVDD	DCOM	–0.3	+6.5	V
ACOM	DCOM	–0.3	+0.3	V
AVDD	DVDD	–6.5	+6.5	V
CLOCK, SLEEP	DCOM	–0.3	DVDD + 0.3	V
Digital Inputs	DCOM	–0.3	DVDD + 0.3	V
IOUTA, IOUTB	ACOM	–1.0	AVDD + 0.3	V
ICOMP	ACOM	–0.3	AVDD + 0.3	V
REFIO, FSADJ	ACOM	–0.3	AVDD + 0.3	V
REFLO	ACOM	–0.3	+0.3	V
Junction Temperature			+150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			+300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options*
AD9752AR	–40°C to +85°C	28-Lead 300 Mil SOIC	R-28
AD9752ARU	–40°C to +85°C	28-Lead TSSOP	RU-28
AD9752-EB		Evaluation Board	

*R = Small Outline IC; RU = Thin Shrink Small Outline Package.

THERMAL CHARACTERISTICS

Thermal Resistance

28-Lead 300 Mil SOIC
θ_{JA} = 71.4°C/W
θ_{JC} = 23°C/W
28-Lead TSSOP
θ_{JA} = 97.9°C/W
θ_{JC} = 14.0°C/W

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9752 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.